the european cmos selection



MOTOROLA Semiconductors

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Prepared by
Technical Information Center

This book presents technical data for the broad line of CMOS integrated circuits. Complete specifications are provided in the form of data sheets.

The comprehensive specifications for the B Series reflect the industry specification developed under the auspices of EIA/JEDEC. This coordination permits multiple sources of the B Series of devices.

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NUMERICAL INDEX

ORDERING INFORMATION – SUFFIXES*

AL – 3 to 18 V, –55 to +125 °C, ceramic package
CL – 3 to 18 V, –40 to +85 °C, ceramic package
CP – 3 to 18 V, –40 to +85 °C, plastic package
L – Limited voltage range, limited temperature range, ceramic package
P – Limited voltage range, limited temperature range, plastic package
EFL – 3 to 18 V, –55 to +125 °C, ceramic package
FL – 3 to 18 V, –40 to +85 °C, ceramic package
FP – 3 to 18 V, –40 to +85 °C, plastic package
EVL – 3 to 6 V, –55 to +125 °C, ceramic package
VL – 3 to 6 V, –40 to +85 °C, ceramic package
VP – 3 to 6 V, –40 to +85 °C, plastic package
Z – Limited voltage range, limited temperature range, leadless ceramic package.

Part Number	Function	Class	Suffix*	Pins	Available in HI-REL	Page
MC14000UB	Dual 3-Input NOR Gate plus Inverter	SSI	AL,CL,CP	14	√	9-3
MC14001B	Quad 2-Input NOR Gate	SSI	AL,CL,CP	14	√	9-6
MC14001UB	Quad 2-Input NOR Gate	SSI	AL,CL,CP	14	√	9-14
MC14002B	Dual 4-Input NOR Gate	SSI	AL,CL,CP	14	√	9-18
MC14002UB	Dual 4-Input NOR Gate	SSI	AL,CL,CP	14	√	9-18
MC14006B	18-Bit Static Shift Register	MSI	AL,CL,CP	14	√	9-19
MC14007UB	Dual Complementary Pair plus Inverter	SSI	AL,CL,CP	14	√	9-23
MC14008B	4-Bit Full Adder	MSI	AL,CL,CP	16	√	9-27
MC14009UB	Hex Inverter/Buffer	SSI	AL,CL,CP	16	√	9-33
MC14010B	Hex Buffer	SSI	AL,CL,CP	16	√	9-33
MC14011B	Quad 2-Input NAND Gate	SSI	AL,CL,CP	14	√	9-40
MC14011UB	Quad 2-Input NAND Gate	SSI	AL,CL,CP	14	√	9-40
MC14012B	Dual 4-Input NAND Gate	SSI	AL,CL,CP	14	√	9-41
MC14012UB	Dual 4-Input NAND Gate	SSI	AL,CL,CP	14	√	9-41
MC14013B	Dual D Flip-Flop	SSI	AL,CL,CP	14	√	9-42
MC14014B	8-Bit Static Shift Register (Synchronous)	MSI	AL,CL,CP	16	√	9-46
MC14015B	Dual 4-Bit Static Shift Register	MSI	AL,CL,CP	16	√	9-50
MC14016B	Quad Analog Switch/Quad Multiplexer	SSI	AL,CL,CP	14	√	9-56
MC14017B	Decade Counter/Divider	MSI	AL,CL,CP	16	√	9-62
MC14018B	Presettable Divide-by-N Counter	MSI	AL,CL,CP	16	√	9-67
MC14020B	14-Bit Binary Counter	MSI	AL,CL,CP	16	√	9-71
MC14021B	8-Bit Static Shift Register (Asynchronous)	MSI	AL,CL,CP	16	√	9-75
MC14022B	Octal Counter/Divider	MSI	AL,CL,CP	16	√	9-76
MC14023B	Triple 3-Input NAND Gate	SSI	AL,CL,CP	14	√	9-81
MC14023UB	Triple 3-Input NAND Gate	SSI	AL,CL,CP	14	√	9-81
MC14024B	7-Stage Ripple Counter	SSI	AL,CL,CP	14	√	9-82
MC14025B	Triple 3-Input NOR Gate	SSI	AL,CL,CP	14	√	9-87
MC14025UB	Triple 3-Input NOR Gate	SSI	AL,CL,CP	14	√	9-87
MC14027B	Dual J-K Flip-Flop	SSI	AL,CL,CP	16	√	9-88
MC14028B	BCD-to-Decimal Decoder	MSI	AL,CL,CP	16	√	9-92
MC14029B	4-Bit Presettable Up/Down Counter	MSI	AL,CL,CP	16	√	9-97
MC14032B	Triple Serial Adder (Positive Logic)	MSI	AL,CL,CP	16	√	9-103
MC14034B	8-Bit Universal Bus Register	LSI	AL,CL,CP	24	√	9-108
MC14035B	4-Bit Shift Register	MSI	AL,CL,CP	16	√	9-115
MC14038B	Triple Serial Adder (Negative Logic)	MSI	AL,CL,CP	16	√	9-119

* Add suffix to part number on all orders.

Chips are available for all CMOS types. Consult your Motorola Sales Office or Authorized Motorola Distributor.

Part Number	Function	Class	Suffix*	Pins	Available in HI-REL	Page
MC14040B	12-Bit Binary Counter	MSI	AL,CL,CP	16	√	9-120
MC14042B	Quad Latch	SSI	AL,CL,CP	16	√	9-124
MC14043B	Quad NOR R-S Latch	MSI	AL,CL,CP	16	√	9-128
MC14044B	Quad NAND R-S Latch	MSI	AL,CL,CP	16	√	9-128
MC14046B	Phase-Locked Loop	MSI	AL,CL,CP	16	√	9-132
MC14049UB	Hex Inverter/Buffer	SSI	AL,CL,CP	16	√	9-137
MC14050B	Hex Buffer	SSI	AL,CL,CP	16	√	9-137
MC14051B	8-Channel Analog Multiplexer	MSI	AL,CL,CP	16	√	9-141
MC14052B	Dual 4-Channel Analog Multiplexer	MSI	AL,CL,CP	16	√	9-141
MC14053B	Triple 2-Channel Analog Multiplexer	MSI	AL,CL,CP	16	√	9-141
MC14066B	Quad Analog Switch	SSI	AL,CL,CP	14	√	9-147
MC14068B	8-Input NAND Gate	SSI	AL,CL,CP	14	√	9-152
MC14069UB	Hex Inverter	SSI	AL,CL,CP	14	√	9-153
MC14070B	Quad Exclusive OR Gate	SSI	AL,CL,CP	14	√	9-155
MC14071	Quad 2-Input OR Gate	SSI	AL,CL,CP	14	√	9-157
MC14071B	Quad 2-Input OR Gate	SSI	AL,CL,CP	14	√	9-157
MC14072B	Dual 4-Input OR Gate	SSI	AL,CL,CP	14	√	9-158
MC14073B	Triple 3-Input AND Gate	SSI	AL,CL,CP	14	√	9-159
MC14075B	Triple 3-Input OR Gate	SSI	AL,CL,CP	14	√	9-160
MC14076B	Quad D-Type Register	MSI	AL,CL,CP	16	√	9-161
MC14077B	Quad Exclusive NOR Gate	SSI	AL,CL,CP	14	√	9-165
MC14078B	8-Input NOR Gate	SSI	AL,CL,CP	14	√	9-166
MC14081	Quad 2-Input AND Gate	SSI	AL,CL,CP	14	√	9-167
MC14081B	Quad 2-Input AND Gate	SSI	AL,CL,CP	14	√	9-167
MC14082B	Dual 4-Input AND Gate	SSI	AL,CL,CP	14	√	9-168
MC14093B	Quad 2-Input NAND Schmitt Trigger	SSI	AL,CL,CP	14	√	9-169
MC14094B	8-Bit Bus-Compatible Shift Store Latch	MSI	AL,CL,CP	16	√	9-173
MC14099B	8-Bit Addressable Latch	MSI	AL,CL,CP	16	√	9-177
MC14160B	Decade Counter (Asynchronous Clear)	MSI	AL,CL,CP	16	√	9-183
MC14161B	Binary Counter (Asynchronous Clear)	MSI	AL,CL,CP	16	√	9-183
MC14162B	Decade Counter (Synchronous Clear)	MSI	AL,CL,CP	16	√	9-183
MC14163B	Binary Counter (Synchronous Clear)	MSI	AL,CL,CP	16	√	9-183
MC14174B	Hex D-Flip-Flop	MSI	AL,CL,CP	16	√	9-191
MC14175B	Quad D-Flip-Flop	SSI	AL,CL,CP	16	√	9-195
MC14194B	4-Bit Universal Shift Register	MSI	AL,CL,CP	16	√	9-199
MC14403	Tone Encoder	LSI	L,P	16		9-203
MC14405	Tone Encoder	LSI	L,P	18		9-203
MC14406	Pulse Code Modulator	LSI	L,P	28		9-207
MC14407	Pulse Code Modulator	LSI	L,P	24		9-207
MC14408	Binary-to-Phone Pulse Converter	LSI	L,P	16		9-217
MC14409	Binary-to-Phone Pulse Converter	LSI	L,P	16		9-217
MC14410	2-of-8 Tone Encoder	LSI	L,P	16		9-225
MC14411	Bit-Rate Frequency Generator	LSI	L,P	24		9-229
MC14412	Universal Low-Speed Modem	LSI	FL,VL,FP,VP	16		9-232
MC14413	PCM CODEC, Sampled Data Filter	LSI	P,L	16		8-2
MC14415	Quad Precision Timer/Driver	LSI	EFL,FL,FP, EVL,VL,VP	16		9-237
MC14419	2-of-8 Keypad-to-Binary Encoder	MSI	L,P	16		9-242
MC14421	Tuning Mem. System Mem. Interface Circuit	LSI	P	24		8-3
MC14422	Remote Control Transmitter	MSI	P	16		9-246

* Suffixes defined on page 1.

Part Number	Function	Class	Suffix*	Pins	Available in HI-REL	Page
MC14424	Remote Control Transmitter	MSI	P	16		9-252
MC14425	Tuning Memory Control	LSI	P	18		9-257
MC14426	Tuning Memory Circuit	MSI	P	16		9-261
MC14429-A	Tuning Memory Control	LSI	P	18		9-264
MC14430	Input Addressing Encoder	MSI	P	16		9-268
MC14433	3-½ Digit A/D Converter	LSI	L,P	24		9-272
MC14435	3-½ Digit A/D Logic Subsystem	LSI	EFL,FL,FP, EVL,VL,VP	16		9-285
MC14443	8-Channel A/D Converter	MSI	L,P	16		9-292
MC14447	8-Channel A/D Converter	MSI	L,P	16		9-292
MC14450	Oscillator/2^{16} Divider/Buffer	SSI	L,P	6		9-296
MC14451	Oscillator/Divider/Buffer	MSI	L,P	16		9-300
MC14457	Transmitter	LSI	P	16		9-304
MC14458	Receiver	LSI	P	24		9-304
MC14459	Automotive Speed Control Processor	LSI	P,L	16		9-315
MC14461	Smoke Detector, Ion Type	MSI	P	16		9-322
MC14462	Smoke Detector, Ion Type, FET	MSI	P	16		9-322
MC14464	Smoke Detector Circuit	MSI	P	16		9-332
MC14465	Smoke Detector Circuit	MSI	P	16		9-332
MC14466	Low Cost Smoke Detector	MSI	P	16		8-4
MC14469	Addressable Asynchr. Receiver/Transmitter	LSI	L,P	40		9-336
MC14490	Hex Contact Bounce Eliminator	LSI	EFL,FL,FP, EVL,VL,VP	16	√	9-344
MC14491	Multifunction Debounce Circuit	MSI	L,P	16		9-351
MC14492	Dual 2 x 2 Cross Point Matrix	MSI	L,P	16		9-352
MC14493	BCD-to-7 Segment Decoder Driver/Latch	MSI	P	16		9-353
MC14494	BCD-to-7 Segment Decoder Driver/Latch	MSI	P	16		9-353
MC14495	BCD-to-7 Segment Decoder Driver/Latch	MSI	L,P	16		9-357
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MC14526B	Programmable Binary Divide-by-N Counter	MSI	AL,CL,CP	16	√	9-473
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MC14528B	Dual Monostable Multivibrator	MSI	AL,CL,CP	16	√	9-480
MC14529B	Dual 4-Channel Analog Data Selector	MSI	AL,CL,CP	16	√	9-485
MC14530B	Dual 5-Input Majority Logic Gate	SSI	AL,CL,CP	16	√	9-491
MC14531B	12-Bit Parity Tree	MSI	AL,CL,CP	16	√	9-496
MC14532B	8-Bit Priority Encoder	MSI	AL,CL,CP	16	√	9-499
MC14534B	Real Time 5-Decade Counter	LSI	AL,CL,CP	24	√	9-505
MC14536B	Programmable Timer	LSI	AL,CL,CP	16	√	9-511
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MC14543B	BCD-to-7 Segment Latch/Decoder/Driver	MSI	AL,CL,CP	16	√	9-544
MC14544B	BCD-to-7 Segment Latch/Decoder/Driver — Ripple Blanking	MSI	AL,CL,CP	18	√	9-549
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MC14549B	Successive Approximation Register	MSI	AL,CL,CP	16	√	9-559
MC14551B	Quad 2-Channel Analog MUX	MSI	AL,CL,CP	16	√	9-566
MCM14552	64 x 4-Bit Static RAM	LSI	AL,CL,CP	24	√	9-572
MC14553B	3-Digit BCD Counter	LSI	AL,CL,CP	16	√	9-579
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MC14556B	Dual Binary to 1-of-4 Decoder (Inverting)	SSI	AL,CL,CP	16	√	9-589
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MC14560B	NBCD Adder	MSI	AL,CL,CP	16	√	9-602
MC14561B	9's Complementer	SSI	AL,CL,CP	14	√	9-606
MC14562B	128-Bit Static Shift Register	LSI	AL,CL,CP	14	√	9-612
MC14566B	Industrial Time-Base Generator	MSI	AL,CL,CP	16	√	9-616
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MC14569B	Dual Programmable BCD Binary Counter	MSI	AL,CL,CP	16	√	9-632
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MC14574	Quad Programmable Comparator	MSI	AL,CL,CP	16	√	9-639
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MC14583B	Dual Schmitt Trigger	SSI	AL,CL,CP	16	√	9-657
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MC14598B	8-Bit Bus Compatible Addressable Latch	MSI	AL,CL,CP	18		9-671

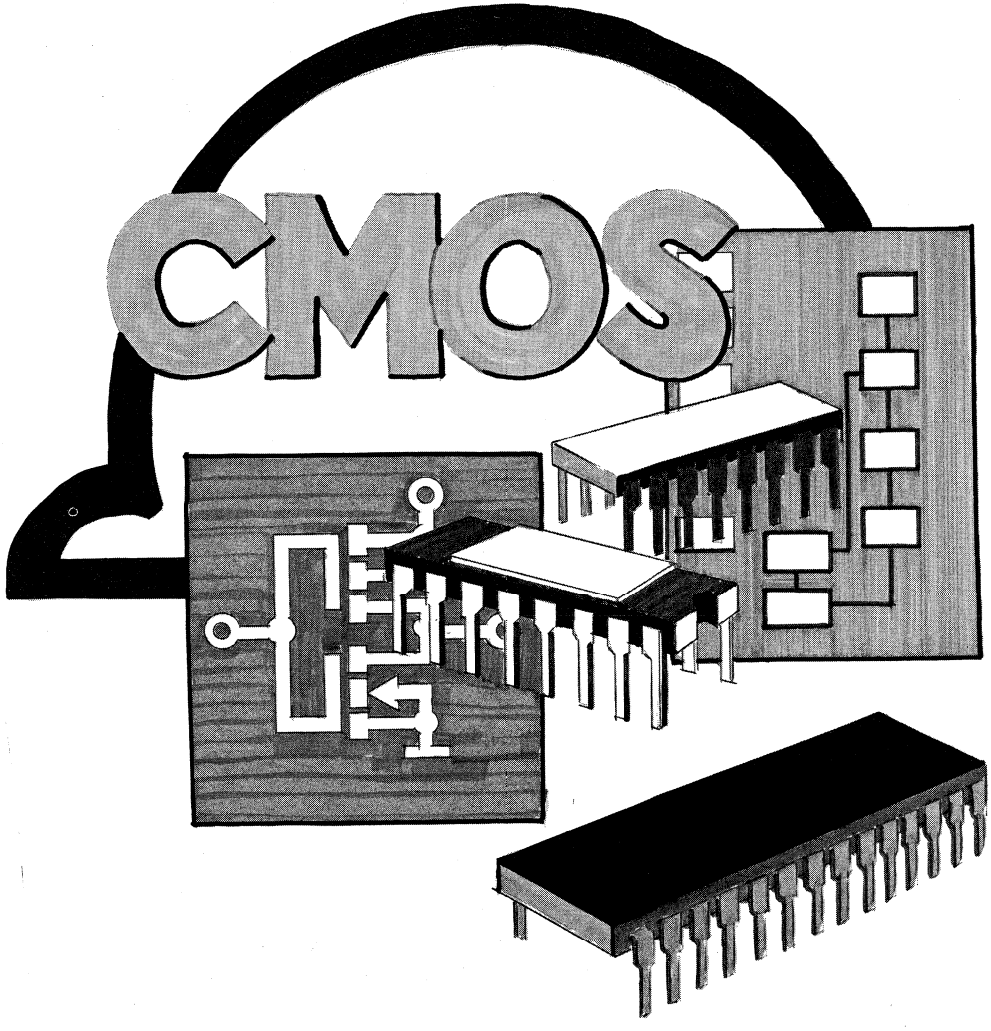
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MC144110	Hex D/A Converter	LSI	P	18		8-9
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MC145100	4 x 4 Cross Point Switch w/Control Memory	MSI	L,P	16		9-688
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MC145107	PLL Frequency Synthesizer	MSI	P	16		9-695
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MCM146504	4096 x 1-Bit Static RAM	LSI	L,P	18		9-701
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Product selection guide 1



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MC14507	Quad Exclusive OR Gate	9-395
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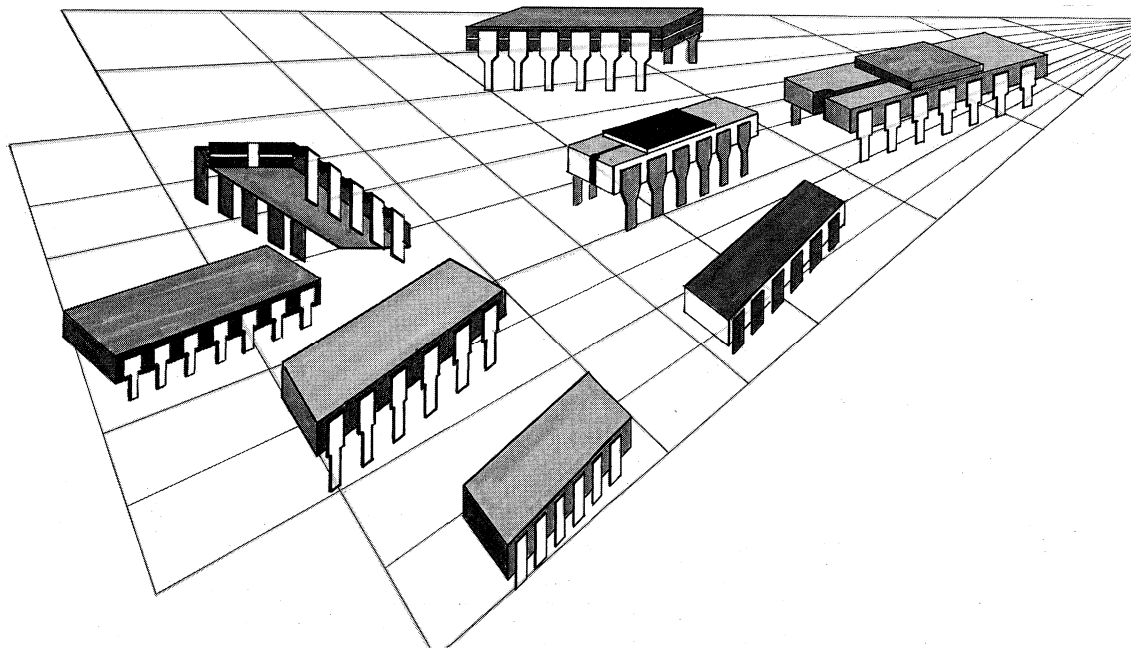
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Summary of Motorola CMOS line



SUMMARY OF MOTOROLA CMOS LINE

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Gates							
Single-Level			Multi-Level				
NOR/NAND	OR/AND	Buffers & Inverters	Multifunction/ AOI	Decoders/ Encoders	Schmitt Triggers	Flip-Flops/ Latches	Multi-vibrators
MC14000	MC14071	MC14007UB	MC14070B	MC14028B	MC14093B	MC14013B	MC14528B
MC14001UB	MC14071B	MC14049UB	MC14077B	MC14514B	MC14583B	MC14027B	MC14538B
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MC14002UB	MC14073B	MC14069UB	MC14507	MC14532B		MC14043B	
MC14002B	MC14075B	MC14502B	MC14519B	MC14555B		MC14044B	
MC14011UB	MC14081	MC14503B	MC14530B	MC14556B		MC14076B	
MC14011B	MC14081B	MC14009UB				MC14174B	
MC14012UB	MC14082B	MC14010B				MC14175B	
MC14012B						MC14508B	
MC14023UB		MC14504B				MC14099B	
MC14023B						MC14598B	
MC14025UB						MC14599B	
MC14025B						MC14597B	
MC14068B							
MC14078B							
MC14093B							
MC14501							
MC14572UB							

	Counters			Phase-Locked Loop	Memories		
Shift Registers	Ripple	Synchronous	Oscillators & Timers		Multiport Register	RAMs	ROMs
MC14006B	MC14020B	MC14017B	MC14450	MC14046B	MC14580B	MCM14505	MCM14524
MC14014B	MC14024B	MC14018B	MC14451	MC14568B		MCM14537	
MC14015B	MC14040B	MC14022B		MC145104		MCM14552	
MC14021B	MC14534B	MC14160B	MC14521B	MC145106		MCM145101	
MC14034B	MC14566B	MC14161B	MC14536B	MC145107		MCM146508	
MC14035B	MC14029B	MC14162B		MC145109		MCM146504	
MC14194B		MC14163B		MC145112		MCM146518	
MC14517B		MC14510B	MC14541B			MCM146514*	
MC14557B		MC14516B					
MC14562B		MC14518B					
MC14094B		MC14520B					
		MC14522B					
		MC14526B					
		MC14553B					
		MC14569B					

Multiplexers/ Demultiplexers, Bilateral Switches	Display Drivers/ Encoders	Arithmetic Circuits			Communication/ Telephone	A/D Converters	Other Complex Functions
		Adders/ Comparators	ALU/Rate Multipliers	Parity Generator/ Checker			
MC14016B	MC14511B	MC14008B	MC14527B	MC14531B	MC14408		MC14415
MC14051B	MC14543B	MC14032B	MC14554B		MC14409	MC14433	MC14490
MC14052B	MC14558B	MC14038B	MC14581B		MC14410	MC14435	MC14469
MC14053B	MC14494	MC14560B			MC14411	MC14549B	MC14459
MC14066B	MC14495	MC14561B			MC14412	MC14559B	MC14491
MC14512B	MC14513B	MC14582B			MC14419	MC14443	MC146818
MC14519B	MC14547B	MC14585B			MC14405	MC14447	MC146819
MC14529B					MC14406	MC144110	
MC14539B					MC14492	MC144111	
MC14551B	MC14493				MC145100		
	MC14499				MC142100		
	MC14544B				MC14403		
	MC144100				MC14407		
					MC14413		

Microprocessors/ Industrial Control	Remote Control/ Tuning	Smoke Detectors	Op-Amps Comparators
MC14500	MC14421	MC14461	MC14573
MC1441000	MC14422	MC14462	MC14574
MC1441099	MC14424	MC14464	MC14575
MC1441200	MC14425	MC14465	
MC146805	MC14426	MC14466	
	MC14429-A		
	MC14430		
	MC14457		
	MC14458		
	MC14497		
	MCM144102		

High Reliability 3



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3

MOTOROLA DOCUMENTS

- **McMOS POR2***

  The Motorola BS9000 CMOS HI-REL Brochure.

- **Motorola – British Standard Cross reference ***

  Lists the BS9000 qualified Motorola CMOS parts, CMOS part numbers and detail specification numbers.

- **Certified Test Records****

  Summarises periodic and lot-by-lot cumulative results of tests and inspections performed on released lots.

* Available from Sales Offices.
** Available upon request to East Kilbride Quality Assurance Department.

INTRODUCTION

High Reliability CMOS Integrated Circuits

Motorola at East Kilbride is the European Centre for CMOS and NMOS products and can offer customers High Reliability (HI-REL) parts to European Quality Assurance schemes. European standards are becoming more widely recognised and adopted so much so that Motorola has built up off the shelf inventories in our bonded warehouse at East Kilbride and will do so in some of our European distributor locations.

MOTOROLA – EUROPEAN INVOLVEMENT IN HIGH RELIABILITY MARKETS

At the end of 1975 Motorola Ltd. Semiconductor Division in the UK embarked on a strategy which by 1980 will make the East Kilbride factory Europe's principle source of Hi-REL MOS components.

The basis of the Motorola HI-REL activity is qualification under the rules of BS9000 in our BS/CECC approved plant.

Subsidiary qualification activities include ESA/GFW and BS9400 Category S11 (recognised by British Post Office).

It is a primary concern of the HI-REL operation to serve the needs of the market place whether these are Telecommunications, Military, Industrial, Avionics, Space or Special Applications by:

- Providing a complete technology in the East Kilbride Plant.
- Ensuring the highest quality attainable for product manufactured in the HI-REL operation.
- Maintaining close liaison and co-operation with the Ministry of Defence, BSI and the British Post Office.
- Complementing our discrete and linear HI-REL operation in Toulouse, France.

Motorola East Kilbride is dedicated to serving the European HI-REL markets.

BS9000 – MOTOROLA INVOLVEMENT

Motorola at East Kilbride is engaged in qualifying CMOS to BS9000, the qualification approval programs being undertaken involved initially the Motorola standard CMOS range of parts and latterly, in collaboration with the UK Ministry of Defence, the preparation of a common detail specification known as common "F". These common specifications are compatible with the JEDEC B standards and it is expected that they will become a British and European Industry Standard.

All BS9000 specifications will eventually be homologated within the framework of the CECC 90,000 specification system which Motorola actively supports.

It is expected that both the full range of Motorola "F" and Common "F" parts will be qualified by the end of 1979.

BS9000 – WHAT DO CUSTOMERS GET?

- Product made wholly in the UK in approved premises.
- Product released by an Inspection organisation approved by the National Supervising Inspectorate (NSI).
- Product released to specifications adopted and copyrighted by BSI.
- Mandatory sample life tests and environmental tests.
- Several optional 100% screening levels.
- Recognition under British and German Military qualified parts lists.
- BS9000 release certificates with each lot supported by audits of records by the NSI.
- Summary certified test records compiled every six months.
- Qualification approval test data and lot release test data on request.

THE BS9000 SCHEME

BS9000 is a scheme for providing electronic components of assessed quality controlled by the British Standards Institution (BSI) and operated by the National Supervising Inspectorate (NSI). It is associated with corresponding schemes in other European Countries and is compatible with schemes being set up by the CENELEC* Electronics Components Committee (CECC) and the International Electrotechnical Commission (IEC).

The BS9000 Scheme includes two essential features of any Quality Assurance Scheme, namely:

- A system of specifications.
- A certification procedure supported by an independent inspectorate.

* CENELEC – The European Committee for Electrotechnical Standardisation.

BS9000 – IN OPERATION

The BS9000 scheme operates essentially in three parts.

Part 1. The plant qualification.
Part 2. The Device qualification.
Part 3. Maintenance of qualification.

Part 1. Establishes to the satisfaction of the National Supervising Inspectorate (NSI) that the organisation has adequate quality systems, procedures and standards to control the manufacture of electronic components to the minimum standard defined in the BS9000 rules document.

Part 2. Establishes by demonstration to the NSI that the electronic components are capable of meeting the requirements of detail specifications which were prepared in accordance with the BS9000 Rules Document. This is accomplished by performing the qualification activity.

Part 3. Establishes on a lot-by-lot and periodic sampling basis that the parts continue to conform to the specification to which they were initially qualified. Data on those results of these tests is provided in the form of test records – CTRs., certified by a representative of the NSI. Certified Test Records are published at 6 monthly intervals. An example is printed at the back of this section. Also, at this stage should any lot be classified as rejected it will become disqualified from being released as a BS part. No re-submission of rejected lots is permitted.

BS9000 – DOCUMENTS

The following documents referenced in each detail specification are essential to a full understanding of the BS9000 scheme.

Document	Title
BS9000	General requirements for electronic parts of assessed quality.
BS2011	Basic environmental testing procedures.
BS3934	Dimensions of semiconductor devices.
BS6001	Sampling procedures and tables for inspection by attributes.
BS9400	Integrated electronic circuits of assessed quality: generic data and methods of test.

BS9000

The following lists some European Sales Agents for BSI documents.

AUSTRIA Österreichisches Normunginstitut, Vienna.
BELGIUM Institut Belge de Normalisation, Brussels.
DENMARK Dansk Standardiseringsraad, Copenhagen.
FINLAND Suomen Standardisoimislütto, r.y., Helsinki.
FRANCE Association Française de Normalisation, Paris (La Défense).
GERMANY Deutsches Institut fur Normung, Berlin and Cologne.
ITALY Ente Nazionale Italiano di Unificazione, Milan.
NETHERLANDS Nederlands Normalisatie-Institut, Rijswijk (ZH).
NORWAY Norges Standardiseringsforbund, Oslo.
SWEDEN Sveriges Standardiseringskommission, Stockholm.
SWITZERLAND Association Suisse de Normalisation, Zurich.

BS9000 – QUALIFICATION FEATURES

Lot-by-lot tests.

Group A Those tests which cover on a lot-by-lot basis the non-destructive requirements of the electrical, mechanical and physical characteristics of a component.

Group B Those tests which cover on a lot-by-lot basis the inspection requirements for mechanical inter-changeability of a part and its ability to withstand environmental stresses and endurance tests.

Periodic tests

Group C Those tests which covered the inspection requirements for electrical, mechanical and endurance characteristics which are carried out at regular intervals of 3 months.

Group D As group C except specified intervals are one year.

BS9000 – QUALIFICATION PROCEDURE TO BS9400

- Raise detail specification in accordance with appropriate rules document.
- Detail specification approved by BSI and EQD*.
- Submit three separate lots for qualification.
- Pass all group A and B tests on each of the three lots.
- Pass all group C test on a combined sample from the three lots.
- Pass all group C tests except C5 endurance.
- Pass C5 endurance at 1,000 hours, submit test records countersigned by supervising inspector, and apply for provisional approval.
- Complete and pass C5 endurance at 2,000 hours, submit countersigned test records, apply for confirmation of qualification approval.
- Complete group D tests.

* Electrical Quality Assurance Directorate. (EQD act as NSI)

EQUIVALENCE OF ENVIRONMENTAL TEST METHODS

Integrated circuits	Sample or 100% screening		
	Method		
Test	BS9400	IEC68 & BS2011	MIL STD833
Precap visual	1.2.10 A or B		2010 A or B
High temperature storage	As BS2011	Ba	1008
Rapid change in temp. (air)	1.2.6.13	Na	1010
Rapid change in temp. (liquid)	As BS2011	Nc	1011
Humidity (Cycled)	As BS2011	Da, Db	
Humidity (Cycled)			1004
Humidity (Constant)	As BS2011	Ca	
Acceleration	As BS2011	Ga	2001
Hermeticity (fine)	As BS2011	Qk	1014A
Hermeticity (gross)	1.2.6.14.3	Fluorocarbon	1014C
Solderability	As BS2011		
Termination Robustness (DIL)	As BS2011 or 1.2.6.16.3	Ua, Ub	2004
Mechanical Shock	As BS2011	Ea	2002
Vibration (Swept frequency)	As BS2011	Fc/B4	2007
Salt Mist		Ka	
Salt Mist			1009
Operating Life Test	1.2.7.2		1005
Electrical Burn-in	1.2.9.2		1015

Notes:

Test methods listed on the same line are identical or essentially similar.

If a significant difference exists between the test methods they are placed on separate lines.

The BS9000 system calls up the BS9400 paragraph or the BS2011 test listed.

The draft CECC document call up the IEC68 test method which is identical to the BS2011 test having the same code letter.

The US Military system calls up the MIL STD883 test method.

BS9000 – PRODUCTS

CMOS products are available in the following application categories:

General application category

Components have electrical, mechanical, environmental and life performance to meet the majority of Military and professional requirements.

Special application category

Components to be used where reliability is important, maintenance difficult and downtime must be low.

Products are designated as follows:

Suffix	Category	Screening
S or Blank	General application category	Full assessment level
S1	Special application category	Level A
S2	Special application category	Level B
S3	Special application category	Level C
S4	Special application category	Level D

For more details of part number, prefix and suffix options please refer to the BS9000 ordering information in this section.

BS9000 – WHAT IS AVAILABLE?

Those devices indicated by a √ in the numerical index at the beginning of the data book, are being produced to BS9000 in both DIL and Flat-Pack.

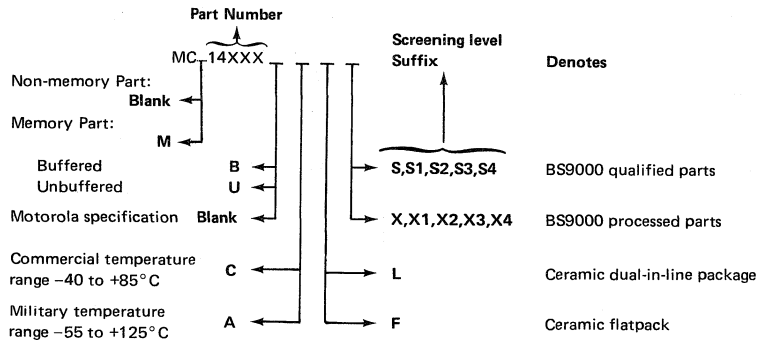
During the interim stage to full qualification, we complement the range of qualified parts by providing parts manufactured entirely at East Kilbride, these being designated by suffixes X, X1, X2, X3 and X4 in place of S, S1, S2, S3 and S4.

Motorola is continually adding to the number of BS9000 qualified parts that already exist and it is for this reason that the Motorola – BS9000 cross reference is available on request separately from Sales Offices.

ORDERING INFORMATION

A – BS9000 PRODUCT

For Motorola "F" specification parts

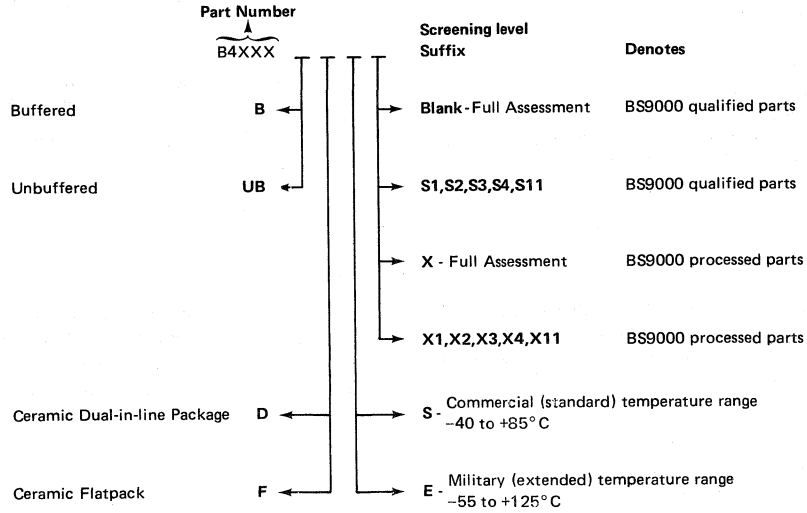


N.B. Combinations not permissible:

1. Qualified or processed parts to screening level S1 or X1 in the Commercial temperature range.
2. Qualified or processed parts to screening level S4 or X4 in both Military and Commercial Temperature range.

B – BS9000 PRODUCT

For Common "F" specification parts

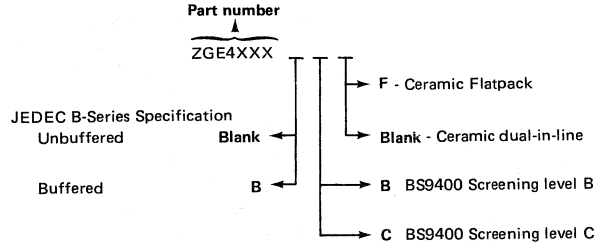


N.B. All combinations are permissible except the following:

1. Unbuffered gates as qualified parts.
2. Types 4007, 4049, and 4069 are not available in buffered versions so use UB suffix.
3. Qualified or processed parts to screening level S1 or X1 in the Commercial Temperature range.

C - OTHER HI-REL PRODUCT

In applications where the use of non UK diffused and assembled CMOS parts is permitted, customers can procure the following military temperature grade parts screened in accordance with BS9400 level B or level C.



Examples of ordering

1. A buffered DIL part (eg. MC14001BAL) screened in accordance with BS9400 level B.
   Order ZGE4001BB
2. An unbuffered DIL part (eg. MC14001UBAL) screened in accordance with BS9400 level C.
   Order ZGE4001C

D – OTHER SPECIFICATION

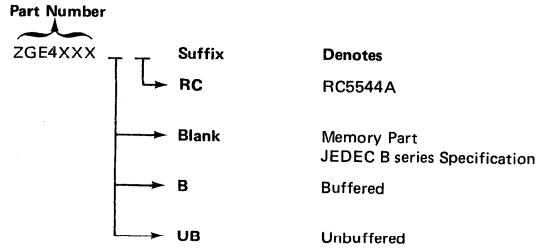
Customers requiring CMOS parts **approved** to the British Post Office Specification RC5544A can procure Ceramic DIL commercial temperature range parts by specifying the following:

Example of ordering

MC14502BAL to RC5544A

Order ZGE4502BRC

Please note that this feature will eventually be superceded when the BS9000 system adopts fully the screening procedures for application category S11.



E – SPECIAL REQUIREMENTS

Customers whose needs are not exactly met in any of the preceding standard specifications and who specifically require deviations are requested to contact their local Motorola Sales Office or Motorola Distributor to obtain further information.

Such deviations currently include:

- Customer pre-cap inspection visits.
- Serialising and the provision of test results for correlation purposes.
- Scanning electron microscope inspection of a wafer.
- X-ray examination.

BS9000

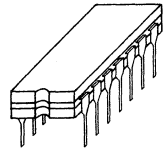
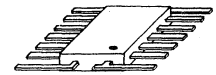
Explicit ordering information is printed in every BS9000 Detail Specification and therefore users should refer to the examples of the BS Specifications contained in this section to familiarise themselves with the procedures.

BS9000 – MOTOROLA "F" and COMMON "F" – a comparison

On the following pages are printed examples of both a MOTOROLA "F" specification and a COMMON "F" detail specification for BS9490 CMOS. In comparing them note that any differences between them exist entirely within the Quality Assurance provisions since all parts to either specification are manufactured using the same wafer/dice source and the same assembly procedures to the same standards. It follows that the parts are almost entirely interchangeable.

BS9000 – THE COMPARISON

1. MOTOROLA "F" specifications with regard to electrical parameters are:
   In subgroup A2 regarded as tighter than COMMON "F"
   In subgroup A3 regarded as equal to those in COMMON "F"
   In subgroup A4 regarded as looser than in COMMON "F"
2. COMMON "F" specifications with regard to electrical inspection tests in subgroups A4 and C4 are more comprehensive that MOTOROLA "F" i.e. There are more dynamic tests performed in A4 and output drive currents are tested at temperature extremes in C4.
3. CTR information is more comprehensive in COMMON "F" than in MOTOROLA "F" specifications.
4. AQLs throughout are identical in both MOTOROLA "F" and COMMON "F".
5. The screening requirements in subgroup A0 are the same except the category S4 screening level D is included in COMMON "F" specifications as a further option.
6. Mechanical and environmental tests are identical in both the screening and inspection procedures, however, regarding B1 dimension L is now 3.2 mm min. and 3.9 mm max.
7. Marking is different.
8. Ratings are similar.
9. With regard to B7, C5 and D4, note that electrical endurance in COMMON "F" is to be performed in a dynamic mode only.
10. Electrical inspection tests meet or exceed JEDEC B electrical requirements. There are a few exceptions and these are the 000, 007, 049 and 069 which should really be referred to as UB parts. Motorola has no plans to introduce a buffered 049 to the JEDEC B specification.
11. Unbuffered gates qualified to BS9000 are available to the MOTOROLA "F" specification.

MOTOROLA LTD. COLVILLES RD, KELVIN ESTATE, EAST KILBRIDE, GLASGOW, G75 0TG.	BS9490 F057-F058 F1267-F1278 ISSUE 1 NOV 1977
ELECTRONIC COMPONENTS OF ASSESSED QUALITY: DETAIL SPECIFICATION	
For detail dimensions see BS3934 S087B BS3934 S093A   BAL/BCL Dual-in-line BAF/BCF Flatpack	SILICON MONOLITHIC INTEGRATED CIRCUIT FULL ASSESSMENT LEVEL AND OPTIONAL APPLICATION CATEGORIES S1, S2 AND S3 Manufacturer's type number MC14006 BAL MC14006 BAF MC14006 BCL MC14006 BCF 18-BIT STATIC SHIFT REGISTER Dual-in-line and Flatpack, Ceramic/glass hermetically sealed encapsulation

1. LIMITING CONDITIONS OF USE (not for inspection purposes)

1.1 Absolute values

Voltages referenced to Pin 7

V_{DD}	Maximum continuous positive supply voltage		+ 18 V
V_{DD}	Maximum continuous negative supply voltage		- 0.5 V
V_{in}	Maximum continuous positive input voltage		V_{DD}
V_{in}	Maximum continuous negative input voltage		- 0.5 V
I_{in}	Maximum continuous input current		10 mA
T_{amb}	Ambient operating temperature range	BAL/BAF version BCL/BCF version	$-55^{o}C$ to $125^{o}C$ $-40^{o}C$ to $85^{o}C$
T_{stg}	Storage temperature range		$-65^{o}C$ to $150^{o}C$
	Shock (t = 0.5 ms)		14700 m/s^2
	Vibration (f = 150 - 2000 Hz)		196 m/s^2

EXAMPLE

1.2 Recommended handling precautions

1.2.1 Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.

1.2.2 Use grounded tip soldering irons.

1.2.3 Ground all test equipment.

1.2.4 Connect all unused device inputs to V_{DD} or V_{SS}.

1.2.5 PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.

1.2.6 Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.

1.2.7 Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.

1.2.8 When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.

1.2.9 Switch off power supply before inserting or removing devices from circuits.

1.2.10 Disconnect all low impedance equipment from device inputs before d.c. power supplies are switched off.

FIGURE 1

BLOCK DIAGRAM

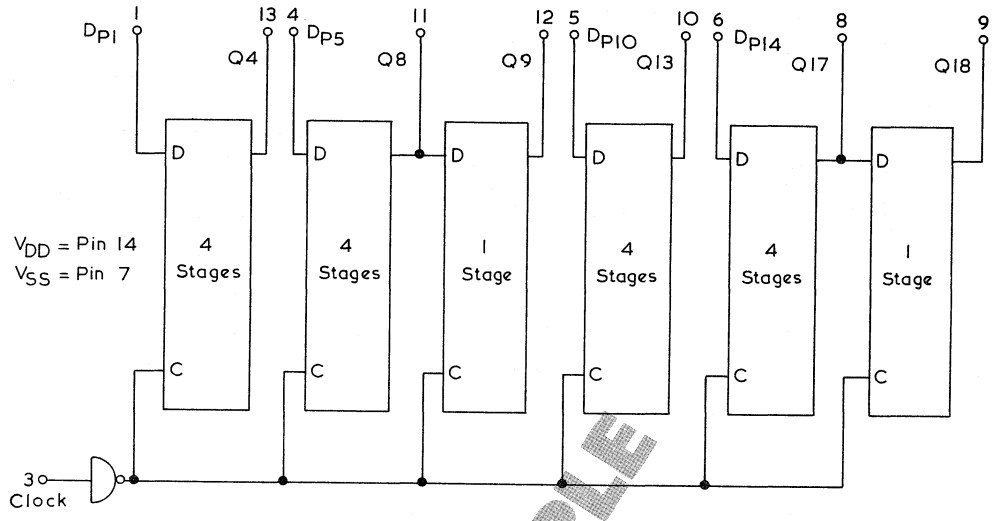
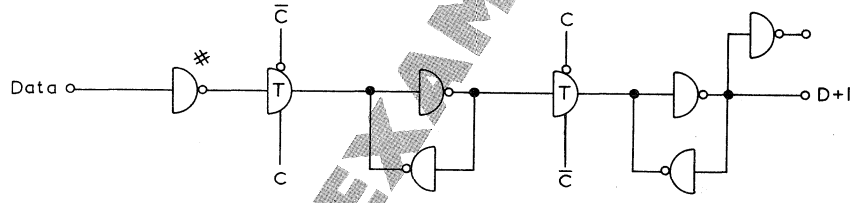
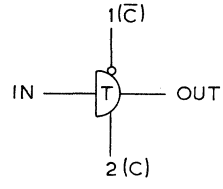


FIGURE 2

LOGIC DIAGRAM (One Register Stage)



※ Inverter used only on the first stage of each four stage element.



Input to output is

(A) A bidirectional low impedance when control input 1 is "low" and control input 2 is "high".

(B) An open circuit when control input 1 is "high" and control input 2 is "low."

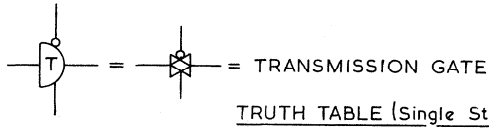


TABLE 1

TRUTH TABLE (Single Stage)

D_n	C	Q_{n+1}
0	↓	0
1	↓	1
X	↑	Q_n

X = Don't Care

EXAMPLE

2. RECOMMENDED CONDITIONS OF USE AND ASSOCIATED CHARACTERISTICS

Not for inspection purposes except as prescribed in Clause 6.

All values for BAL/BAF version : $T_{low} = -55^{o}C$, $T_{high} = 125^{o}C$

and BCL/BCF version : $T_{low} = -40^{o}C$, $T_{high} = 85^{o}C$

V_{DD} continuous power supply voltage 5.0 V to 15.0 V

		V_{DD}	T_{low}	25°C	T_{high}	Units
V_{OL}	Low state output voltage V_{IL} = 0 V, $V_{IH} = V_{DD}$, R_L > 10 MΩ	5 10 15	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	V max. V max. V max.
V_{OH}	High state output voltage	5 10 15	4.95 9.95 14.95	4.95 9.95 14.95	4.95 9.95 14.95	V min. V min. V min.
V_{IL}	Low state input voltage V_{OL} = 0.5 V, V_{OH} = 4.5 V V_{OL} = 1.0 V, V_{OH} = 9.0 V V_{OL} = 1.5 V, V_{OH} = 13.5 V	5 10 15	1.50 3.00 4.00	1.50 3.00 4.00	1.50 3.00 4.00	V max. V max. V max.
V_{IH}	High state input voltage V_{OL} = 0.5 V, V_{OH} = 4.5 V V_{OL} = 1.0 V, V_{OH} = 9.0 V V_{OL} = 1.5 V, V_{OH} = 13.5 V	5 10 15	3.50 7.00 11.00	3.50 7.00 11.00	3.50 7.00 11.00	V min. V min. V min.
$-I_{OH}$	Output drive source current BAL/BAF version V_{OH} = 2.5 V V_{OH} = 9.5 V V_{OH} = 13.5 V	5 10 15	1.20 0.62 1.80	1.00 0.50 1.50	0.70 0.35 1.10	mA min. mA min. mA min.
I_{OL}	Output drive sink current BAL/BAF version V_{OL} = 0.4 V V_{OL} = 0.5 V V_{OL} = 1.5 V	5 10 15	0.64 1.60 4.20	0.51 1.30 3.40	0.36 0.90 2.40	mA min. mA min. mA min.
$-I_{OH}$	Output drive source current BCL/BCF version V_{OH} = 2.5 V V_{OH} = 9.5 V V_{OH} = 13.5 V	5 10 15	1.00 0.50 1.40	0.80 0.40 1.20	0.60 0.30 1.00	mA min. mA min. mA min.
I_{OL}	Output drive sink current BCL/BCF version V_{OL} = 0.4 V V_{OL} = 0.5 V V_{OL} = 1.5 V	5 10 15	0.52 1.30 3.60	0.44 1.10 3.00	0.36 0.90 2.40	mA min. mA min. mA min.
I_{DD}	Supply current BAL/BAF version	5 10 15	5.00 10.00 20.00	5.00 10.00 20.00	150.00 300.00 600.00	µA max. µA max. µA max.
I_{DD}	Supply current BCL/BCF version	5 10 15	20.00 40.00 80.00	20.00 40.00 80.00	150.00 300.00 600.00	µA max. µA max. µA max.
I_{IN}	Input current for all permitted values of V_{IN} BAL/BAF version	15	-	0.10	-	µA
I_{IN}	Input current for all permitted values of V_{IN} BCL/BCF version	15	-	0.30	-	µA

EXAMPLE

2. RECOMMENDED CONDITIONS OF USE AND ASSOCIATED CHARACTERISTICS (Contd.)

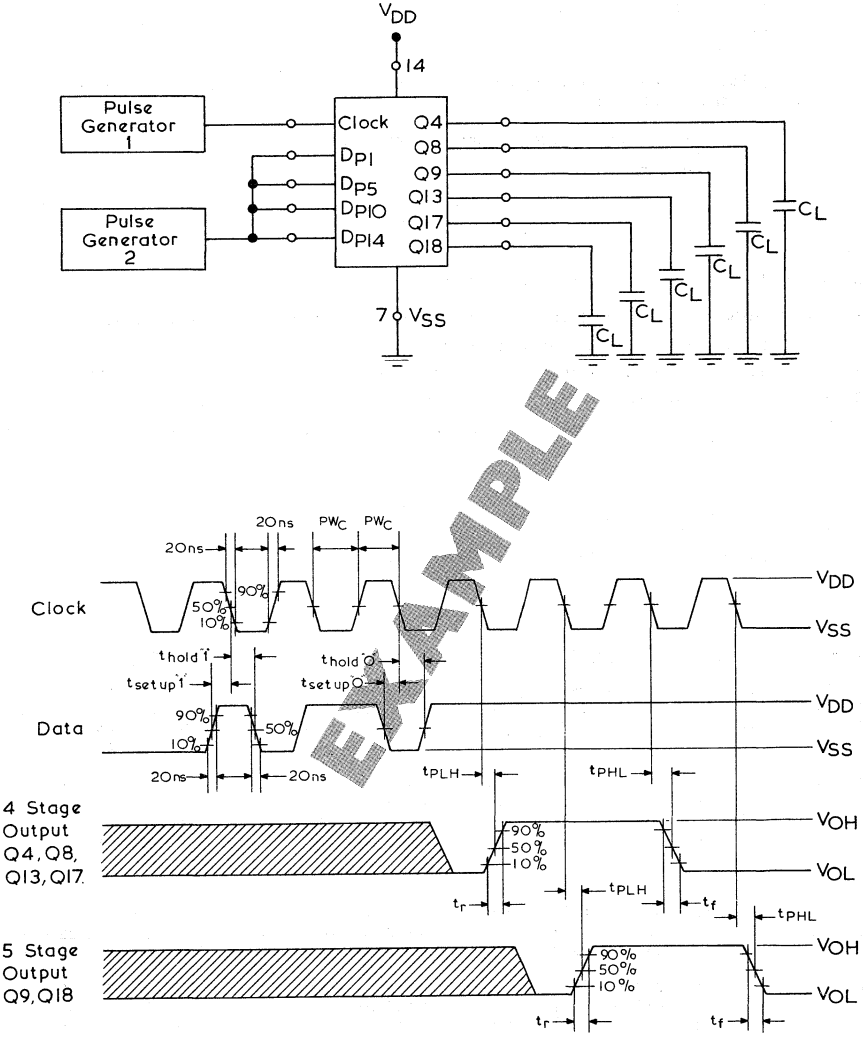
Switching Characteristics (C_L = 50 pF, T_{Amb} = 25°C)

		V_{DD}	BAL/BAF version	BCL/BCF version	Units
t_r	Output rise time	5	350	400	ns max.
		10	150	200	ns max.
		15	110	160	ns max.
t_f	Output fall time	5	175	200	ns max.
		10	75	100	ns max.
		15	55	80	ns max.
t_{PLH}, t_{PHL}	Propagation delay time	5	460	600	ns max.
		10	165	275	ns max.
		15	120	200	ns max.
t_{hold}	Hold time	5	180	220	ns max.
		10	90	110	ns max.
		15	75	90	ns max.
t_{setup}	Setup time	5	-15	0	ns max.
		10	-5	0	ns max.
		15	-3	0	ns max.
PW_C	Minimum clock pulse width	5	200	250	ns max.
		10	70	125	ns max.
		15	55	95	ns max.
PRF	Maximum clock pulse frequency	5	2.5	2.0	MHz min.
		10	7.0	4.0	MHz min.
		15	10.0	6.0	MHz min.
t_r, t_f	Maximum clock pulse rise and fall time	5	15	15	µs min.
		10	15	15	µs min.
		15	15	15	µs min.

EXAMPLE

FIGURE 3

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



EXAMPLE

Output state can change since data previously clocked in might be in either state.

Note: 10% and 90% values refer to V_{IL} and V_{IH}.

3. MARKING

(1) Each integrated circuit shall bear the following marking

a. Manufacturer's type number (See Table 2).

b. Factory identification code.

c. Date code.

(2) Each primary package containing one or more of these circuits shall bear all the above markings and in addition

d. The British Standard detail specification number.

e. M.O.S. warning label.

4. RELATED DOCUMENTS

This specification shall be read in conjunction with:-

BS 2011 Methods for the environmental testing of electronic components and electronic equipment.

BS 3934 Dimensions of semiconductor devices.

BS 6001 Sampling procedures and tables for inspection by attributes.

BS 9000 General requirements for electronic parts of assessed quality.

BS 9400 Specification for integrated electronic circuits of assessed quality, generic data and methods of test.

EXAMPLE

5. ORDERING INFORMATION

Orders for these integrated circuits shall contain the following information:-

TABLE 2

Order Type		BS Number				Marking
MC14006 BAL S	to	BS9490 F057	Issue 1	dated	Nov 1977	MC14006 BAL BS
MC14006 BAL S1	to	BS9490 F1269	Issue 1	dated	Nov 1977	MC14006 BAL BS - S1
MC14006 BAL S2	to	BS9490 F1270	Issue 1	dated	Nov 1977	MC14006 BAL BS - S2
MC14006 BAL S3	to	BS9490 F1271	Issue 1	dated	Nov 1977	MC14006 BAL BS - S3
MC14006 BAF S	to	BS9490 F1267	Issue 1	dated	Nov 1977	MC14006 BAF BS
MC14006 BAF S1	to	BS9490 F1274	Issue 1	dated	Nov 1977	MC14006 BAF BS - S1
MC14006 BAF S2	to	BS9490 F1275	Issue 1	dated	Nov 1977	MC14006 BAF BS - S2
MC14006 BAF S3	to	BS9490 F1276	Issue 1	dated	Nov 1977	MC14006 BAF BS - S3
MC14006 BCL S	to	BS9490 F058	Issue 1	dated	Nov 1977	MC14006 BCL BS
MC14006 BCL S2	to	BS9490 F1272	Issue 1	dated	Nov 1977	MC14006 BCL BS - S2
MC14006 BCL S3	to	BS9490 F1273	Issue 1	dated	Nov 1977	MC14006 BCL BS - S3
MC14006 BCF S	to	BS9490 F1268	Issue 1	dated	Nov 1977	MC14006 BCF BS
MC14006 BCF S2	to	BS9490 F1277	Issue 1	dated	Nov 1977	MC14006 BCF BS - S2
MC14006 BCF S3	to	BS9490 F1278	Issue 1	dated	Nov 1977	MC14006 BCF BS - S3

Note: Order Type S means full assessment level parts.

Order Type S1 means screened parts to the appropriate level on Page 7.

Order Type S2 means screened parts to the appropriate level on Page 7.

Order Type S3 means screened parts to the appropriate level on Page 7.

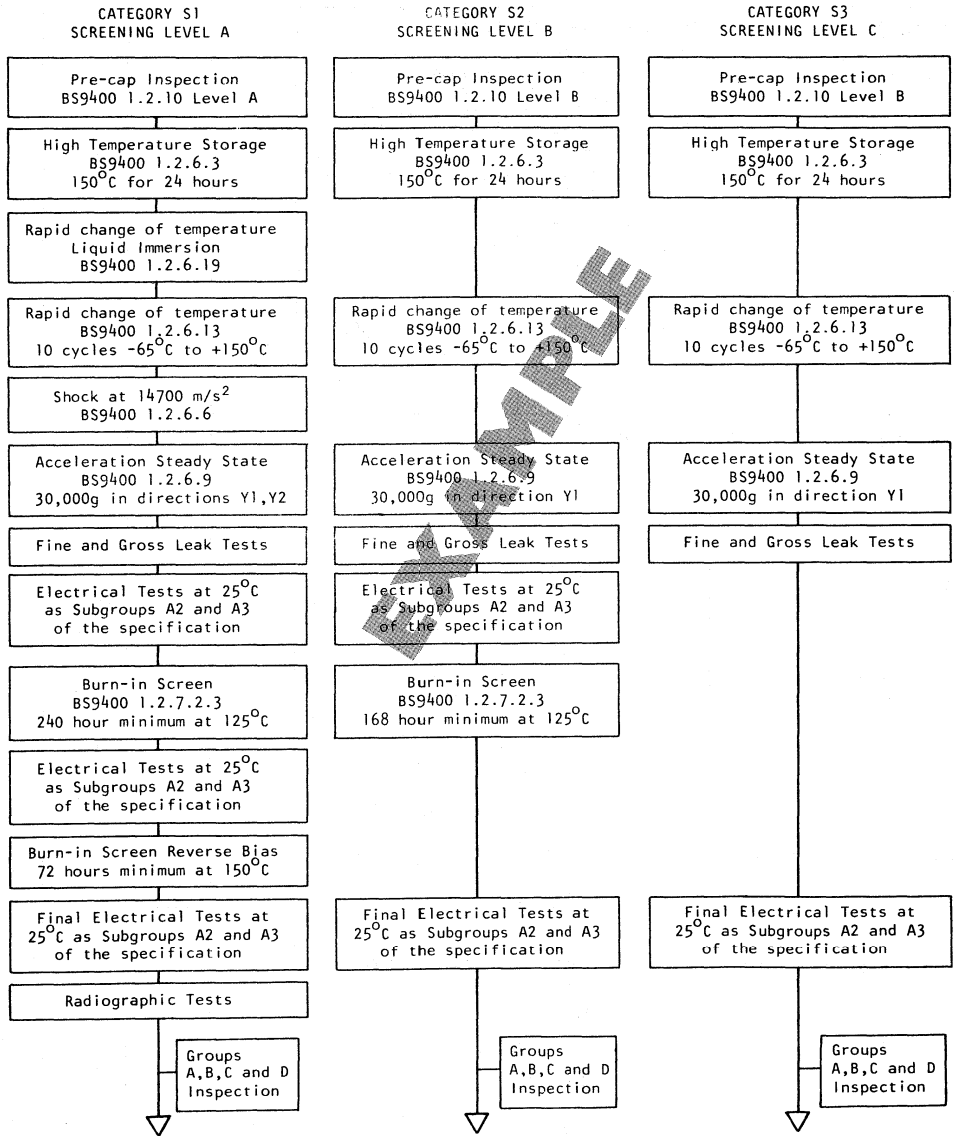
6. INSPECTION REQUIREMENTS

All tests to be conducted at T_{amb} = 25°C.

Samples submitted to tests marked 'D' shall not be accepted for release under BS 9000 (see clause 2.6.5 of BS 9000, Part 1).

Subgroup A0 is not applicable for Full Assessment Level.

100% SCREENING LEVELS



Note 1. Radiographic Tests. Each device shall be examined, for extraneous matter and assembly defects, in the X and Y directions.

Note 2. Burn-In. If during electrical tests after Burn-In (Categories S1 and S2) more than 10% defectives are found the lot will be rejected.

Inspection	BS 9400 reference and conditions of test	Symbol	Limits Min.	Limits Max.	Unit
Group A Subgroup A0	Subgroup A5 not applicable. See Page 7, for screening levels where applicable.				
Subgroup A1 Visual inspection	Inspection level I, AQL 1.5% 1.2.2 None.				
Subgroup A2 Verification of type of integrated circuit	Inspection level II, AQL 0.15% 1001 Perform functional truth table (Table 1) for each stage in the package in turn, in each functional mode, using the following definitions of high and low. Unused inputs not being tested to be connected to 0 V. $V_{IH} = V_{DD}$ $R_L \geq 10$ MΩ $V_{IL} = 0$ V				
	V_{DD} | V_{OH} min. | V_{OL} max. 3 | 2.10 | 0.90 18 | 12.60 | 5.40				
Subgroup A3 Supply current	Inspection level II, AQL 1.5% 2011 Test for each state in Table 1. $V_{IH} = 15$ V $V_{IL} = 0$ V $V_{DD} = 15$ V				
	BAL/BAF version	I_{DD}	-	20.00	µA
	BCL/BCF version	I_{DD}	-	80.00	µA
Low state output voltage	2001 Each output tested in turn. All inputs connected to $V_{IL} = 0$ V				
	$V_{DD} = 5$ V $V_{IN} = 5$ V	V_{OL}	-	0.05	V
	$V_{DD} = 10$ V $V_{IN} = 10$ V	V_{OL}	-	0.05	V
	$V_{DD} = 15$ V $V_{IN} = 15$ V	V_{OL}	-	0.05	V
High state output voltage	2002 $V_{DD} = 5$ V $V_{IN} = 0$ V	V_{OH}	4.95	-	V
	$V_{DD} = 10$ V $V_{IN} = 0$ V	V_{OH}	9.95	-	V
	$V_{DD} = 15$ V $V_{IN} = 0$ V	V_{OH}	14.95	-	V
Low and high state input currents	2013 Each input tested in turn, other inputs at 0 V $V_{DD} = 15$ V				
	$V_{IN} = 0$ V BAL/BAF version	$-I_{IL}$	-	0.10	µA
	$V_{IN} = 15$ V BAL/BAF version	I_{IH}	-	0.10	µA
	$V_{IN} = 0$ V BCL/BCF version	$-I_{IL}$	-	0.30	µA
	$V_{IN} = 15$ V BCL/BCF version	I_{IH}	-	0.30	µA

EXAMPLE

Inspection	BS 9400 reference and conditions of test.		Symbol	Limits Min.	Limits Max.	Unit
Subgroup A3 (Contd.)						
Output drive source current	2018	Apply input conditions to give a high output state. All inputs connected to $V_{IH} = V_{DD}$				
		V_{DD} = 5 V V_{OH} = 2.5 V				
		BAL/BAF version	$-I_{OH}$	1.00	-	mA
		BCL/BCF version	$-I_{OH}$	0.80	-	mA
		V_{DD} = 10 V V_{OH} = 9.5 V				
		BAL/BAF version	$-I_{OH}$	0.50	-	mA
		BCL/BCF version	$-I_{OH}$	0.40	-	mA
		V_{DD} = 15 V V_{OH} = 13.5 V				
		BAL/BAF version	$-I_{OH}$	1.50	-	mA
		BCL/BCF version	$-I_{OH}$	1.20	-	mA
Output drive sink current	2018	Apply input conditions to give a low output state. All inputs connected to V_{IL} = 0 V				
		V_{DD} = 5 V V_{OL} = 0.4 V				
		BAL/BAF version	I_{OL}	0.51	-	mA
		BCL/BCF version	I_{OL}	0.44	-	mA
		V_{DD} = 10 V V_{OL} = 0.5 V				
		BAL/BAF version	I_{OL}	1.30	-	mA
		BCL/BCF version	I_{OL}	1.10	-	mA
		V_{DD} = 15 V V_{OL} = 1.5 V				
		BAL/BAF version	I_{OL}	3.40	-	mA
		BCL/BCF version	I_{OL}	3.00	-	mA
Verification of integrated circuit function under worst case conditions	1001	Perform functional truth table (Table 1) for each stage in turn, in each functional mode, using the following definitions of high and low and V_{DD}.				

V_{DD}	V_{IH}	V_{IL}	V_{OH} min.	V_{OL} max.
5	3.50	1.50	4.50	0.50
10	7.00	3.00	9.00	1.00
15	11.00	4.00	13.50	1.50

$R_L \geq 10$ MΩ

Inputs not being tested connected to V_{DD} or V_{SS}

EXAMPLE

Inspection	BS 9400 reference and conditions of test.	Symbol	Limits		Unit
			Min.	Max.	
Subgroup A4	Inspection level S-4, AQL 4.0%				
High to low output state propagation delay time	2008 See Figure 3. t_r = 20 ns (10% to 90%) t_f = 20 ns (10% to 90%) C_L = 50 pF f = 500 kHz 50% duty cycle R_L > 1 MΩ				
	V_{DD} = 5 V BAL/BAF version	t_{PHL}	-	460	ns
	BCL/BCF version	t_{PHL}	-	600	ns
	V_{DD} = 10 V BAL/BAF version	t_{PHL}	-	165	ns
	BCL/BCF version	t_{PHL}	-	275	ns
	V_{DD} = 15 V BAL/BAF version	t_{PHL}	-	120	ns
	BCL/BCF version	t_{PHL}	-	200	ns
Low to high output state propagation delay time	2008 Tests, test conditions and limits as for high to low propagation delay time.	t_{PLH}			

EXAMPLE

Inspection	BS 9400 reference and conditions of test.	Symbol	Limits Min.	Limits Max.	Unit
Group B	Subgroups B4 and B5 not applicable.				
Subgroup B1 Dimensions	Inspection level S-2, AQL 6.5% 1.2.3 To BS 3934 SO-87B	A D	- -	5.10 20.32	mm mm
	BS 3934 SO-93A	A H_E n	- 18.30 14	2.27 19.60 14	mm mm
Subgroup B2(a) '(D)' Solderability	Inspection level S-4, AQL 4.0% 1.2.6.15.1 See Note 2.				
Subgroup B2(b) Rapid change of temperature followed by Fine leak Gross leak	Inspection level S-4, AQL 4.0% 1.2.6.13 T_{amb} = -65°C to 150°C Transfer time 5 min. max. 1.2.6.14.1 1.2.6.14.3				
Subgroup B3 '(D)' Terminal robustness, bending	Inspection level S-3, AQL 6.5% 1.2.6.16.3				
Subgroup B6 Acceleration, steady state	Inspection level S-4, AQL 4.0% 1.2.6.9 Non-operating. Direction of acceleration = Y2 Acceleration = 196,000 m/s^2				
Subgroup B7 Electrical endurance	Inspection level S-4, AQL 1.5% 1.2.7.1 (See Figure 4) For type BAL/BAF T_{amb} = 125°C For type BCL/BCF T_{amb} = 85°C V_{DD} = 10 V Duration 160 h. min.				
Post-Test End-Points for Subgroups B2(b), B6 and B7 Verification of type of integrated circuit	1001 Requirements as for Subgroup A2				
Low state output voltage High state output voltage Low state input current High state input current	2001 2002 2013 2013 Conditions and limits as for Subgroup A3	V_{OL} V_{OH} $-I_{IL}$ I_{IH}			
Subgroup B8 CTR information	1.1.11 Attributes information for Subgroups B2(a), B2(b), B3, B6 and B7.				

EXAMPLE

Inspection	BS 9400 reference and conditions of test.	Symbol	Limits Min.	Limits Max.	Unit
Group C	Subgroup C2 not applicable.				
Subgroup C1	Inspection level S-2, AQL 6.5%				
Dimensions	1.2.3 To BS 3934 SO-87B	A_1	0.51	-	mm
		b	0.38	0.59	mm
		c	0.20	0.36	mm
		L	3.10	4.50	mm
	BS 3934 SO-93A	b	0.25	0.54	mm
		e	1.27 TP	-	
		L_E	5.40	-	mm
		Z^E	-	0.63	mm
Subgroup C3	Inspection level S-2, AQL 6.5%				
Vibration, swept frequency	1.2.6.8.1 Non-operating. Frequency range 150 Hz to 2000 Hz. Acceleration = 196 m/s^2				
followed by					
Shock	1.2.6.6 Non-operating. Peak acceleration 14,700 m/s^2. Duration 0.5 ms. The body shall be clamped and three successive shocks shall be applied in each of directions of Y_1, Y_2 and X_1				
and					
Damp heat cyclic	1.2.6.5 Non-operating. 28 cycles				
Subgroup C4(a)	Inspection level S-4, AQL 4.0%				
	For type BAL/BAF T_{amb} = 125°C				
	For type BCL/BCF T_{amb} = 85°C				
Low state output voltage	2001 Each output tested in turn. All inputs connected to V_{IL} = 0 V				
	V_{DD} = 5 V	V_{OL}	-	0.05	V
	V_{DD} = 10 V	V_{OL}	-	0.05	V
	V_{DD} = 15 V	V_{OL}	-	0.05	V
High state output voltage	2002 V_{DD} = 5 V	V_{OH}	4.95	-	V
	V_{DD} = 10 V	V_{OH}	9.95	-	V
	V_{DD} = 15 V	V_{OH}	14.95	-	V

EXAMPLE

Inspection	BS 9400 reference and conditions of test.		Symbol	Limits		Unit
				Min.	Max.	
Subgroup C4(b)	Inspection level S-4, AQL 4.0%					
		For type BAL/BAF T_{amb} = -55°C				
		For type BCL/BCF T_{amb} = -40°C				
Low state output voltage	2001	Each output tested in turn. All inputs connected to V_{IL} = 0 V				
		V_{DD} = 5 V	V_{OL}	-	0.05	V
		V_{DD} = 10 V	V_{OL}	-	0.05	V
		V_{DD} = 15 V	V_{OL}	-	0.05	V
High state output voltage	2002	V_{DD} = 5 V	V_{OH}	4.95	-	V
		V_{DD} = 10 V	V_{OH}	9.95	-	V
		V_{DD} = 15 V	V_{OH}	14.95	-	V
Subgroup C5	Inspection level S-3, AQL 4.0%					
Electrical endurance	1.2.7.1	Test conditions and limits as for Subgroup B7. Duration 2000 h. min.				
Post-Test End-Points for Subgroups C3 and C5		Tests, test conditions and limits as for Post-Test End-Points in Group B, additionally corrosion check as 1.2.6.5				
Subgroup C6						
CTR information	1.1.11	Attributes information for Subgroups C3 and C5. Measurements information for each test, except the verification test before and after conditioning, in Subgroup C5.				

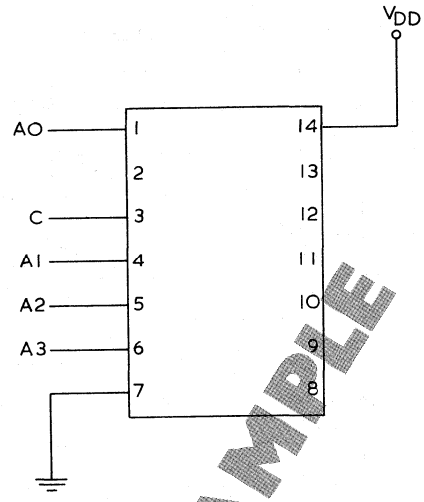
EXAMPLE

BS 9490 F 057 - F 058 F1267 - F1278 ISSUE 1 NOV 1977					
Inspection	BS 9400 reference and conditions of test.	Symbol	Limits		Unit
			Min.	Max.	
Group D (See Note 1)	Subgroups D2 and D3 not applicable.				
Subgroup D1 Dimensions	Inspection level S-2 1.2.3 To BS 3934 SO-87B BS 3934 SO-93A All dimensions not checked in subgroups B1 and C1				
Subgroup D4 Electrical endurance	Inspection level S-3 1.2.7.1 Test conditions and limits as for Subgroup B7. Duration 8000 h. min.				
Post-Test End-Points for Subgroup D4	Tests, test conditions and limits as for Post-Test End-Points in Group B.				
Subgroup D5 CTR information	1.1.11 Attributes information for Subgroups D1 and D4. Measurements information for each test, except the verification test before and after the conditioning in Subgroup D4.				
Note 1 Note 2	See paragraph 1.1.10 of BS 9400. When method 1.2.6.15(1) is used the inspection level is reduced to S3.				

EXAMPLE

ELECTRICAL ENDURANCE TEST CIRCUIT FOR SUBGROUPS B7, C5 AND D4

FIGURE 4



EXAMPLE

7. ADDITIONAL INFORMATION

7.1 Total supply current

Total supply current, Dynamic plus Quiescent, per package C_L = 50 pF on all outputs, all buffers switching.

V_{DD} = 5 V	I_T	=	(1.30	x	f)	+	I_{DD}	µA
V_{DD} = 10 V	I_T	=	(2.60	x	f)	+	I_{DD}	µA
V_{DD} = 15 V	I_T	=	(3.90	x	f)	+	I_{DD}	µA

Note: f is the frequency in kHz.
I_{DD} is the static current in µA.

7.2 Input current

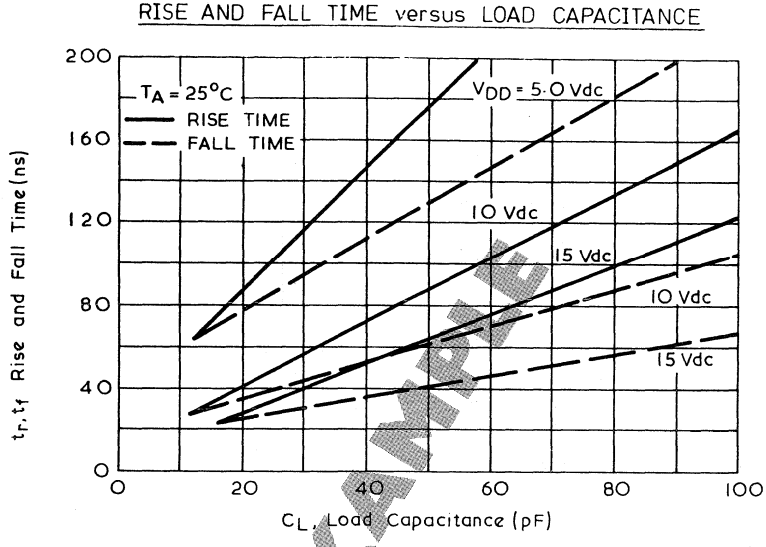
The main contribution to the input current is that due to the diode protection circuit and is typically 10 pA at 25°C.

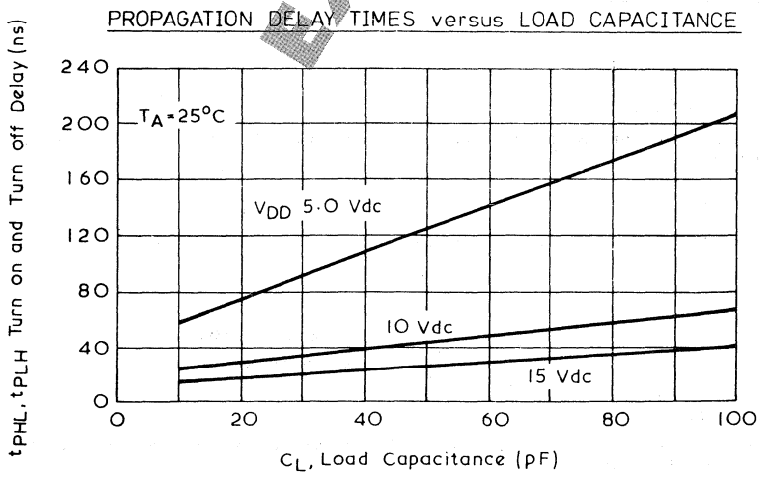
7.3 Loading rules

Due to the very low input current requirements for CMOS there is practically no d.c. fanout factor limitation when driving other CMOS inputs.

The actual fanout of the CMOS device is limited by a capacitive load consideration based on the desired system operating frequency.

The effects of capacitive load on the dynamic characteristics are shown below.



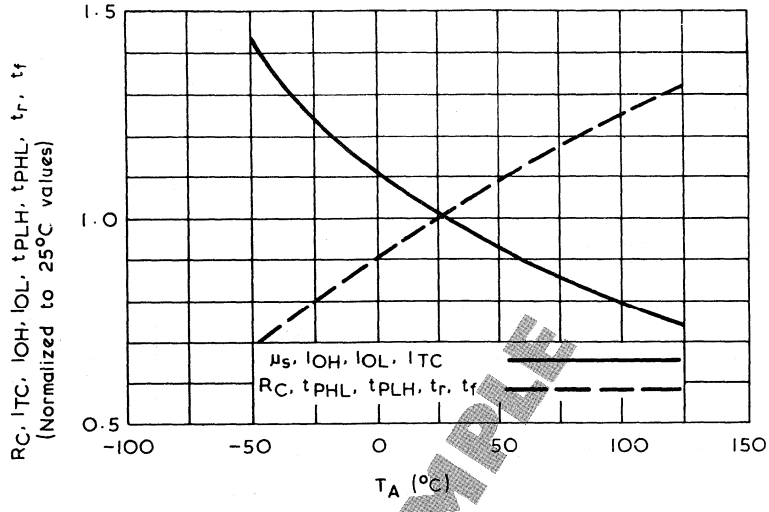


EXAMPLE

The capacitive load consists of the input capacitance of each input connected to the output (typically 5 pF/input) plus capacitance of all lines connected to the output.

7.4 Variation of switching parameters with temperature

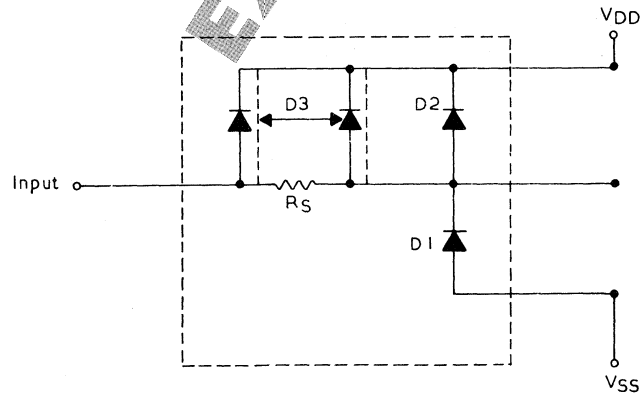
A normalised plot showing variations of t_{PLH}, t_{PHL}, t_r, t_f with temperature is shown below.



EXAMPLE

7.5 Input protection

All CMOS circuits have built-in protection circuitry on all inputs to prevent damage to the MOS input gates of the device.



Added Protection Circuitry At Each External Input Lead

R_S 1·5KΩ Nominal

Avalanche Voltages

BVD1 = 30V

BVD2 = 30V

BVD3 = 80V

7.6 Noise immunity

The noise immunity V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal '1' or '0' input level before producing an output state change. The noise immunity is specified for worst case voltage level.

7.7 Unused inputs

The unused inputs should be connected to either V_{DD} or V_{SS}.

7.8 Capacitive loading

The effect of capacitive loads on the output typically affects the dynamic characteristics as indicated by the equations below.

	V_{DD} = 5.0 V	V_{DD} = 10.0 V	V_{DD} = 15.0 V
t_r	3.00 C_L + 30 ns	1.50 C_L + 15 ns	1.10 C_L + 10 ns
t_f	1.50 C_L + 25 ns	0.75 C_L + 12.5 ns	0.55 C_L + 9.5 ns
t_{PLH}, t_{PHL}	1.70 C_L + 220 ns	0.66 C_L + 77 ns	0.50 C_L + 55 ns

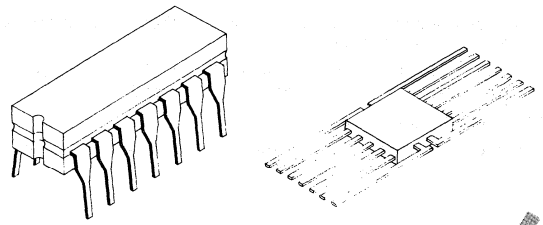
EXAMPLE

7.9 Input capacitance

The input capacitance (V_{in} = 0 V) is 5 pF typical.

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BRITISH STANDARDS INSTITUTION 2, PARK STREET, LONDON, W1A 2BS	BS9490 F2810 to F2818 F2820 to F2828
Specification available from: — AS SHOWN IN PD 9002	ISSUE **DRAFT B** *Page 1 of 21 pages*
ELECTRONIC COMPONENTS OF ASSESSED QUALITY **DETAIL SPECIFICATION IN ACCORDANCE WITH** **BS9400:1970**	MANUFACTURER'S TYPE NUMBER B4006 B See PD9002 For ordering information see clause 5
Outline NOT TO SCALE — Isometric projection  BDE/BDS Dual-in-line — BFE/BFS Flatpack	18 bit static shift register
	Silicon monolithic Integrated circuit — CMOS Dual-in-line and flatpack Ceramic/Glass hermetically Sealed encapsulation
For detail dimensions see BS3934 SO-87 Marking information see clause 3	Full assessment level and optional application categories S1, S2, S3 and S4

EXAMPLE

1. **LIMITING CONDITIONS OF USE** (not for inspection purposes)

1.1 **Absolute values**

Voltages references to V_{SS}

V_{DD}	Maximum continuous supply voltage	+18 V
V_{IN}	Maximum continuous input voltage	V_{DD}
I_{IN}	Maximum continuous input current	±10 mA
V_{DD}	Maximum continuous negative supply voltage	− 0.3 V
T_{amb}	Ambient operating temperature range E version	− 55°C to 125°C
T_{amb}	Ambient operating temperature range S version	− 40°C to 85°C
T_{stg}	Storage temperature range	− 65°C to 150°C
	Shock (t = 0.5 ms)	14 700 m/s²
	Vibration (f = 150 - 2000 Hz)	196 m/s²
	Acceleration	296 000 m/s²

Refer to Qualified Products List PD9002 for details of manufacturers approved to this specification

1.2 **Recommended handling precautions**

1.2.1 Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.

1.2.2 Use grounded tip soldering irons.

1.2.3 Ground all test equipment.

1.2.4 Connect all unused device inputs to V_{DD} or V_{SS}.

1.2.5 PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.

1.2.6 Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.

1.2.7 Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.

1.2.8 When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, ''Dummy connectors'' should be used to electrically short all PC board terminals together.

1.2.9 Switch off power supply before inserting or removing devices from circuits.

1.2.10 Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.

EXAMPLE

PIN CONNECTION DIAGRAM

(Pin connections viewed from above for both dual-in-line and flatpack)

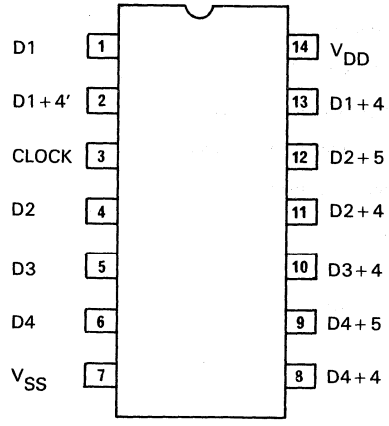
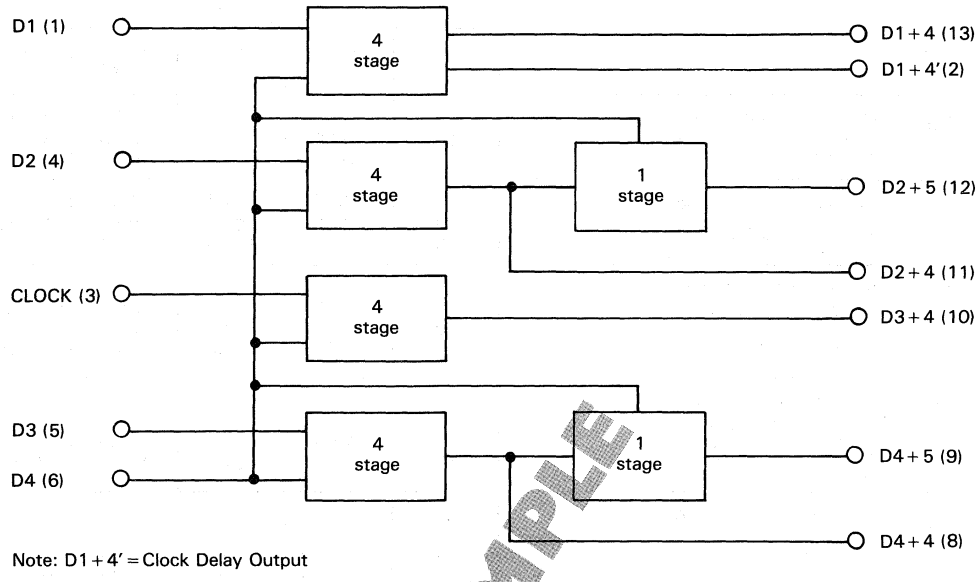


Figure 1

		BS9490 F2810 to F2818 F2820 F2828

FUNCTION BLOCK DIAGRAM



Note: D1 + 4' = Clock Delay Output

Figure 2

EXAMPLE

FUNCTION THRUTH TABLE

Table 1

Thruth table for output from terminal 2		
D1+4	CL*	D1+4'
L	⌒	L
H	⌒	H
X	⌣	NC

H = High Level
L = Low Level
X = Don't Care
NC = No Change
* = Level Change

Thruth table for shift register stage		
D	CL*	D+1
L	⌣	L
H	⌣	H
X	⌒	NC

H = High Level
L = Low Level
X = Don't Care
NC = No Change
* = Level Change

2. **RECOMMENDED CONDITIONS OF USE AND ASSOCIATED CHARACTERISTICS** (not for inspection purposes)

V_{DD} recommended power supply voltage range 3 V to 15 V

2.1 **Static Characteristics**

All limits for E version at $T_{low} = -55°C$, $T_{high} = 125°C$
for S version at $T_{low} = -40°C$, $T_{high} = 85°C$

		V_{OO}	T_{low}	25°C	T_{high}	Units
V_{OL}	Low stage output voltage $V_I = V_{SS}$ or V_{DD} $I_O < 1\mu A$	5	0.05	0.05	0.05	V max.
		10	0.05	0.05	0.05	V max.
		15	0.05	0.05	0.05	V max.
V_{OH}	High state output voltage $V_I = V_{SS}$ or V_{DD} $I_O > 1\mu A$	5	4.95	4.95	4.95	V min.
		10	9.95	9.95	9.95	V min.
		15	14.95	14.95	14.95	V min.
V_{IL}	Low state input voltage					
	$V_O = 0.5$ V or 4.5 V	5	1.50	1.50	1.50	V max.
	$V_O = 1.0$ V or 9.0 V	10	3.00	3.00	3.00	V max.
	$V_O = 1.5$ V or 13.5 V	15	4.00	4.00	4.00	V max.
V_{IH}	High state input voltage					
	$V_O = 0.5$ V or 4.5 V	5	3.50	3.50	3.50	V min.
	$V_O = 1.0$ V or 9.0 V	10	7.00	7.00	7.00	V min.
	$V_O = 1.5$ V or 13.5 V	15	11.00	11.00	11.00	V min.
I_{OL}	Output drive sink current					
	E version					
	$V_O = 0.4$ V $V_I = 0$ or 5 V	5	0.64	0.51	0.36	mA min.
	$V_O = 0.5$ V $V_I = 0$ or 10 V	10	1.60	1.30	0.90	mA min.
	$V_O = 1.5$ V $V_I = 0$ or 15 V	15	4.20	3.40	2.40	mA min.
	S version					
	$V_O = 0.4$ V $V_I = 0$ or 5 V	5	0.52	0.44	0.36	mA min.
	$V_O = 0.5$ V $V_I = 0$ or 10 V	10	1.30	1.10	0.90	mA min.
	$V_O = 1.5$ V $V_I = 0$ or 15 V	15	3.60	3.00	2.40	mA min.
$-I_{OH}$	Output drive source current					
	E version					
	$V_O = 4.6$ V $V_I = 0$ or 5 V	5	0.25	0.20	0.14	mA min.
	$V_O = 9.5$ V $V_I = 0$ or 10 V	10	0.62	0.50	0.35	mA min.
	$V_O = 13.5$ V $V_I = 0$ or 15 V	15	1.80	1.50	1.10	mA min.
	S version					
	$V_O = 4.6$ V $V_I = 0$ or 5 V	5	0.20	0.16	0.12	mA min.
	$V_O = 9.5$ V $V_I = 0$ or 10 V	10	0.50	0.40	0.30	mA min.
	$V_O = 13.5$ V $V_I = 0$ or 15 V	15	1.40	1.20	1.00	mA min.
I_I	Input current for all permitted values of V_I					
	E version	15	±0.10	±0.10	±1.00	µA max.
	S version	15	±0.30	±0.30	±1.00	µA max.
I_{DD}	Power supply current					
	E version	15	20.0	20.0	600.0	µA max.
	S version	15	80.0	80.0	600.0	µA max.
C_{in}	Input capacitance. Any input $V_I = 0$ V	—	—	7.50	—	pF max.

EXAMPLE

2.2 Dynamic Characteristics

Switching Characteristics (C_L = 50 pF)

			V_{DD}	T_{low}	25°C	T_{high}	Units
t_{PHL}	Propagation Delay Time		5	–	460	–	ns max.
t_{PLH}	High to Low state and		10	–	165	–	ns max.
	Low to High state	**E Version**	15	–	120	–	ns max.
t_{PHL}	Propagation Delay Time		5	–	600	–	ns max.
t_{PLH}	High to Low state and		10	–	275	–	ns max.
	Low to High state	**S Version**	15	–	200	–	ns max.
t_{THL}	Transition Time		5	–	175	–	ns max.
	High to Low state		10	–	75	–	ns max.
		E Version	15	–	55	–	ns max.
t_{THL}	Transition Time		5	–	200	–	ns max.
	High to Low state		10	–	100	–	ns max.
		S Version	15	–	80	–	ns max.
t_{TLH}	Transition Time		5	–	350	–	ns max.
	Low to High state		10	–	150	–	ns max.
		E Version	15	–	110	–	ns max.
t_{TLH}	Transition time		5	–	400	–	ns max.
	Low to High state		10	–	200	–	ns max.
		S Version	15	–	160	–	ns max.
t_{PWC}	Minimum Clock pulse width		5	–	200	–	ns min.
			10	–	70	–	ns min.
		E Version	15	–	55	–	ns min.
t_{PWC}	Minimum Clock pulse width		5	–	250	–	ns min.
			10	–	125	–	ns min.
		S Version	15	–	95	–	ns min.
$f_{max.}$	Maximum Clock Pulse frequency		5	–	2.5	–	MHz min.
			10	–	7.0	–	MHz min.
		E Version	15	–	10.0	–	MHz min.
$f_{max.}$	Maximum Clock Pulse frequency		5	–	2.0	–	MHz min.
			10	–	4.0	–	MHz min.
		S Version	15	–	6.0	–	MHz min.

EXAMPLE

2.2 **Dynamic Characteristics** (cont.)

Switching Characteristics ($C_L = 50$ pF)

	V_{DD}	T_{low}	25°C	T_{high}	Units
t_r Maximum clock pulse rise and fall time	5	–	15	–	µs min.
t_f	10	–	15	–	µs min.
E Version	15	–	15	–	µs min.
t_r Maximum clock pulse rise and fall time	5	–	15	–	µs min.
t_f	10	–	15	–	µs min.
S Version	15	–	15	–	µs min.
t_{PWST} Setup time	5	–	– 15	–	ns max.
	10	–	– 5	–	ns max.
E Version	15	–	– 3	–	ns max.
$t_{PWST'}$ Setup time	5	–	0	–	ns max.
	10	–	0	–	ns max.
S Version	15	–	0	–	ns max.
t_{PWH} Hold Time	5	–	180	–	ns max.
	10	–	90	–	ns max.
E Version	15	–	75	–	ns max.
t_{PWH} Hold Time	5	–	220	–	ns max.
	10	–	110	–	ns max.
S Version	15	–	90	–	ns max.

EXAMPLE

		BS9490 F2810 to F2818 F2820 F2828

3. **MARKING**

(1) Each integrated circuit shall bear the following marking:

a. Type number (see Table 2).

b. Factory identification code.

c. Date code.

(2) Each primary package shall bear all the above markings and in addition

d. The British Standard detail specification number.

e. M.O.S. warning label.

4. **RELATED DOCUMENTS**

BS3934 Dimensions of semiconductor devices.

BS6001 Sampling procedures and tables for inspection by attributes.

BS9000 General requirements for electronic parts of assessed quality.

BS9400 Specification for integrated electronic circuits of assessed quality, generic data and methods of test.

PD9002 BS9000 component selection guide.

5. **ORDERING INFORMATION**

Orders for components to this specification shall contain the following minimum information:

(1) Quantity

(2) Manufacturer's type number (as Table 2).

(3) BS specification number, issue and date.

EXAMPLE

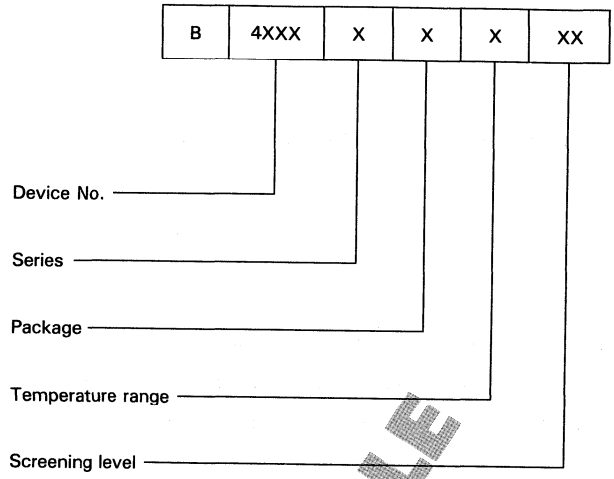
TABLE 2

Manufacturer's type number	BS specification number	Marking*
B4006BDE	BS9490 F2810 Issue 1 Dated	4006E BS
B4006BDE S1	BS9490 F2811 Issue 1 Dated	4006E BS S1
B4006BDE S2	BS9490 F2812 Issue 1 Dated	4006E BS S2
B4006BDE S3	BS9490 F2813 Issue 1 Dated	4006E BS S3
B4006BDE S4	BS9490 F2814 Issue 1 Dated	4006E BS S4
B4006BDS	BS9490 F2815 Issue 1 Dated	4006S BS
B4006BDS S2	BS9490 F2816 Issue 1 Dated	4006S BS S2
B4006BDS S3	BS9490 F2817 Issue 1 Dated	4006S BS S3
B4006BDS S4	BS9490 F2818 Issue 1 Dated	4006S BS S4
B4006BFE	BS9490 F2820 Issue 1 Dated	4006E BS
B4006BFE S1	BS9490 F2821 Issue 1 Dated	4006E BS S1
B4006BFE S2	BS9490 F2822 Issue 1 Dated	4006E BS S2
B4006BFE S3	BS9490 F2823 Issue 1 Dated	4006E BS S3
B4006BFE S4	BS9490 F2824 Issue 1 Dated	4006E BS S4
B4006BFS	BS9490 F2825 Issue 1 Dated	4006S BS
B4006BFS S2	BS9490 F2826 Issue 1 Dated	4006S BS S2
B4006BFS S3	BS9490 F2827 Issue 1 Dated	4006S BS S3
B4006BFS S4	BS9490 F2828 Issue 1 Dated	4006S BS S4

*See clause 3

BS9490 F2810 to F2818 F2820 F2828		

INTERPRETATION OF MANUFACTURERS TYPE NUMBER



EXAMPLE

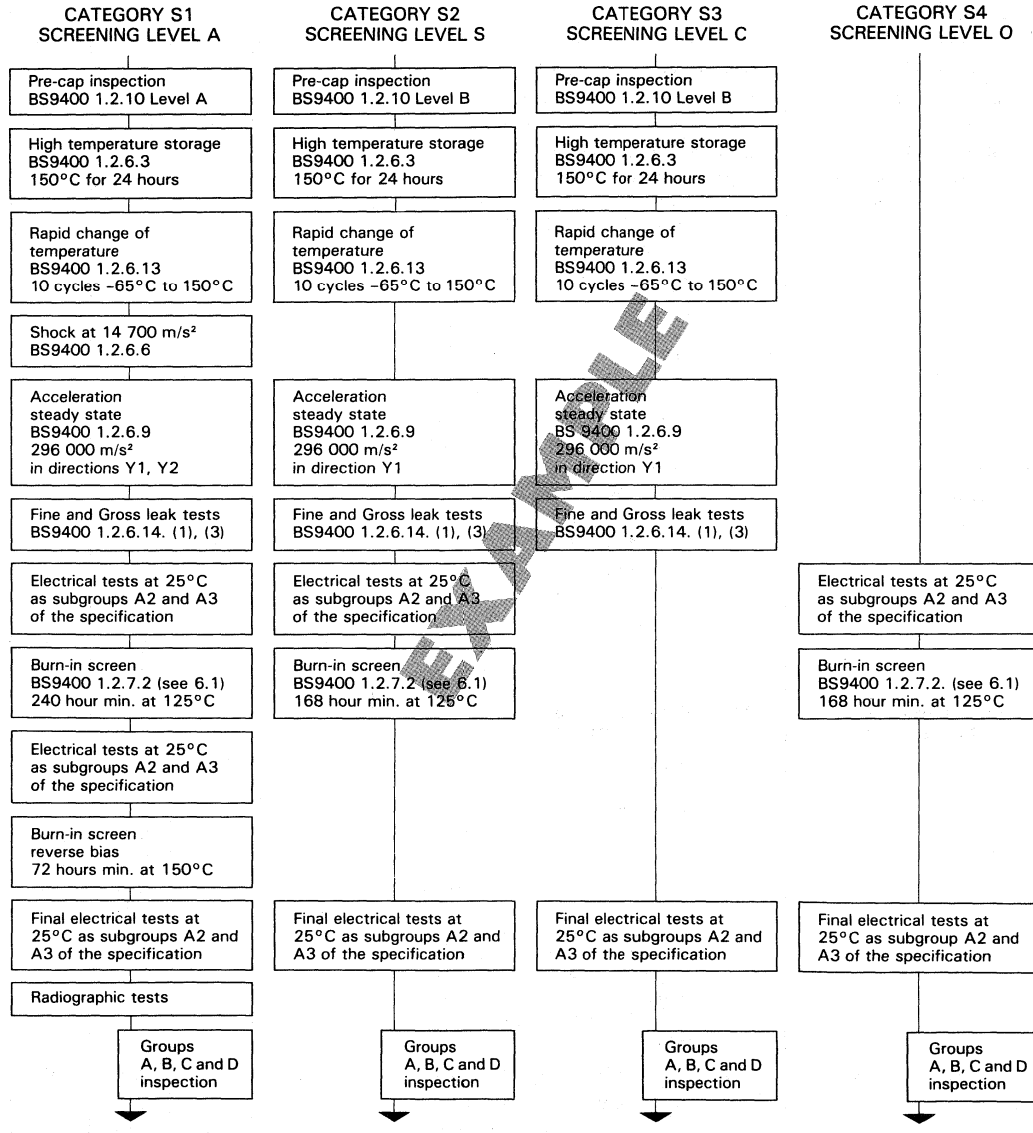
Key:

Device No.		4 digits
Series	B	B series (buffered)
	UB	B series (unbuffered)
Package	D	Dual-in-line
	F	Flatpack
Temperature range	S	Standard (— 40°C to 85°C)
	E	Extended (— 55°C to 125°C)
Screening level	(Blank)	Full assessment
	S1	Screening level S1
	S2	Screening level S2
	S3	Screening level S3
	S4	Screening level S4

Example: B4008BDS S2 is B4008, Series B, Dual-in-line — 40°C to 85°C BS9000 Screening level S2.

6. INSPECTION REQUIREMENTS

All tests to be conducted at $T_{amb} = 25°C$ unless otherwise specified.
Samples submitted to tests marked "D" shall not be accepted for release under BS9000 (see 2.6.5 of BS9000, Part 1).
If during electrical tests after Burn-in more than 10% defectives are found the production lot will be rejected.



Radiographic Tests

Each device shall be examined, for extraneous matter and assembly defects, in the X and Y directions.

Inspection	BS9400 reference and conditions of test	Symbol	Limits Min	Limits Max	Unit
Group A	Subgroup A5 not applicable				
Subgroup A0 Screening (where applicable)	100% Inspection (see Flow Chart) 1.2.9 1.2.10				
Subgroup A1 Visual inspection	**Inspection level I, AQL 1.5%** 1.2.2 none				
Subgroup A2 Verification of type of integrated circuit	**Inspection level II, AQL 0.15%** 1001 Perform functional truth table (Table 1) using the following definitions for high and low $V_I = V_{DD}$ or V_{SS} R_L 10 MΩ (see 7.8) V_{DD} 3 V: V_{OH} min. 2.50 V; V_{OL} max. 0.50 V V_{DD} 18 V: V_{OH} min. 16.90 V; V_{OL} max. 0.50 V				
Subgroup A3 Power supply current	**Inspection level II, AQL 1.5%** 2011 Test for appropriate state in Table 1 (see 7.8) $V_{IH} = 15$ V $V_{IL} = 0$ V $V_{DD} = 15$ V E Version S Version	I_{DD} I_{DD}	– –	20.0 80.0	µA µA
Low and high state input currents	2013 Each input tested in turn other inputs at 0 V $V_{DD} = 15$ V $V_{IL} = 0$ V $V_{IH} = 15$ V E Version S Version Each output tested separately. Unused inputs connected to V_{DD} or V_{SS}. Apply input conditions to give a high or low output state as applicable at each output (see Table 1)	$-I_{IL}$ I_{IH} $-I_{IL}$ I_{IH}	– – – –	0.10 0.10 0.30 0.30	µA µA µA µA
Low state output voltage	2001 $V_{DD} = 5$ V $V_I = 0$ or 5 V $V_{DD} = 10$ V $V_I = 0$ or 10 V $V_{DD} = 15$ V $V_I = 0$ or 15 V	V_{OL} V_{OL} V_{OL}	– – –	0.05 0.05 0.05	V V V
High state output voltage	2002 $V_{DD} = 5$ V $V_I = 0$ or 5 V $V_{DD} = 10$ V $V_I = 0$ or 10 V $V_{DD} = 15$ V $V_I = 0$ or 15 V	V_{OH} V_{OH} V_{OH}	4.95 9.95 14.95	– – –	V V V

EXAMPLE

Inspection	BS9400 reference and conditions of test		Symbol	Limits Min	Limits Max	Unit
Subgroup A3 (Contd.) Output drive source current	2018 V_{DD} = 5 V, V_I = 0 or 5 V, V_O = 4.6 V	E Version	$-I_{OH}$	0.20	—	mA
		S Version	$-I_{OH}$	0.16	—	mA
	V_{DD} = 10 V, V_I = 0 or 10 V, V_O = 9.5 V	E Version	$-I_{OH}$	0.50	—	mA
		S Version	$-I_{OH}$	0.40	—	mA
	V_{DD} = 15 V, V_I = 0 or 15 V, V_O = 13.5 V	E Version	$-I_{OH}$	1.50	—	mA
		S Version	$-I_{OH}$	1.20	—	mA
Output drive sink current	2018 V_{DD} = 5 V, V_I = 0 or 5 V, V_O = 0.4 V	E Version	I_{OL}	0.51	—	mA
		S Version	I_{OL}	0.44	—	mA
	V_{DD} = 10 V, V_I = 0 or 10 V, V_O = 0.5 V	E Version	I_{OL}	1.30	—	mA
		S Version	I_{OL}	1.10	—	mA
	V_{DD} = 15 V, V_I = 0 or 15 V, V_O = 1.5 V	E Version	I_{OL}	3.40	—	mA
		S Version	I_{OL}	3.00	—	mA
Verification of integrated circuit function under worst case conditions	1001 Perform functional truth table (Table 1) using the following definitions for high, low and V_{DD} (see) 7.8) $R_L > 10\,M\Omega$					

V_{DD}	V_{IH}	V_{IL}	V_{OH}	V_{OL}
5	3.5	1.5	4.5	0.5
10	7.0	3.0	9.0	1.0
15	11.0	4.0	13.5	1.5

EXAMPLE

Inspection	BS9400 reference and conditions of test		Symbol	Limits		Unit
				Min	Max	
Subgroup A4	**Inspection level S-4, AQL 4.0%** Input frequency = 500 kHz Duty cycle = 50% C_L = 50 pF (See Figure 3 and 4)					
Propagation Delay Time High to Low state and Low to High state	2008	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V **E Version**	^tPHL ^tPLH ^tPHL ^tPLH ^tPHL ^tPLH	– – –	460 165 120	ns ns ns
Propagation Delay Time High to Low state and Low to High state	2008	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V **S Version**	^tPHL ^tPLH ^tPHL ^tPLH ^tPHL ^tPLH	– – –	600 275 200	ns ns ns
Transition Time High to Low state	2007	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V **E Version**	^tTHL ^tTHL ^tTHL	– – –	175 75 55	ns ns ns
Transition Time High to Low state	2007	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V **S Version**	^tTHL ^tTHL ^tTHL	– – –	200 100 80	ns ns ns
Transition Time Low to High state	2007	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V **E Version**	^tTLH ^tTLH ^tTLH	– – –	350 150 110	ns ns ns
Transition Time Low to High state	2007	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V **S Version**	^tTLH ^tTLH ^tTLH	– – –	400 200 160	ns ns ns

EXAMPLE

Inspection	BS9400 reference and conditions of test	Symbol	Limits		Unit
			Min	Max	
Subgroup A4 (contd)	**Inspection level S-4, AQL 4.0%** Input frequency = 500 kHz Duty cycle = 50% C_L = 50 pF (See Figure 3 and 4)				
Minimum Clock Pulse Width	2017 V_{DD}= 5 V	t_{PWC}	–	200	ns
	V_{DD}= 10 V	t_{PWC}	–	70	ns
	V_{DD}= 15 V **E Version**	t_{PWC}	–	55	ns
Minimum Clock Pulse Width	2017 V_{DD}= 5 V	t_{PWC}	–	250	ns
	V_{DD}= 10 V	t_{PWC}	–	125	ns
	V_{DD}= 15 V **S Version**	t_{PWC}	–	95	ns

EXAMPLE

Inspection	BS9400 reference and conditions of test	Symbol	Limits		Unit
			Min	Max	
Group B	Subgroups B4 and B5 not applicable				
Subgroup B1	**Inspection level S-2, AQL 6.5%**				
Dimensions	1.2.3. BS3934 SO-87B	A	–	5.10	mm
		D	–	20.32	mm
	BS3934 SO-93A	A	–	2.27	mm
		H_E	18.30	19.60	mm
		n	14	14	
Subgroup B2 (a) '(D)'	**Inspection level S-4, AQL 4.0%**				
Solderability	1.2.6.15.1 See Note 2				
Subgroup B2 (b)	**Inspection level S-4, AQL 4.0%**				
Rapid change of temperature	1.2.6.13 T_{amb} = – 65°C to 150°C Transfer time 5 min. max.				
Followed by					
Fine leak	1.2.6.14.1 4.96×10^{-8} mbar l/s				
Gross leak	1.2.6.14.3				
Subgroup B3 '(D)'	**Inspection level S-3, AQL 6.5%**				
Terminal robustness, bending	1.2.6.16.3 and 1.2.6.16.2 as applicable				
Subgroup B6	**Inspection level S-4, AQL 4.0%**				
Acceleration, steady state	1.2.6.9 Non-operating Direction of acceleration = Y2 Acceleration = 196 000 m/s²				
Subgroup B7	**Inspection level S-4, AQL 1.5%**				
Electrical endurance	1.2.7.2.6 V_{DD} = 15 V (See 6.1) E version T_{amb} = 125°C min. S version T_{amb} = 85°C min. Duration = 160 h. min.				
Post-test end-points for subgroups B2(b), B6 and B7					
Verification of type of integrated circuit	1001 Requirements as for subgroup A2				
Low state output voltage	2001	V_{OL}			
High state output voltage	2002	V_{OH}			
Low state output current	2018 Conditions and limits as for subgroup A3	I_{OL}			
High state output current	2018	$-I_{OH}$			
Power supply current	2011	I_{DD}			
Subgroup B8					
CTR information	1.1.11 Attributes information for subgroups B2(a), B2(b), B3 B6 and B7				

SAMPLE

Inspection	BS9400 reference and conditions of test	Symbol	Limits		Unit
			Min	Max	
Group C	Subgroup C2 not applicable				
Subgroup C1	**Inspection level S-2, AQL 6.5%**				
Dimensions	1.2.3 BS3934 SO-87B	A_1	0.51	–	mm
		b	0.38	0.59	mm
		c	0.20	0.36	mm
		L	2.54	4.50	mm
	BS3934 SO-93A	b	0.25	0.54	mm
		e	1.27TP	–	mm
		L_E	5.40	–	mm
		Z	–	0.63	mm
Subgroup C3	**Inspection level S-2, AQL 6.5%**				
Vibration, swept frequency	1.2.6.8.1 Non-operating Frequency range = 150 Hz to 2000 Hz Acceleration = 196 m/s²				
Followed by Shock	1.2.6.6 Non-operating Peak acceleration = 14.700 m/s² Duration = 0.5 ms The body shall be clamped and three successive shocks shall be applied in each of directions of Y_1, Y_2 and X_1				
and Damp heat cyclic	1.2.6.5 28 cycles				
Subgroup C4 (a)	**Inspection level S-4, AQL 4.0%** E Version T_{amb} = 125°C S Version T_{amb} = 85°C Test conditions as for subgroup A3				
Low state output voltage	2001 V_{DD} = 5 V	V_{OL}	–	0.05	V
	V_{DD} = 10 V	V_{OL}	–	0.05	V
	V_{DD} = 15 V	V_{OL}	–	0.05	V
High state output, voltage	2002 V_{DD} = 5 V	V_{OH}	4.95	–	V
	V_{DD} = 10 V	V_{OH}	9.95	–	V
	V_{DD} = 15 V	V_{OH}	14.95	–	V
Power supply current	2011 V_{DD} = 15 V E Version	I_{DD}	–	600.0	µA
	S Version	I_{DD}	–	600.0	µA
Output drive source current	2018 V_{DD} = 5 V E Version	$-I_{OH}$	0.14	–	mA
	S Version	$-I_{OH}$	0.12	–	mA
	V_{DD} = 10 V E Version	$-I_{OH}$	0.35	–	mA
	S Version	$-I_{OH}$	0.30	–	mA
	V_{DD} = 15 V E Version	$-I_{OH}$	1.10	–	mA
	S Version	$-I_{OH}$	1.00	–	mA
Output drive sink current	2018 V_{DD} = 5 V E Version	I_{OL}	0.36	–	mA
	S Version	I_{OL}	0.36	–	mA
	V_{DD} = 10 V E Version	I_{OL}	0.90	–	mA
	S Version	I_{OL}	0.90	–	mA
	V_{DD} = 15 V E Version	I_{OL}	2.40	–	mA
	S Version	I_{OL}	2.40	–	mA

EXAMPLE

Inspection	BS9400 reference and conditions of test			Symbol	Limits		Unit
					Min	Max	
Subgroup C4(b)	**Inspection level S-4, AQL 4.0%** E Version $T_{amb} = -55°C$ S Version $T_{amb} = -40°C$ Test conditions as for subgroup A3						
Low state output voltage	2001	$V_{DD} = 5$ V $V_{DD} = 10$ V $V_{DD} = 15$ V		V_{OL} V_{OL} V_{OL}	– – –	0.05 0.05 0.05	V V V
High state output voltage	2002	$V_{DD} = 5$ V $V_{DD} = 10$ V $V_{DD} = 15$ V		V_{OH} V_{OH} V_{OH}	4.95 9.95 14.95	– – –	V V V
Power supply current	2011	$V_{DD} = 15$ V	E Version S Version	I_{DD} I_{DD}	– –	20.0 80.0	µA µA
Output drive source current	2018	$V_{DD} = 5$ V	E Version S Version	$-I_{OH}$ $-I_{OH}$	0.25 0.20	– –	mA mA
		$V_{DD} = 10$ V	E Version S Version	$-I_{OH}$ $-I_{OH}$	0.62 0.50	– –	mA mA
		$V_{DD} = 15$ V	E Version S Version	$-I_{OH}$ $-I_{OH}$	1.80 1.40	– –	mA mA
Output drive sink current	2018	$V_{DD} = 5$ V	E Version S Version	I_{OL} I_{OL}	0.64 0.52	– –	mA mA
		$V_{DD} = 10$ V	E Version S Version	I_{OL} I_{OL}	1.60 1.30	– –	mA mA
		$V_{DD} = 15$ V	E Version S Version	I_{OL} I_{OL}	4.20 3.60	– –	mA mA
Subgroup C5 Electrical endurance	**Inspection level S-3, AQL 4.0%** 1.2.7.2.6 Test conditions as for subgroup B7 Duration 2000 h. min.						
Post-test end-points for subgroups C3 and C5	Tests, test conditions and limits as for post-test end-points in Group 8. Additionally corrosion check as 1.2.6.5						
Subgroup C6 CTR information	1.1.11 Atributes information for V_{OL}, V_{OH}, I_{DD} and $-I_{OH}$ for subgroups C3 and C5 Measurements information for I_{OL} and $-I_{OH}$ for one output per package after the test in subgroup C5.						

EXAMPLE

Inspection	BS9400 reference and conditions of test	Symbol	Limits		Unit
			Min	Max	
Group D (See Note 1)	Subgroups D2 and D3 not applicable				
Subgroup D1 Dimensions	**Inspection level S-2** 1.2.3. BS3934 SO-87B BS3934 SO-93A All dimensions not checked in subgroups B1 and C1				
Subgroup D4 Electrical endurance	**Inspection level S-3** 1.2.7.2.6 Test conditions and limits as for subgroup B7 Duration 8000 h. min.				
Post-test end-points for subgroup D4	Tests, test conditions and limits as for post-test end-point in group B				
Subgroup D5 CTR information	1.1.11 Attributes information for V_{OL}, V_{OH}, I_{DD} and $-I_{OH}$ after subgroup D4 Measurements information for I_{OL} and $-I_{OH}$ (one output only per package) after subgroup D4				

EXAMPLE

Note 1: See paragraph 1.1.10 of BS9400

Note 2: When method 1.2.6.15.1 (1) is used the inspection level is reduced to S3

6.1 BURN-IN AND ELECTRICAL ENDURANCE CONDITIONS

100% Burn-in conducted in either a static or dynamic mode.
Electrical endurance is conducted in a dynamic mode only.

Table 3

Static Burn-in (Notes 3 and 4)	T_{amb}	Ambient temperature	E Version S Version	125°C min. 85°C min.
	V_{DD} V_I	Power supply voltage Input voltage		15 V V_{DD} or V_{SS}
Dynamic Burn-in and Electrical endurance (Note 3)	T_{amb}	Ambient temperature	E Version S Version	125°C 85°C
	V_{DD} V_I	Power supply voltage Input voltage		15 V V_{DD} or V_{SS}
		Input frequency Duty cycle		50 kHz 50%
	t_{TLH} t_{THL}	Rise time Fall time		50 ns max. 50 ns max.

Note 3 Unused inputs connected either directly to the supplies or via a nominal 47 kΩ resistor. Outputs connected either to $V_{DD/2}$ via a normal 47kΩ resistor or left open circuit. (See 7.8).

Note 4 Inputs are to be connected so that at least one P. channel and one N. channel is reverse biased in each circuit element.

Note 5 Circuit diagrams for the tests held by National Supervisory Inspectorate.

EXAMPLE

SWITCHING TIME TEST CONDITIONS

Loading conditions shown below

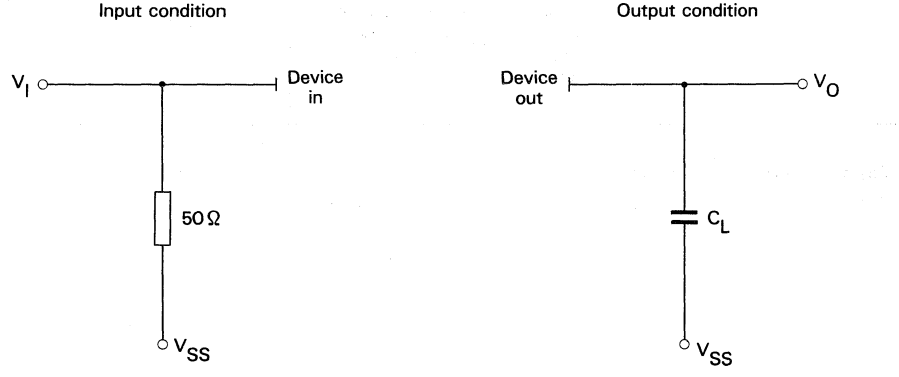


Figure 3

SWITCHING TIME WAVEFORMS

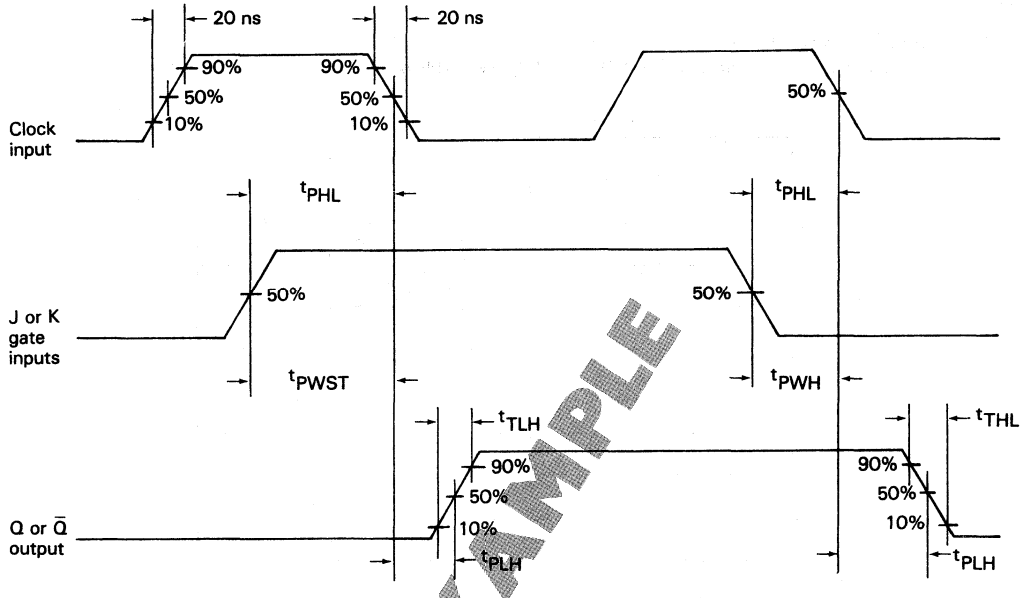


Figure 4

EXAMPLE

7. ADDITIONAL INFORMATION

7.1 Input curent

The main contribution to the input current is that due to the diode protection circuit and is typically 10 pA at 25°C.

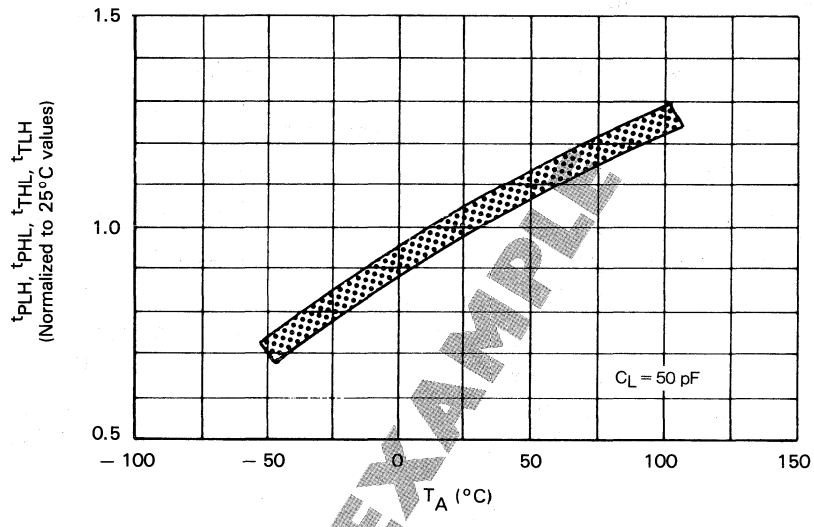
7.2 Loading rules

Due to the very low input current requirements for CMOS there is practically no d.c. fanout factor limitation when driving other CMOS inputs.

The actual fanout of the CMOS device is limited by a capacitive load consideration based on the desired system operating frequency.

7.3 Variation of switching parameters with temperature

A normalized plot showing variations of ^{t}PLH, ^{t}PHL, ^{t}TLH, ^{t}THL with temperature is shown below.



EXAMPLE

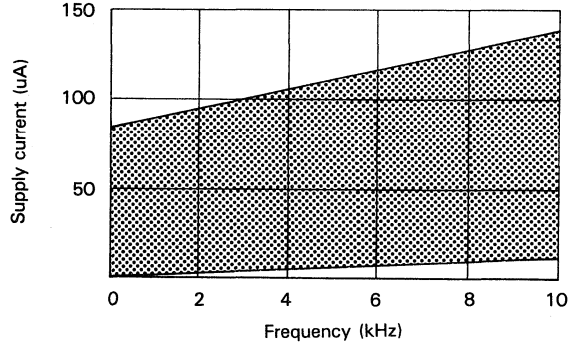
7.4 Noise immunity

The noise immunity V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "High" or "Low" input level before producing an output state change. The noise immunity is specified for worst case voltage level.

7.5 Unused inputs

Unused inputs should be connected to either V_{DD} or V_{SS}

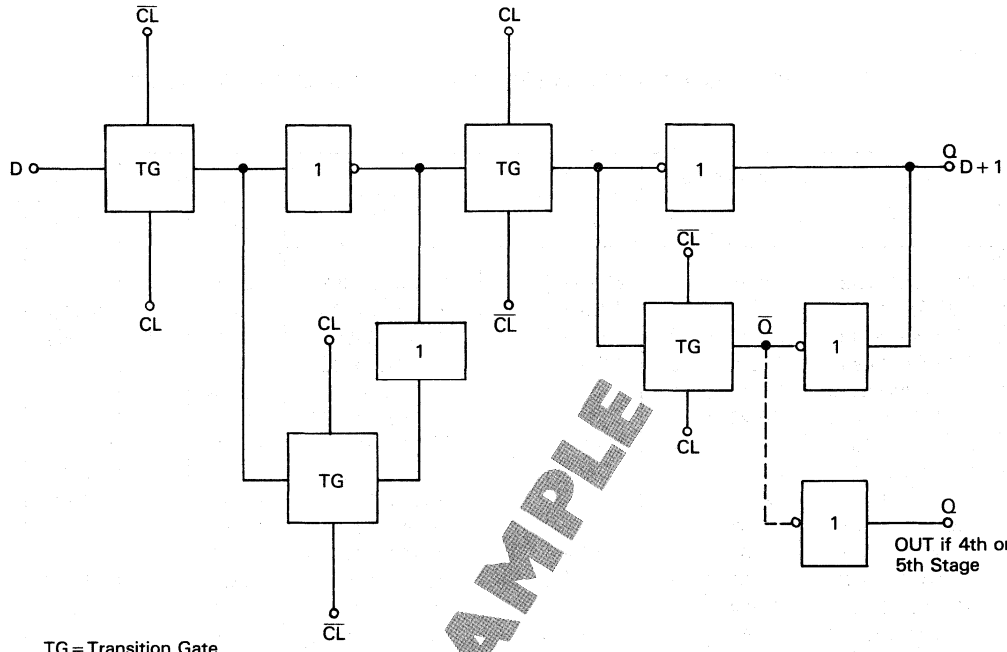
7.6 Power supply current v frequency



7.7 Each input is protected by a multi-diode/resistive network.

7.8 Apply to the manufacturer for further information

LOGIC DIAGRAM



TG = Transition Gate
CL = Clock

Figure 5

EXAMPLE

CERTIFIED TEST RECORD

MOTOROLA LTD

COLVILLES ROAD — KELVIN ESTATE — EAST KILBRIDE — SCOTLAND

Device title	BS 9490BSI				Device title	BS9490		BSI	
	Spec	ISS	Cert	ISS		Spec	ISS	Cert	ISS
MC14000ALS3	F1235	2	0731/F	1	MC14023BCLS3	F2596		*	
MC14000CLS3	F1237	2	0733/F	1	MC14025ALS3	F1487	2	0757/F	1
MC14001ALS3	F1247	2	0736/F	1	MC14025CLS3	F1489	2	0759/F	1
MC14001CLS3	F1249	2	0738/F	1	MC14025BALS3	F2608		*	
MC14001BALS3	F2514	1	*		MC14025BCLS3	F2614		*	
MC14001BCLS3	F2520	1	*		MC14070BALS3	F1728		*	
MC14002ALS3	F1259	2	0741/F	1	MC14070BCLS3	F1730		*	
MC14002CLS3	F1261	2	0743/F	1	MC14071ALS3	F1740	2	0807/F	1
MC14002BALS3	F2532	1	*		MC14071CLS3	F1742	2	0809/F	1
MC14002BCLS3	F2538	1	*		MC14071BALS3	F2626		*	
MC14011ALS3	F1331	2	0816/F	1	MC14071BCLS3	F2632		*	
MC14011CLS3	F1333	2	0818/F	1	MC14081ALS3	F1826	2	0812/F	1
MC14011BALS3	F2554		*		MC14081CLS3	F1828	2	0814/F	1
MC14011BCLS3	F2560		*		MC14081BALS3	F2640		*	
MC14012ALS3	F1343	2	0747/F	1	MC14081BCLS3	F2646		*	
MC14012CLS3	F1345	2	0749/F	1	MC14507ALS3	F1926		*	
MC14012BALS3	F2572		*		MC14507CLS3	F1928		*	
MC14012BCLS3	F2578		*		MC14023ALS3	F1463	2	0752/F	1
MC14023BALS3	F2590		*		MC14023CLS3	F1465	2	0754/F	1

EXAMPLE

Description of Component: CMOS silicon Monolithic integrated circuit

Current six months' period 1.1.78 to 30.6.78

Date of commencement of current three years' period 1.7.76

This certified test record is a complete and accurate record of the tests carried out in accordance with the specified procedures.

CHIEF INSPECTOR SUPERVISING INSPECTOR

Subgroup		Current six months' period		Current three years period	
		Tested	Defectives	Tested	Defectives
B2 (a)	Solderability	26	0	26	0
B2 (b)	Rapid change of temperature	33	0	33	0
B3	Robustness of terminations	26	0	26	0
B6	Steady state acceleration	33	0	33	0
B7	Electrical endurance 168h	64	1	64	1
C3	Vibration Shock Damp heat cyclic	8	1	8	1
C5	Electrical endurance 2000h	20	0 See remarks	20	0
D4	Electrical endurance 8000h	–	–	–	0

EXAMPLE

BS9490 F1246/1247

MC14001ALS2/S3

Lot No. 1892

Report No. _____

Subgroup C5
POST END POINT ELECTRICAL TEST

Test No.	Description	Range	Units	Frequency
241	I_{IH}	0 - 3	nA	133
8 Tests per	Input Leakage	3 - 7	nA	19
unit	Low State	7 - 9	nA	0
	V_{DD} = 15 V Limits = 100 nA. max.			
231	$-I_{IL}$	0 - 1	nA	148
8 Tests per	Input Leakage	1 - 2	nA	3
unit	High State	2 - 3	nA	1
	V_{DD} = 15 V	3 - 4	nA	0
	Limits = 100 nA max.			
240 and 241	V_{OL}	0.000 - 0.001	V	122
8 Tests per	Out Voltage	0.001 - 0.002	V	30
unit	Low State	0.002 - 0.003	V	0
	V_{DD} = 15 V Limits = 0.05 V max.			

BS9490 F1246/1247 Report No. _____

MC14001ALS2/S3

Lot No. 1892

Subgroup C5
POST END POINT ELECTRICAL TEST

Test No.	Description	Range	Units	Frequency
242 and 243	V_{OL}	0.000 - 0.001	V	115
8 Tests per unit	Out Voltage	0.001 - 0.002	V	36
	Low State	0.002 - 0.003	V	1
	V_{DD}= 10 V Limits = 0.05 V max.	0.003 - 0.004	V	0
244 and 245	V_{OL}	0.000 - 0.001	V	86
8 Tests per unit	Out Voltage	0.001 - 0.002	V	66
	Low State	0.002 - 0.003	V	0
	V_{DD}= 5 V Limits = 0.05 V			
246	$-V_{OH}$	15.000 - 14.999	V	58
4 Tests per unit	Out Voltage	14.999 - 14.998	V	18
	High State V_{DD}= 15 V	14.998 - 14.997	V	0
247	$-V_{OH}$	10.000 - 9.999	V	55
4 Tests per unit	Out Voltage	9.999 - 9.998	V	21
	High State V_{DD}= 10 V Limits = 9.95 V min.	9.998 - 9.997	V	0
250	$-V_{OH}$	5.000 - 4.999	V	63
4 Tests per unit	Out Voltage	4.999 - 4.998	V	13
	High State V_{DD}= 5 V Limits = 4.95 V min.	4.998 - 4.997	V	0

EXAMPLE

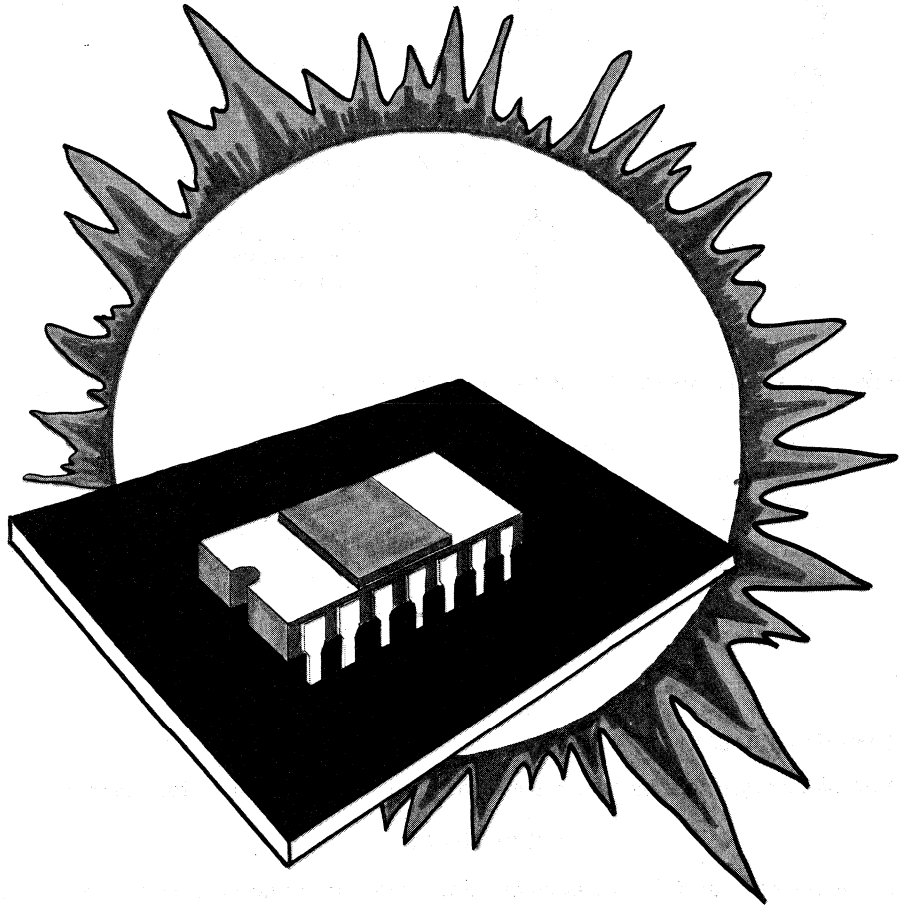
REMARKS:

1. C3 REJECT — Not catastrophic, met CL electrical limits.
   Input Leakage 110 nA. Max. allowed 100 nA.
2. C5 Initially one sample had been thought to be a reject and so was left out of the distribution summary. Upon further investigation, the problem was determined to be a machine fault.

NOTES

1. These devices were qualified on fully assessed product and screening facilities.
   Data on fully assessed presented in CTRs reference SS1/76B/S
2. BSI CERTIFICATES — Devices marked* have been qualified and the certificate is pending.
3. The structural set that this CTR refers to is No. 1 on the structural similarity chart issue 1 (QA1/1).

Burn-in options 4



BURN-IN OPTIONS

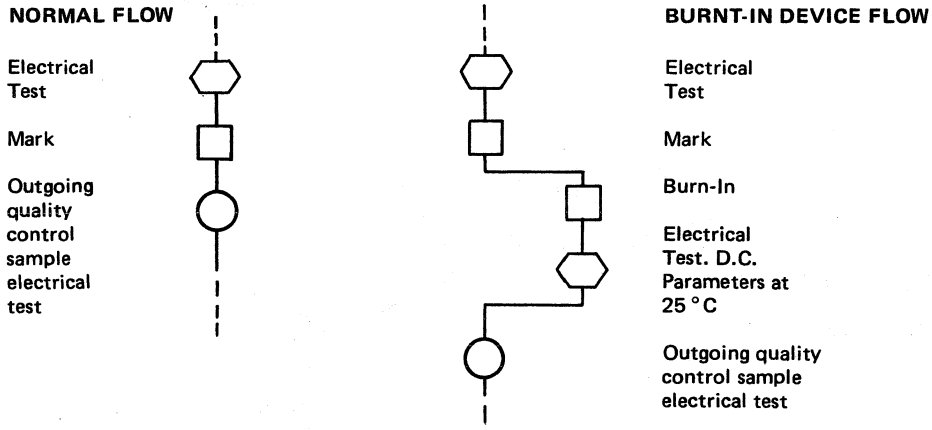
Motorola CMOS integrated circuits are manufactured under strict quality control. In-process screens and tight out-going inspection result in a high order of quality and reliability.

In addition, **Burn-in** is an option available on all CMOS packaged products. The benefits of this option are:

- reduced infant mortality;
- reduced board and system rework;
- reduced equipment downtime;
- reduced field failures.

Additional processing of these burnt-in circuits is as follows:

4



Motorola Burn-in is performed under the following conditions:

V_{DD}	15 V
Temperature	125°C ambient
Time	168 hours
Bias	Dynamic for Memories and Analog Circuits Static for all others.

ORDERING INFORMATION

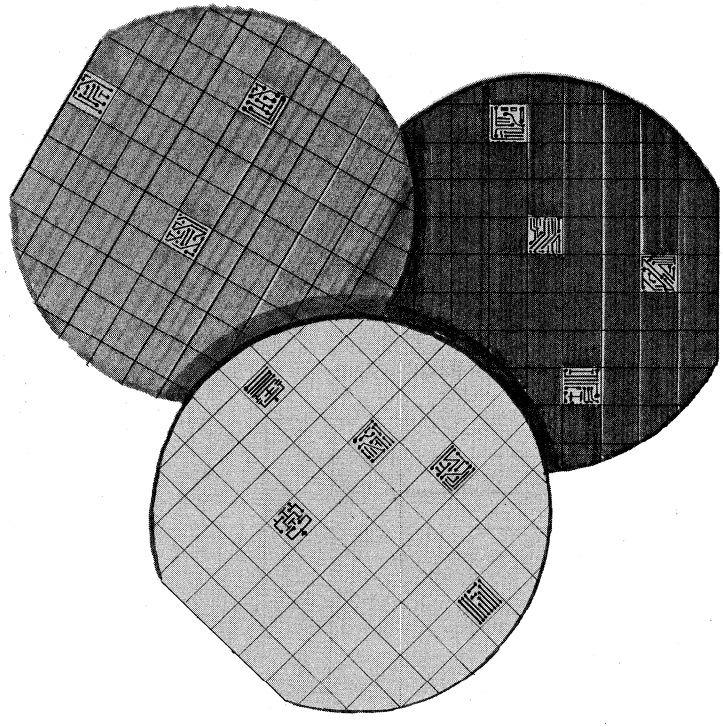
The Burn-in option is selected by adding the suffix D to the part number, for example:

MC14001BALD

Other burn-in options can be made available. For further information consult Motorola Sales Offices.

Further details on improved reliability resulting from burn-in are given in the Reliability section of this book.

CMOS Chips 5



CMOS CHIPS

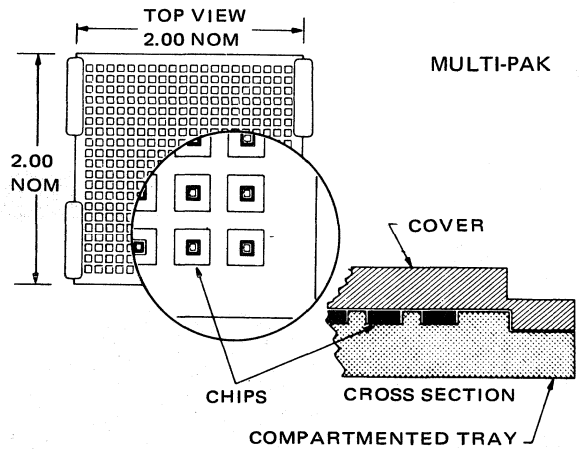
The majority of standard commercial and military quality devices are available in chip form. These chips are normally supplied in multi-pak. If requested, unscribed, sample probed or fully probed wafers can be supplied in Wafer Pak.

In Wafer test the die on the wafer are individually tested to Data Sheet or negotiated specifications. Die failing any test are automatically inked as rejects.

It is not possible to test all AC parameters of die on the wafer. These parameters can be guaranteed by testing encapsulated samples from wafers.

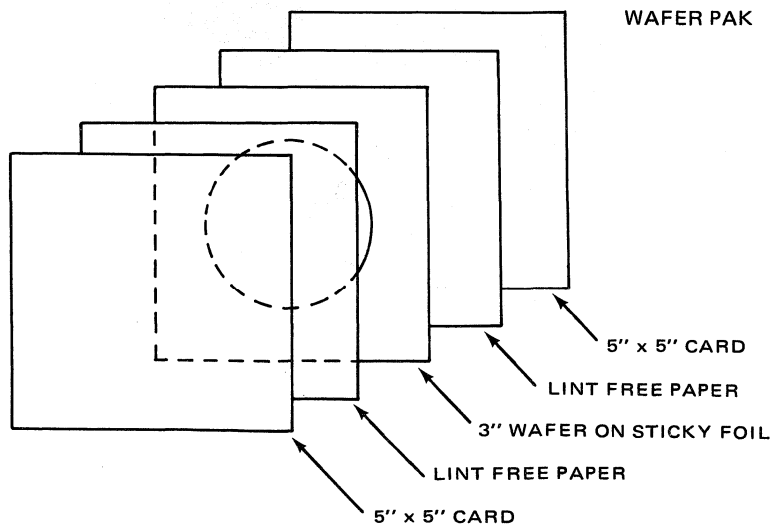
FIGURE 1

INDIVIDUAL PACKAGING



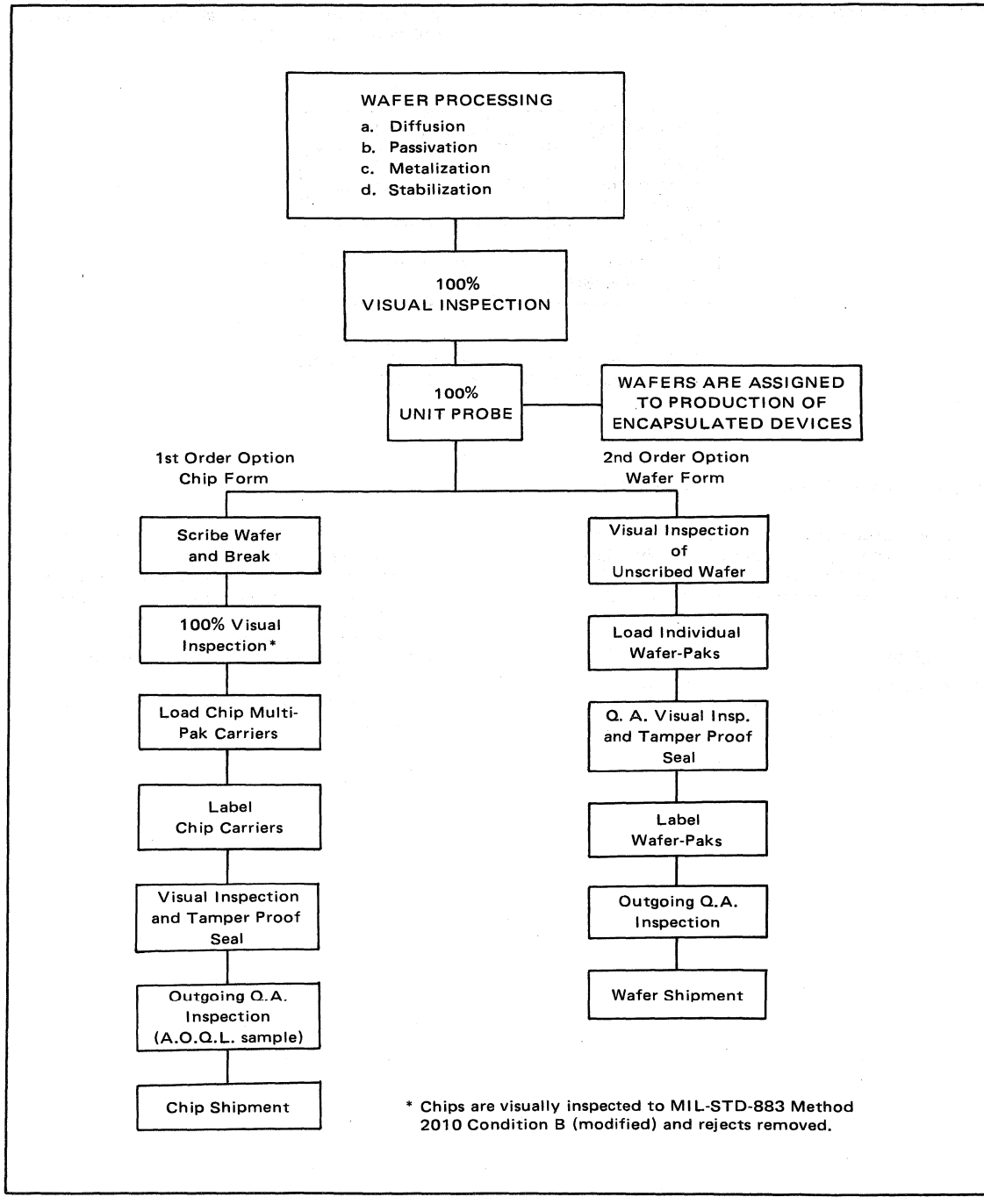
This is a 2" x 2" waffle type carrier with a separate hole for each chip, holding up to 400 chips depending upon chip size.

WAFER PACKAGING



The Wafer-Pak is sealed in an evacuated plastic bag.

Following wafer test the wafers are scribed the die underging 100% visual inspection prior to shipping. In addition, sample dice are sealed into hermetric packages and tested over the full range of electrical characteristics. The flow chart in Fig. 2 shows the monitoring and processing of the chips before shipping.



QUALITY ASSURANCE

Integrated circuit chips are subjected to the same in-process controls as Motorola's standard encapsulated devices. The chips processing and quality control requirements are designed to ensure reliability and performance of the finished product.

Chip processing steps include several independent visual and electrical checks on the product by Quality Assurance (QA) personnel. Prior to shipment, a final QA examination of the product is performed to insure that all requirements of the pruchase order are met.

Device category	AQL	Level	Mag
Commercial temperature range: UB, B	1.5	II	75x - 150x
Military Temperature range: UBH, BH	1.0	II	75x - 150x

For special AQL's, mil standard or BS9400 selections contact your local Motorola Sales Office, Sampling tables: BS6001 or MIL-STD 105D.

5

INCOMING INSPECTION PROCEDURES

Motorola assures that the devices will meet the customer's incoming visual inspection when inspected to the visual criteria specified. Inspection must be performed at the power and magnification indicated.

How to Order

MCC14XXX

- B : B Series Commercial
- BH : B Series Military
- UB : UB Series Commercial
- UBH : UB Series Military

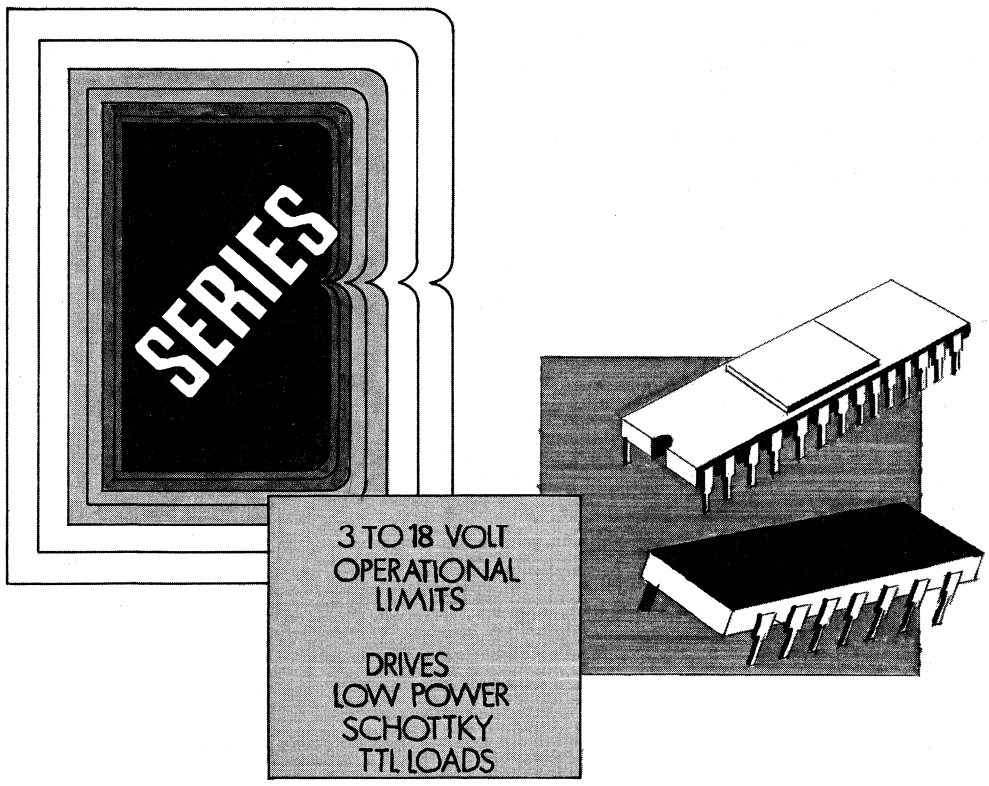
The ordering code is in fact quite simple, all you do to the standard device code is:

a) Remove all suffix package and temperature designators from the desired device type (eg. MC14011BCL now becomes MC14011B).

b) for chips – add a C to the prefix designator (eg. MC14011B now becomes MCC14011B).

For the latest information on which chips are available or how to order wafers please contact your local sales office.

B-Series family data 6



B AND UB SERIES CMOS FAMILY DATA

The CMOS Devices in this volume which have a B or UB suffix meet the minimum values for the industry-standardized* family specification. These standardized values are shown in the Maximum Ratings and Electrical Characteristics Tables. In addition to a standard minimum specification for characteristics the B/UB devices feature:

- **3–18 volt operational limits**
- **Capable of driving two low-power TTL loads, one low-power Schottky TTL load, or two HTL loads over the rated temperature range**
- **Maximum input current of ±1 μA at 15 volt power supply over the temperature range**
- **Parameters specified at 5.0, 10, and 15 volt supply**
- **Noise margins of 1.0 V min @ 5.0 V supply**
  2.0 V min @ 10 V supply
  2.5 V min @ 15 V supply

The industry-standardized maximum ratings and recommended operating range are shown at the bottom of this page. Limits for the static characteristics are shown in two formats: Table 1 is in the industry format and Table 2 is in the equivalent Motorola format. The Motorola format is used throughout this data book. Additional specification values are shown on the individual data sheets.

Switching characteristics for the B and UB series devices are specified under the following conditions:

Load Capacitance, C_L, of 50 pF
Input pulse voltage equal to $+V_{DD}$ supply voltage
Input pulse rise and fall times of 20 ns
Propagation Delay times measured from 50% point of input voltage to 50% point of output voltage
Three different supply voltages: 5, 10, and 15 V

Exceptions to the B and UB Series Family Specification

There are a number of devices which have a B or UB suffix whose input and/or outputs vary somewhat from the family specification because of functional requirements. Some categories of notable exceptions are:

Devices with specialized outputs on the chip, such as NPN emitter-follower drivers or transmission gates, do not meet output specifications.

Devices with specialized inputs, such as oscillator inputs, have unique input specifications.

Input Voltage

The input voltage specification is interpreted as the worst-case input voltage to produce an output level of "1" or "0". The "1" or "0" output level is defined as a deviation from the supply (V_{DD}) and ground (V_{CC}) levels. For a 5.0 V supply, this deviation is 0.5 V; for a 10 V supply, 1.0 V; and for 15 V, 1.5 V. As an example, in a device operating at a 5.0 V supply, the device with the input starting at ground is guaranteed to switch on or before 3.5 V and not to switch up to 1.5 V. Switching and not switching are defined as within 0.5 V of the ideal output level for the example with a 5.0 V supply. The actual switching level referred to the input is between 1.5 V and 3.5 V.

Noise Margin

The values for input voltage and the given defined output deviation lead to minimum noise margins of 1.0 V, 2.0 V, and 2.5 V for a 5.0 V, 10 V, and 15 V supply, respectively.

Output Drive Current

Devices in the B Series are capable of sinking a minimum of 0.36 mA over the temperature range with a 5.0 V supply. This value guarantees that these CMOS devices will drive one Schottky low-power TTL input.

B Series vs UB CMOS

The primary difference between B series and UB series devices is that UB series gates and inverters are constructed with a single inverting stage between input and output. The decreased gain caused by using a single stage results in less noise immunity and a transfer characteristic that is less ideal.

The decreased gain is quite useful when CMOS Gates and inverters are used in a "Linear" mode to form oscillators, monostables or amplifiers. The decreased gain results in increased stability and a "cleaner" output waveform. In addition to linear operation, the UB gates and inverters offer an increase in speed since only a single stage is involved.

The B series, UB CMOS, and devices with no suffix can be used interchangeably in digital circuits that interface to other CMOS devices.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING RANGE

DC Supply Voltage	V_{DD}	+3.0 to +15	Vdc

*Specifications coordinated by EIA/JEDEC Solid-State Products Council.

TABLE 1 – EIA/JEDEC FORMAT FOR CMOS INDUSTRY B AND UB SERIES SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

PARAMETER		TEMP RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS						UNITS
					T_{LOW}*		+ 25°C		T_{HIGH}*		
					Min	Max	Min	Max	Min	Max	
I_{DD}	Quiescent Device Current	Mil	5	$V_{in} = V_{SS}$ or V_{DD}		0.25		0.25		7.5	μAdc
			10			0.5		0.5		15	
			15			1.0		1.0		30	
	GATES	Comm	5	All valid input combinations		1.0		1.0		7.5	μAdc
			10			2.0		2.0		15	
			15			4.0		4.0		30	
		Mil	5	$V_{IN} = V_{SS}$ or V_{DD}		1.0		1.0		30	μAdc
			10			2.0		2.0		60	
			15			4.0		4.0		120	
	BUFFERS, FLIP-FLOPS	Comm	5	All valid input combinations		4		4.0		30	μAdc
			10			8		8.0		60	
			15			16		16.0		120	
		Mil	5	$V_{IN} = V_{SS}$ or V_{DD}		5		5		150	μAdc
			10			10		10		300	
			15			20		20		600	
	MSI	Comm	5	All valid input combinations		20		20		150	μAdc
			10			40		40		300	
			15			80		80		600	
V_{OL}	Low-Level Output Voltage	All	5	$V_{IN} = V_{SS}$ or V_{DD} $\lvert I_O \rvert < 1\mu A$		0.05		0.05		0.05	Vdc
			10			0.05		0.05		0.05	
			15			0.05		0.05		0.05	
V_{OH}	High-Level Output Voltage	All	5	$V_{IN} = V_{SS}$ or V_{DD} $\lvert I_O \rvert < 1\mu A$	4.95		4.95		4.95		Vdc
			10		9.95		9.95		9.95		
			15		14.95		14.95		14.95		
V_{IL}	Input Low Voltage # B Types	All	5	$V_O = 0.5V$ or 4.5V $V_O = 1.0V$ or 9.0V $V_O = 1.5V$ or 13.5V $\lvert I_O \rvert < 1\mu A$		1.5		1.5		1.5	Vdc
			10			3.0		3.0		3.0	
			15			4.0		4.0		4.0	
V_{IL}	Input Low Voltage # UB Types	All	5	$V_O = 0.5V$ or 4.5V $V_O = 1.0V$ or 9.0V $V_O = 1.5V$ or 13.5V $\lvert I_O \rvert < 1\mu A$		10		1.0		1.0	Vdc
			10			2.0		2.0		2.0	
			15			2.5		2.5		2.5	
V_{IH}	Input High Voltage # B Types	All	5	$V_O = 0.5V$ or 4.5V $V_O = 1.0V$ or 9.0V $V_O = 1.5V$ or 13.5V $\lvert I_O \rvert < 1\mu A$	3.5		3.5		3.5		Vdc
			10		7.0		7.0		7.0		
			15		11.0		11.0		11.0		
V_{IH}	Input High Voltage # UB Types	All	5	$V_O = 0.5V$ or 4.5V $V_O = 1.0V$ or 9.0V $V_O = 1.5V$ or 13.5V $\lvert I_O \rvert < 1\mu A$	4.0		4.0		4.0		Vdc
			10		8.0		8.0		8.0		
			15		12.5		12.5		12.5		
I_{OL}	Output Low (Sink) Current	Mil	5	$V_O = 0.4V$, $V_{IN} = 0$ or 5V	0.64		0.51		0.36		mAdc
			10	$V_O = 0.5V$, $V_{IN} = 0$ or 10V	1.6		1.3		0.9		
			15	$V_O = 1.5V$, $V_{IN} = 0$ or 15V	4.2		3.4		2.4		
		Com	5	$V_O = 0.4V$, $V_{IN} = 0$ or 5V	0.52		0.44		0.36		mAdc
			10	$V_O = 0.5V$, $V_{IN} = 0$ or 10V	1.3		1.1		0.9		
			15	$V_O = 1.5V$, $V_{IN} = 0$ or 15V	3.6		3.0		2.4		

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TABLE 1 – Continued

ELECTRICAL CHARACTERISTICS

PARAMETER		TEMP RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS						UNITS
					T_{LOW}*		+ 25°C		T_{HIGH}*		
					Min	Max	Min	Max	Min	Max	
I_{OH}	Output High (Source) Current	Mil	5	V_O = 4.6V, V_{IN} = 0 or 5V	-0.25		-0.2		-0.14		mAdc
			10	V_O = 9.5V, V_{IN} = 0 or 10V	-0.62		-0.5		-0.35		
			15	V_O = 13.5V, V_{IN} = o or 15V	-1.8		-1.5		-1.1		
		Com	5	V_O = 4.6V, V_{IN} = 0 or 5V	-0.2		-0.16		-0.12		mAdc
			10	V_O = 9.5V, V_{IN} = 0 or 10V	-0.5		-0.4		-0.3		
			15	V_O = 13.5V V_{IN} = 0 or 15V	-1.4		-1.2		-1.0		
I_{IN}	Input Current	Mil	15	V_{IN} = 0 or 15V		±0.1		±0.1		±1.0	µAdc
		Comm	15	V_{IN} = 0 or 15V		±0.3		±0.3		±1.0	µAdc
I_{oz}	3-State Output Leakage Current	Mil	15	V_{IN} = 0 or 15V		±0.4		±0.4		±12	µAdc
		Comm	15	V_{IN} = 0 or 15V		±1.6		±1.6		±12	µAdc
C_{IN}	Input Capacitance per unit load	All	–	Any Input				7.5			pF

*T_{LOW} = -55°C for Military temperature range device, -40°C for Commercial temperature range device.
T_{HIGH} = +125°C for Military temperature range device, +85°C for Commercial temperature range device.
#Applies for Worst Case input combinations.

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TABLE 2 – MOTOROLA FORMAT FOR CMOS INDUSTRY B AND UB SERIES SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}*		25°C		T_{high}*		Unit
				Min	Max	Min	Max	Min	Max	
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0			10	–	0.05	–	0.05	–	0.05	
			15	–	0.05	–	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}			10	9.95	–	9.95	–	9.95	–	
			15	14.95	–	14.95	–	14.95	–	
Input Voltage # B Types	"0" Level	V_{IL}								Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.5	–	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	–	3.0	–	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	4.0	–	4.0	–	4.0	
	"1" Level	V_{IH}								Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	3.5	–	3.5	–	3.5	–	
(V_O 1.0 or 9.0 Vdc)			10	7.0	–	7.0	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	11.0	–	11.0	–	11.0	–	
Input Voltage # UB Types	"0" Level	V_{IL}								Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.0	–	1.0	–	1.0	
(V_O = 9.0 or 1.0 Vdc)			10	–	2.0	–	2.0	–	2.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	2.5	–	2.5	–	2.5	
	"1" Level	V_{IH}								Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	4.0	–	4.0	–	4.0	–	
(V_O = 1.0 or 9.0 Vdc)			10	8.0	–	8.0	–	8.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	12.5	–	12.5	–	12.5	–	

TABLE 2 – Continued

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}*		25°C		T_{high}*		Unit
			Min	Max	Min	Max	Min	Max	
Output Drive Current (AL) B Gates	I_{OH}								mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	–	2.4	–	
Output Drive Current (CL/CP) B Gates	I_{OH}								mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	–	2.4	–	
Output Drive Current (AL) UB Gates	I_{OH}								mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	–	2.4	–	
Output Drive Current (CL/CP) UB Gates	I_{OH}								mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	–	2.4	–	
Output Drive Current (AL) Other Devices	I_{OH}								mAdc
(V_{OH} = 4.6 Vdc) Source		5.0	-0.25	–	-0.2	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	–	2.4	–	
Output Drive Current (CL/CP) Other Devices	I_{OH}								mAdc
(V_{OH} = 4.6 Vdc) Source		5.0	-0.2	–	-0.12	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	7.5	–	–	pF
Gate Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.25	–	7.5	μAdc
		10	–	0.5	–	0.5	–	15	
		15	–	1.0	–	1.0	–	30	
(CL/CP Device)	I_{DD}	5.0	–	1.0	–	1.0	–	7.5	μAdc
		10	–	2.0	–	2.0	–	15	
		15	–	4.0	–	4.0	–	30	

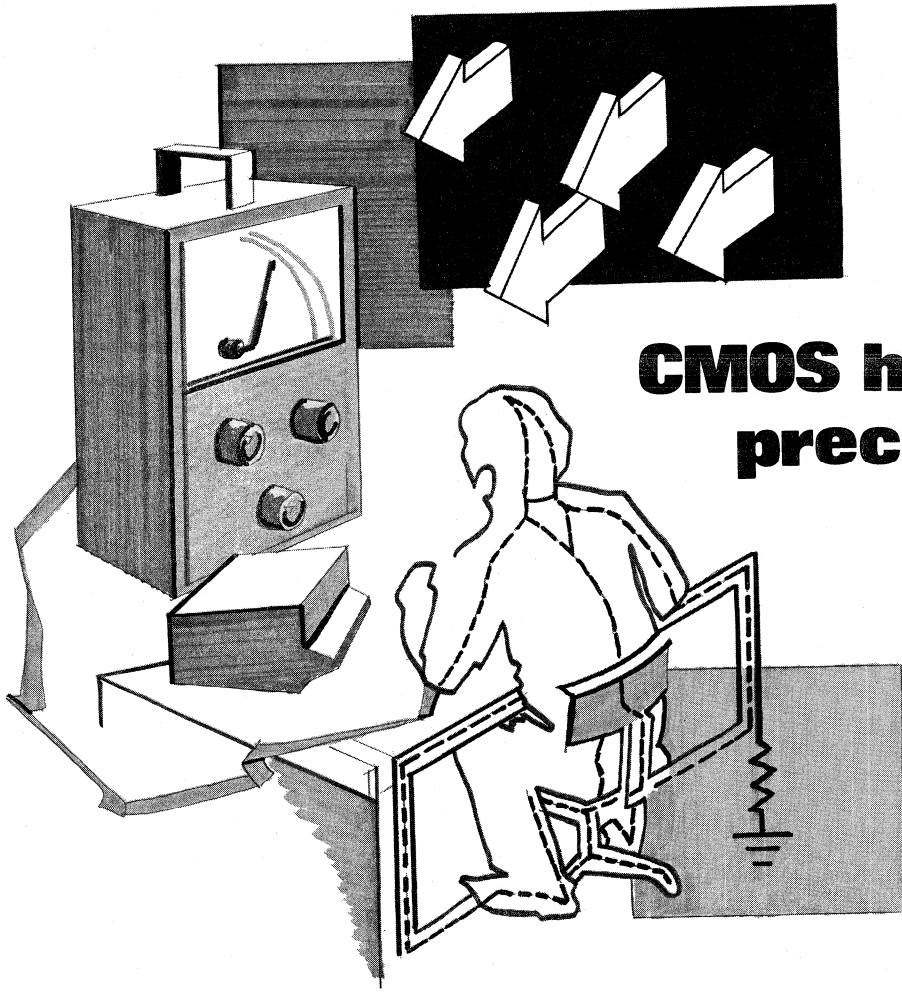
TABLE 2 – Continued

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}*		25°C		T_{high}*		Unit
				Min	Max	Min	Max	Min	Max	
Flip-Flop and Buffer Quiescent Current (Per Package)	(AL Device)	I_{DD}	5.0	–	1.0	–	1.0	–	30	μAdc
			10	–	2.0	–	2.0	–	60	
			15	–	4.0	–	4.0	–	120	
	(CL/CP Device)	I_{DD}	5.0	–	4.0	–	4.0	–	30	μAdc
			10	–	8.0	–	8.0	–	60	
			15	–	16	–	16	–	120	
MSI Quiescent Current (Per Package)	(AL Device)	I_{DD}	5.0	–	5.0	–	5.0	–	150	μAdc
			10	–	10	–	10	–	300	
			15	–	20	–	20	–	600	
	(CL/CP Device)	I_{DD}	5.0	–	20	–	20	–	150	μAdc
			10	–	40	–	40	–	300	
			15	–	80	–	80	–	600	
LSI Quiescent Current		I_{DD}		See Individual Data Sheets.						

* T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

6



CMOS handling precautions

HANDLING PROCEDURES FOR CMOS DEVICES

HANDLING PRECAUTIONS

Motorola CMOS devices have diode input protection against adverse electrical environments such as electrostatic discharge. In regards to this, the following statement is included on each data sheet:

> This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Unfortunately, severe electrical transient voltages can be generated during handling. For example, static voltages generated by a person walking across a common waxed floor have been measured in the 4 to 15 kV range (depending on humidity, surface conditions, etc.) These static voltages are potentially dangerous when discharged into a CMOS input, considering the energy stored in the capacity ($\approx$ 300 pF) of the human body at these voltage levels.

Present CMOS gate protection structures can generally protect against overvoltages. This is usually sufficient except in the severe cases.

The input protection circuit, while adding some delay time, provides protection by clamping positive and negative potentials to V_{DD} and V_{SS}, respectively. Figure 1 shows the internal circuitry for the diode-resistor protection.

The input protection circuit consists of a series isolation resistor R_S, whose typical value is 1.5 KΩ, and diodes D1 and D2, which clamp the input voltages between the power supply pins V_{DD} and V_{SS}. Diode D3 is a distributed structure resulting from the diffusion fabrication of R_S.

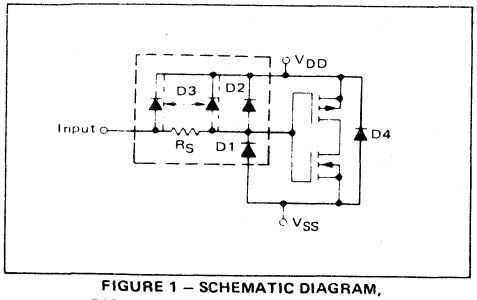


FIGURE 1 – SCHEMATIC DIAGRAM, DIODE-RESISTOR INPUT PROTECTION

In addition to the internal protection network, the following steps are recommended to further reduce damage to CMOS integrated circuits due to improper handling.

1. All CMOS devices should be stored or transported in materials that are antistatic. CMOS devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.

2. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 2.

3. Nylon or other static generating materials should not come in contact with CMOS circuits.

4. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices or boards. Avoid this by grounding suspect areas and/or by the use of ionized air blowers.

5. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.

6. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.

7. The following steps should be observed during wave solder operations.
   a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
   b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
   c. Operators must comply with precautions previously explained.
   d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.

8. The following steps should be observed during board cleaning operation.
   a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.

b. Brush or spray cleaning should not be used.
c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
d. Cleaned assemblies should be placed in antistatic container immediately after removal from the cleaning basket.
e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.

9. The use of static detection meters for line surveillance is highly recommended.

10. All low impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the CMOS is powered up. Similarly, this type of equipment should be disconnected before power is turned off.

11. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.

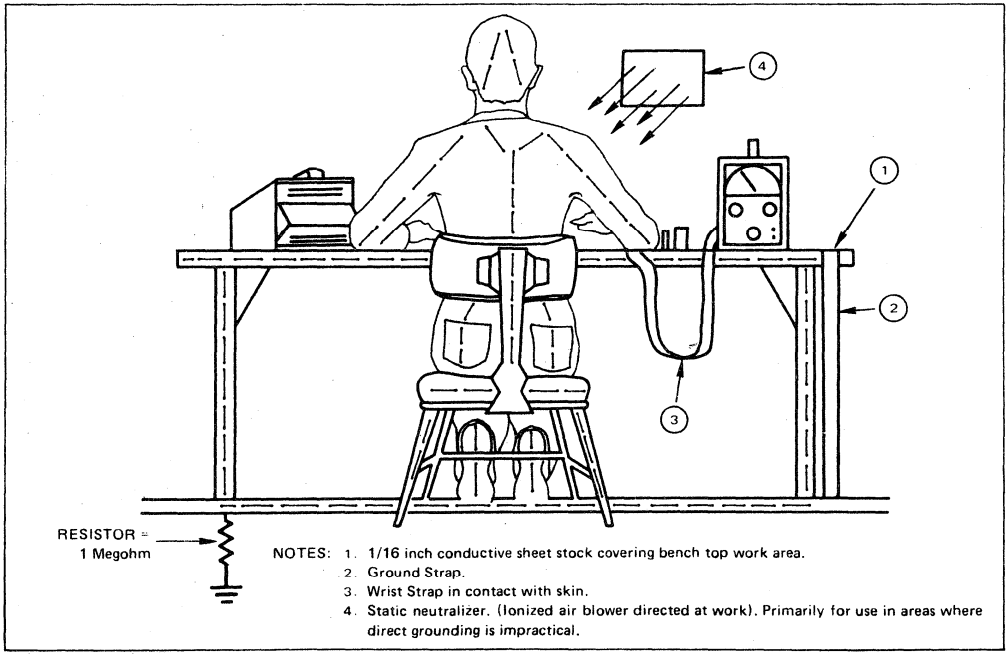
12. A circuit board containing CMOS devices is merely an extension of the device and the same handling precautions apply. Contacting edge connectors wired directly to CMOS device inputs can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address only an input of a CMOS integrated circuit, it is recommended that a resistance or 10 KΩ or greater be used in series with the input. This resistor will limit accidental damage if the PC board is removed and brought into contact with static generating materials.

13. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing CMOS devices to be certain there are no voltage transients present.

14. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.

15. Do not exceed the maximum electrical voltage ratings specified by the data sheet.

16. All unused device inputs should be connected to V_{DD} or V_{SS}.



NOTES: 1. 1/16 inch conductive sheet stock covering bench top work area.
2. Ground Strap.
3. Wrist Strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work). Primarily for use in areas where direct grounding is impractical.

FIGURE 2 – TYPICAL MANUFACTURING WORK STATION

Another type of precaution involves the CERDIP package. Since this device employs a glass seal, a high stress on the leads can cause hermeticity failure which will eventually result in aluminum corrosion on the die. To avoid this, the leads should never be flexed above the seating plane. All insertion tools or automated equipment should contact the lead at its narrowest dimension allowing it to bend without affecting the wide portion above the seating plane.

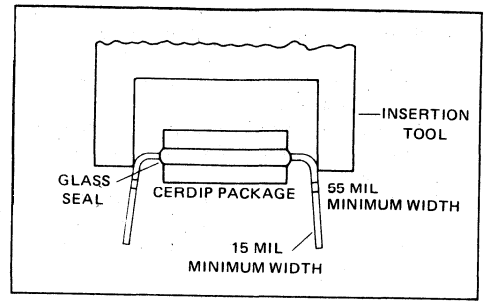
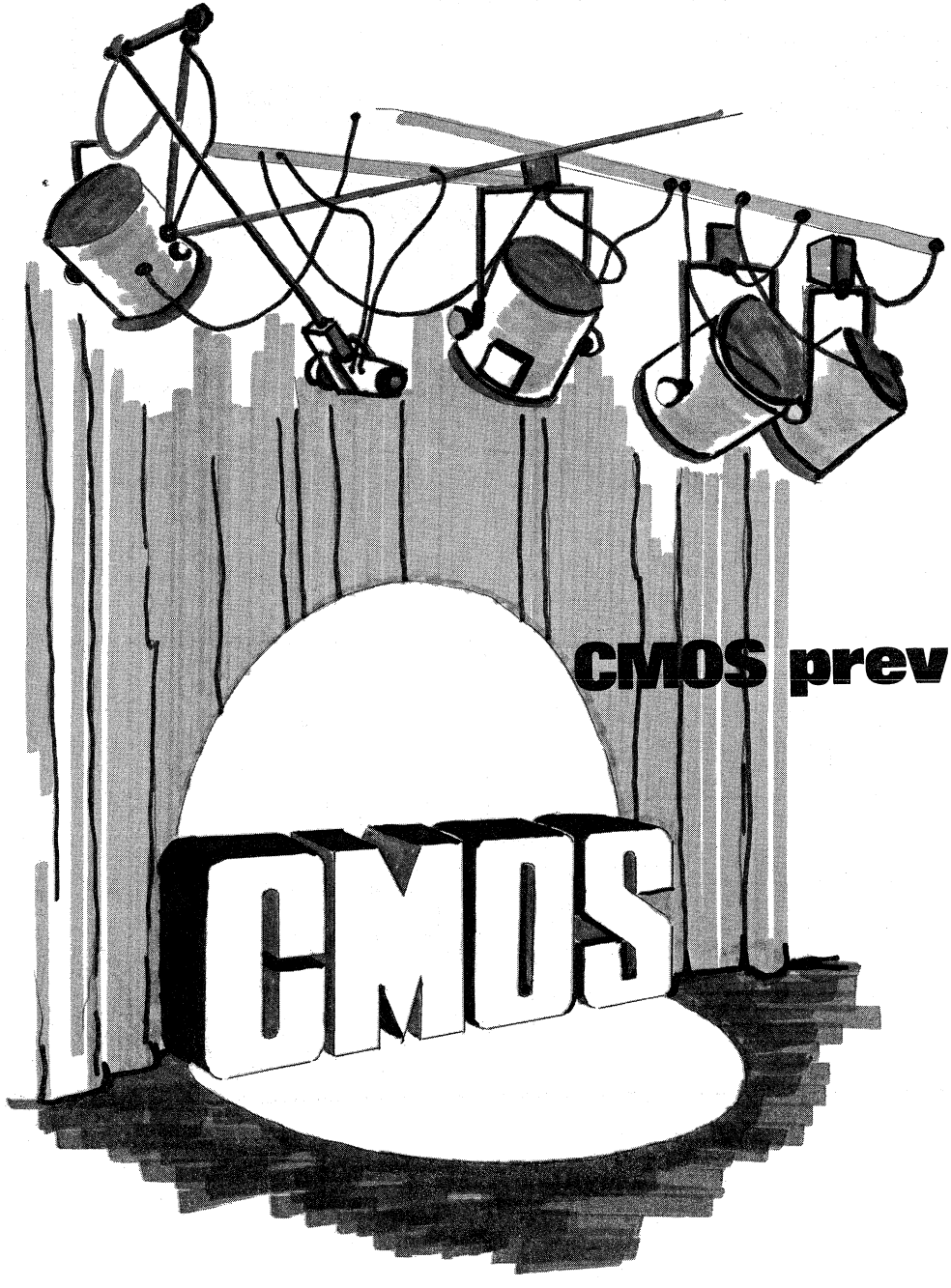


FIGURE 3 – CERDIP INSERTION PRECAUTIONS



CMOS previews 8

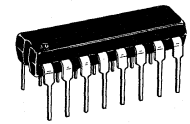
MC14413

PCM FILTER

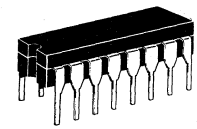
This device is designed to be used in PCM Codec based digital switching systems.

- Includes both transmit + receive filters
- Low power consumption
- Power down capability
- Wide dynamic range
- On chip clock generation

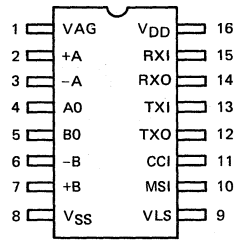
CMOS LSI
(LOW POWER COMPLEMENTARY MOS)

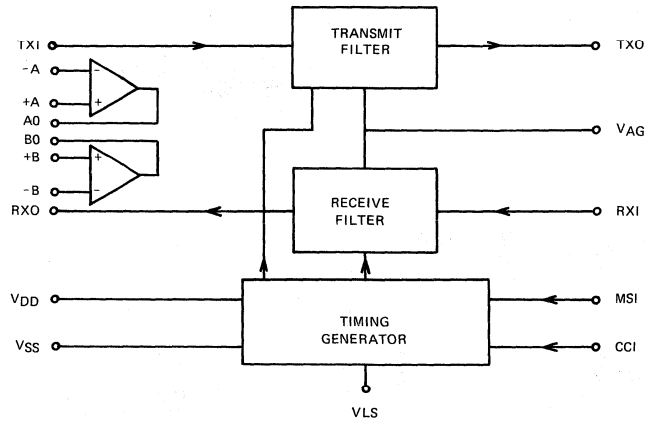


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620





8

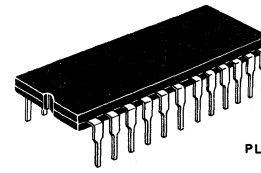
Product Preview

MC14421

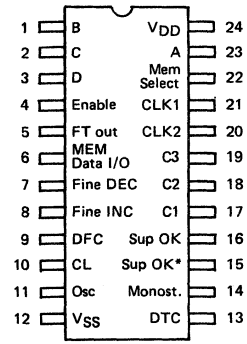
TV INTERFACE CIRCUIT

CMOS LSI
(LOW POWER COMPLEMENTARY MOS)

- Can be used in conjunction with the MC144102 and SMA2001 memory circuits
- Binary coded program address inputs
- Fine tuning value memorised on all channels
- Directly expandable to 32 channels



P SUFFIX
PLASTIC PACKAGE
CASE 623



8

Product Preview

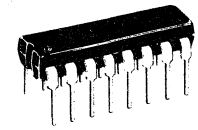
MC14466

LOW COST SMOKE DETECTOR

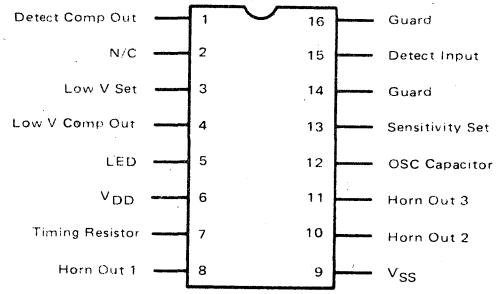
CMOS MSI

(LOW POWER COMPLEMENTARY MOS)

- Ionization Type with On Chip FET
- Piezoelectric Horn Driver
- Guard Outputs on Both Sides of Detect Input
- Low Battery Trip Point Internally Set Can Be Altered Via External Resistor
- Detect Threshold Internally Set Can Be Altered Via External Resistor
- Pulse Testing for Low Battery Uses LED for Battery Loading
- Comparator Outputs for Detect and Low Battery



P SUFFIX
PLASTIC PACKAGE
CASE 648



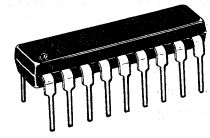
8

MC14497

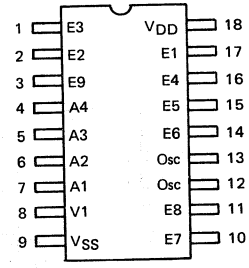
PCM REMOTE CONTROL TRANSMITTER

CMOS LSI
(LOW POWER COMPLEMENTARY MOS)

- Uses either FSK or AM modulation
- Can be used with MC6201/2/3 and MC6215 receiver circuits
- 62 channels/up to 62 keys
- 455 kHz reference oscillator
- Very low duty cycle
- Very low standby current
- Output interfaceable with IR transmitter
- Start bit polarity selectable



P SUFFIX
PLASTIC PACKAGE
CASE 707



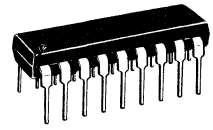
8

MC14499

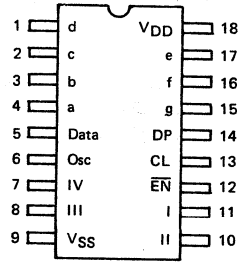
FOUR DIGIT MULTIPLEXED SEVEN SEGMENT DECODER DRIVER

- Synchronous serial data input
- High current output
- Intended for use in microprocessor applications
- Internal RC oscillator/scanner
- 3 data bus lines clock, data and chip enable
- 16 bits for digit display
- 4 bits for decimal point
- Decimal point/cascading device facility

CMOS MSI
(LOW POWER COMPLEMENTARY MOS)



P SUFFIX
PLASTIC PACKAGE
CASE 707



8

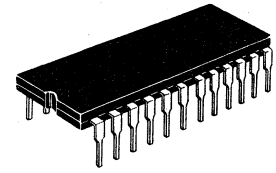
MC144100

DUPLEX 32 SEGMENT DRIVER

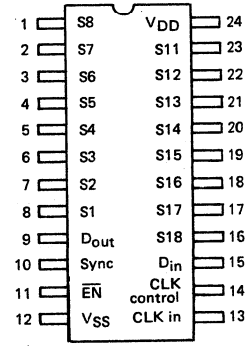
CMOS MSI

(LOW POWER COMPLEMENTARY MOS)

- Intended for use as a 4 digit LED display driver in microprocessor controlled, mains powered, clock/radio applications
- Three data bus lines: clock, data and chip enable
- NPN output drivers on chip
- Data serial in serial out
- Devices can be cascaded



P SUFFIX
PLASTIC PACKAGE
CASE 623



8

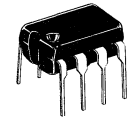
MCM144102

16 BIT/16 WORD STATIC RAM

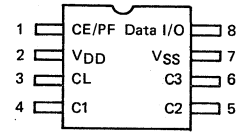
CMOS MSI

(LOW POWER COMPLEMENTARY MOS)

- 3 data bus lines, data I/O, chip select and clock input
- Directly expandable to 32 words
- Low power consumption in standby mode
- Compatible with non volatile memory SMA2001
- Clock frequency 0 to 100 kHz



P SUFFIX
PLASTIC PACKAGE
CASE 626



8

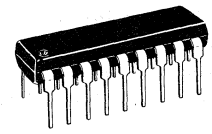
Product Preview

MC144110

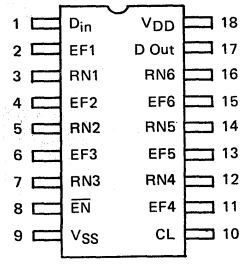
HEX STATIC D/A CONVERTER

CMOS LSI
(LOW POWER COMPLEMENTARY MOS)

- Six bit resolution
- Outputs analogue control voltages for use in TV and radio applications
- Six emitter follower outputs
- MPU compatible input level
- Serial data input
- Cascade data output



P SUFFIX
PLASTIC PACKAGE
CASE 707

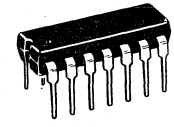


MC144111

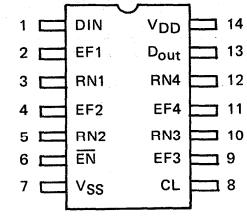
QUAD STATIC D/A CONVERTER

CMOS MSI
(LOW POWER COMPLEMENTARY MOS)

- Six bit resolution
- Outputs analogue control voltages for use in TV and radio applications
- Four emitter follower outputs
- MPU compatible input level
- Serial data input
- Cascade data output



P SUFFIX
PLASTIC PACKAGE
CASE 646



Product Preview

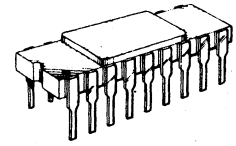
MCM146514

1 K X 4 STATIC RAM

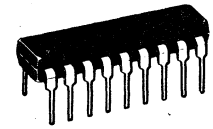
CMOS LSI

(LOW POWER COMPLEMENTARY MOS)

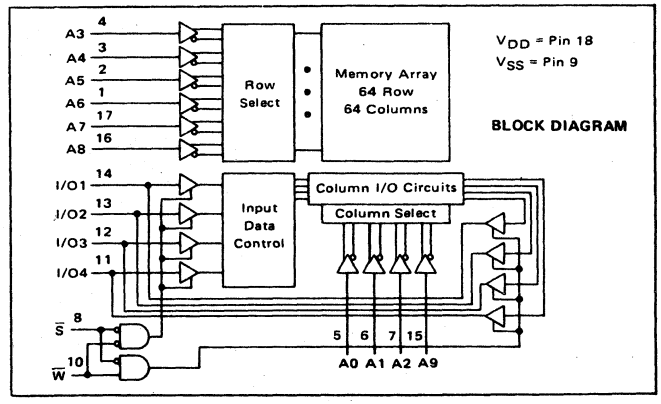
- 1024 Words by 4-Bit Organization
- Industry Standard 18-Pin Configuration
- Single Supply – 5 Volt Operation
- Fully Static – No Clocks or Refresh Required



L SUFFIX
CERAMIC PACKAGE
CASE 680



P SUFFIX
PLASTIC PACKAGE
CASE 707



Product Preview

MC146805 Series

MICROPROCESSORS/MICROCOMPUTERS

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

CONFIGURATION FEATURES:

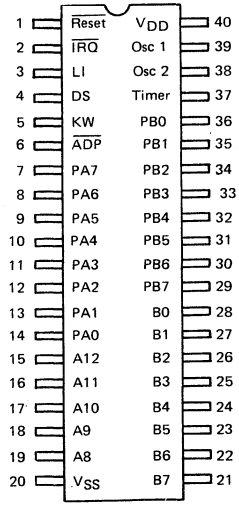
- CMOS Microprocessors and Microcomputers
  - Low Power Operation
  - Very Low Power in Standby
  - 3.0 to 6.0 Volt Power Supply
- On-Chip RAM
  - 64 Byte Option
  - 112 (128-16 I/O) Byte Option
- On-Chip ROM
  - 2K Byte Option
  - 1.1K (1K + 128 = 1152) Byte Option
  - No ROM Option
- External Interrupt
- Timer/Counter
  - 8 Bits Programmable
  - 7-Bit Prescaler
  - External or Internal Clock
  - Time-Out Interrupt
- I/O Ports
  - 2-1/2 Port (20 Line) Option – 28 Pins
  - 4 Port (32 Line) Option – 40 Pins
  - Each Line May Be Input or Output
- 4.0 MHz Oscillator – 1.0 MHz Cycle
- Other I/O Options Are Planned Within the Digital and Linear Capabilities of CMOS

SOFTWARE FEATURES:

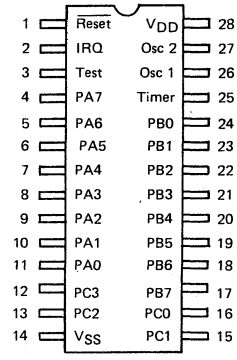
- Software Compatible with NMOS MC6805
- Programming Similar to MC6800
- RAM, ROM and I/O Use the Same Addressing Modes
  - Powerful Access to All Data
  - Look-Up Tables in ROM
  - Special I/O Instructions Not Needed
- Bit Manipulation of I/O and RAM
- Index Register – Powerful Indexed Addressing
- Stack Pointer – For Multilevel Subroutining
- Memory Modification Instructions – Increment, Decrement, Shift, Rotate, Complement, Negate, and Clear
- Less Code Per Function
  - Program Quicker
  - Change Easier
  - More Reliable

MC146805E2	**MC146805F2**	**MC146805G2**
40 pins	28 pins	40 pins
Expansion Bus	No Expansion Bus	112 Bytes RAM
112 Bytes RAM	64 Bytes RAM	2304 Bytes of ROM
No ROM	1.1 K ROM	32 I/O lines
16 I/O lines	20 I/O lines	

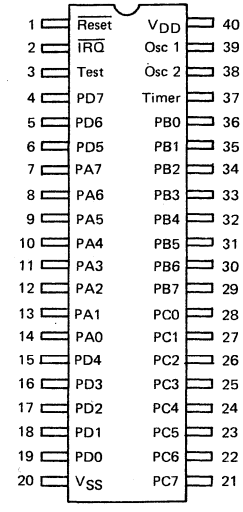
MC146805E2



MC146805F2



MC146805G2



Product Preview

MC146818/MC146819

REAL-TIME CLOCK/RAM

CMOS LSI

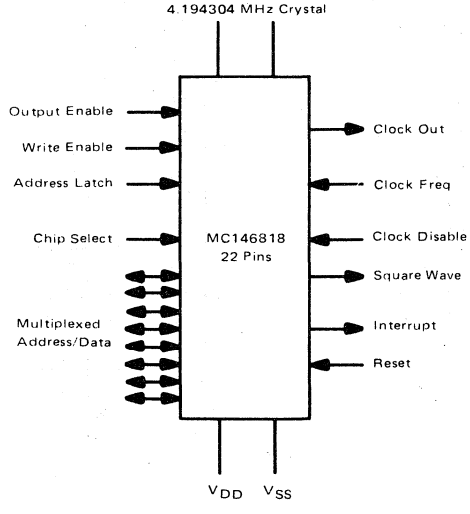
(LOW POWER COMPLEMENTARY MOS)

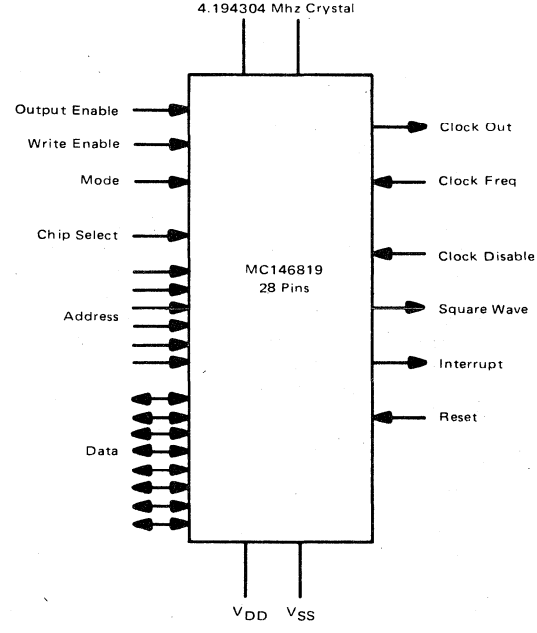
FEATURES:

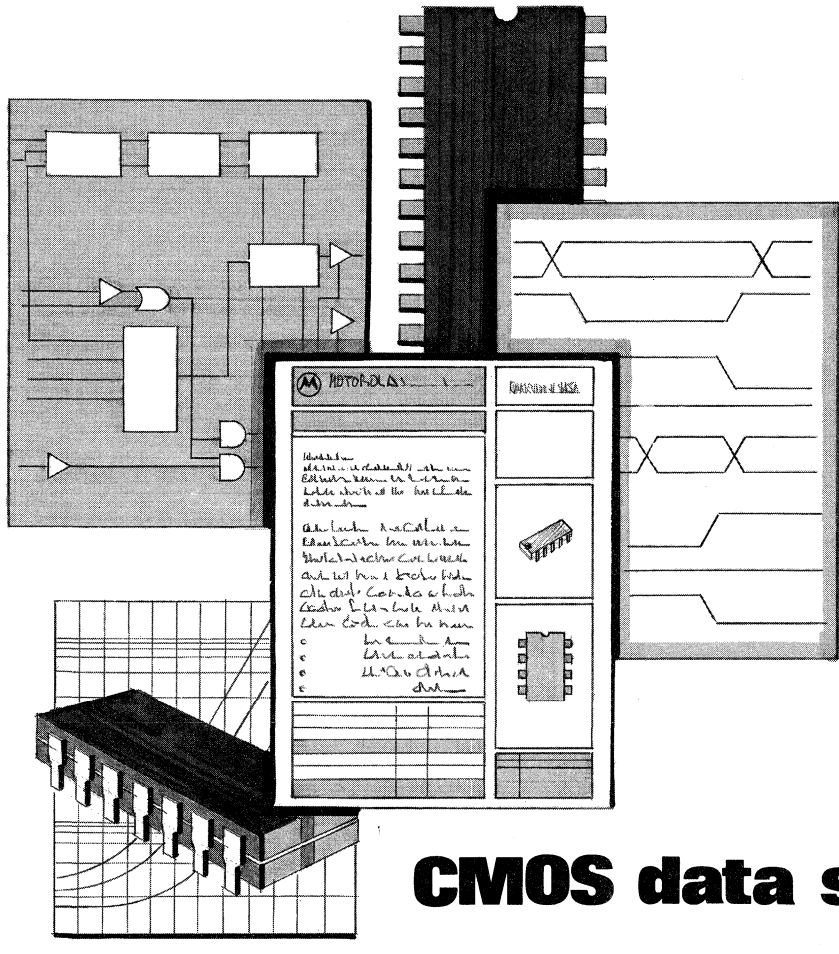
- Counts Seconds, Minutes, Hours, Days, Date, Month and Year
- Low Power CMOS Operation from 3.0 to 6.0 Volts
- Direct Microprocessor Interface
- MC146818 Is Multiplex Bus Compatible With MC146805, MC6801, 8085, 8048, and 8086
- MC146819 Is General-Purpose, Non-Multiplexed, Memory Type Interface
- 64 X 8 RAM – 12 Bytes for Clock, 52 Bytes for User Data Storage
- Interrupt to Microprocessor:
  Time of Day Alarm or
  Periodic Rates From 122 μs to 1 Hour
- Square Wave Output Signal at the Interrupt Rate
- Microprocessor Clock Output at 4 or 1 MHz
- Binary or BCD Time, Calender and Alarm
- 12 or 24 Hour Clock
- Leap Year
- Daylight Savings Time Option

APPLICATIONS:

- Battery Powered Clock and RAM for:
  NMOS Microprocessors (MC6800, 8080, etc.)
  NMOS Microcomputers (MC3870, 2000, etc.)
  CMOS Microprocessors (MC146805, etc.)
- Real-Time Data Collection
- Point of Sale
- Gas Pump Control
- Automatic Teller
- Small Business Machine
- Word Processing
- Data Entry (Form Fill-In)
- Time Clock
- Taxi Meter
- Heating and Cooling Control
- Home Computer
- Games
- Appliances







CMOS data sheets 9

MOTOROLA

MC14000UB

DUAL 3-INPUT "NOR" GATE PLUS INVERTER

The MC14000UB dual 3-input NOR gate plus inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4000UB

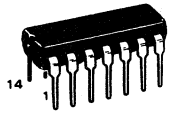
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 3-INPUT "NOR" GATE PLUS INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

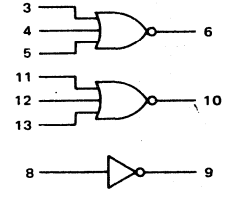
ORDERING INFORMATION

MC14XXXUB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

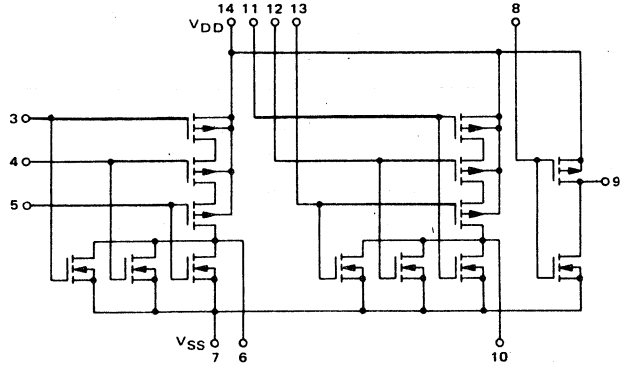
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

9

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5 Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0 Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	$I_T = (0.3\ \mu A/kHz)\ f + I_{DD}/N$							μAdc
		10	$I_T = (0.6\ \mu A/kHz)\ f + I_{DD}/N$							
		15	$I_T = (0.8\ \mu A/kHz)\ f + I_{DD}/N$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
0.5 Vdc min @ V_{DD} = 5.0 Vdc
1.0 Vdc min @ V_{DD} = 10 Vdc
1.0 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + N \times 10^{-3}(C_L - 50)V_{DD}f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency and N is number of gates per package.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns		5.0	–	115	230	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	–	55	110	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 15 ns		15	–	40	80	

*The formulas given are for the typical characteristics only.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

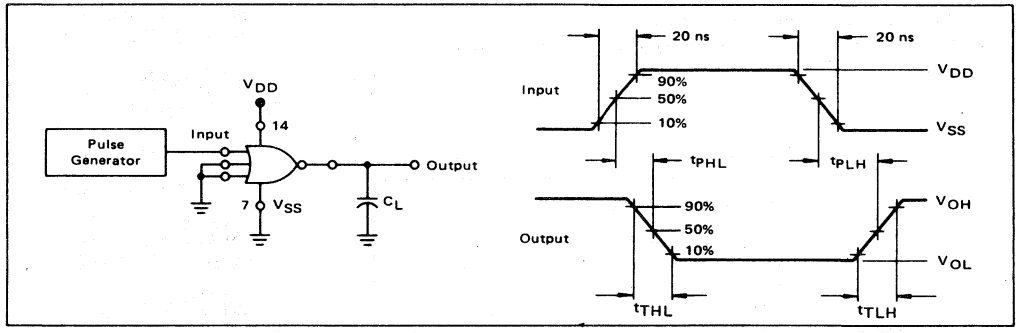


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

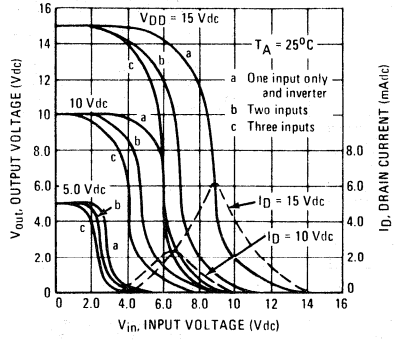
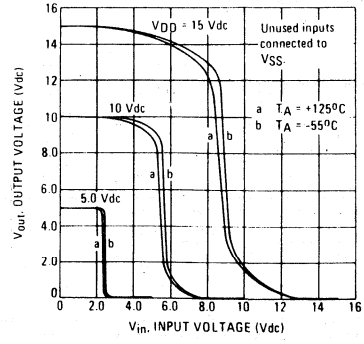


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE



9

MOTOROLA

MC14001B
Quad 2-Input NOR Gate

MC14002B
Dual 4-Input NOR Gate

MC14011B
Quad 2-Input NAND Gate

MC14012B
Dual 4-Input NAND Gate

MC14023B
Triple 3-Input NAND Gate

MC14025B
Triple 3-Input NOR Gate

MC14068B
8-Input NAND Gate

MC14071B
Quad 2-Input OR Gate

MC14072B
Dual 4-Input OR Gate

MC14073B
Triple 3-Input AND Gate

MC14075B
Triple 3-Input OR Gate

MC14078B
8-Input NOR Gate

MC14081B
Quad 2-Input AND Gate

MC14082B
Dual 4-Input AND Gate

B-SUFFIX SERIES CMOS GATES

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices

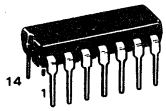
ORDERING INFORMATION

MC14XXXB — Suffix Denotes

- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

9

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

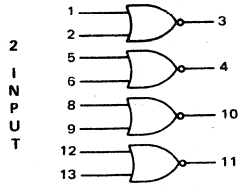
CMOS SSI

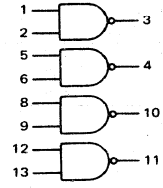
(LOW-POWER COMPLEMENTARY MOS)

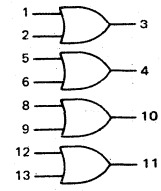
B-SERIES GATES

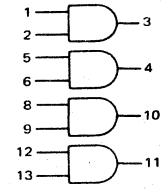
LOGIC DIAGRAMS

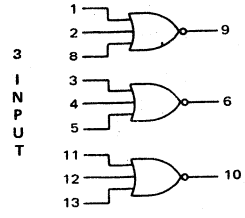
	NOR	NAND	OR	AND
2 INPUT	MC14001B Quad 2-Input NOR Gate	MC14011B Quad 2-Input NAND Gate	MC14071B Quad 2-Input OR Gate	MC14081B Quad 2-Input AND Gate
3 INPUT	MC14025B Triple 3-Input NOR Gate	MC14023B Triple 3-Input NAND Gate	MC14075B Triple 3-Input OR Gate	MC14073B Triple 3-Input AND Gate
4 INPUT	MC14002B Dual 4-Input NOR Gate	MC14012B Dual 4-Input NAND Gate	MC14072B Dual 4-Input OR Gate	MC14082B Dual 4-Input AND Gate
8 INPUT	MC14078B 8-Input NOR Gate	MC14068B 8-Input NAND Gate		

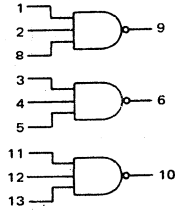


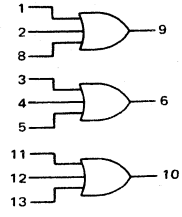


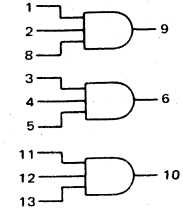


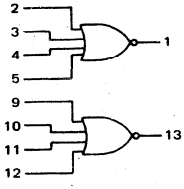


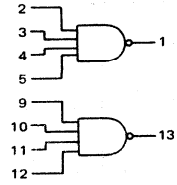


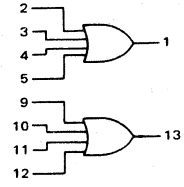


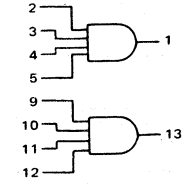


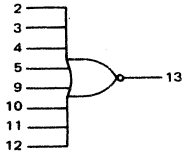


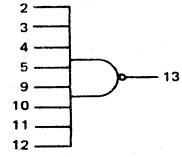












V_{DD} = Pin 14
V_{SS} = Pin 7
for All Devices

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0		1.5		2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10		3.0		4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15		4.0		6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5		3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15		±0.1		±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15		±0.3		±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–			5.0	7.5			pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0		0.25	–	0.0005	0.25	–	7.5	µAdc
		10		0.50	–	0.0010	0.50	–	15.0	
		15		1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0		1.0	–	0.0005	1.0	–	7.5	µAdc
		10		2.0	–	0.0010	2.0	–	15.0	
		15		4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}/N							µAdc
		10	I_T = (0.6 µA/kHz) f + I_{DD}/N							
		15	I_T = (0.9 µA/kHz) f + I_{DD}/N							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + N \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency and N is number of gates per package.
**The formulas given are for the typical characteristics only at 25°C.

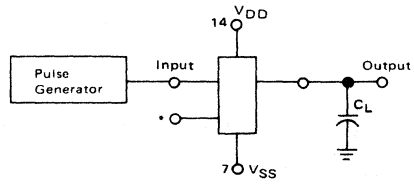
B-SERIES GATE SWITCHING TIMES

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

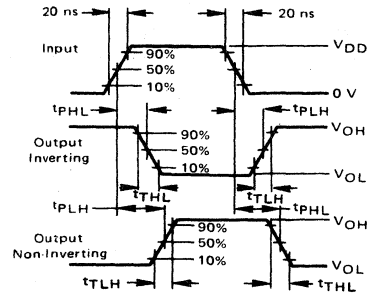
Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time, All B-Series Gates	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Output Fall Time, All B-Series Gates	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
MC14001B, MC14011B only						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 80 ns		5.0	–	125	250	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 32 ns		10	–	50	100	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 27 ns		15	–	40	80	
All Other 2, 3, and 4 Input Gates						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns		5.0	–	160	300	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns		10	–	65	130	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		15	–	50	100	
8-Input Gates (MC14068B, MC14078B)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 155 ns		5.0	–	200	350	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 62 ns		10	–	80	150	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	–	60	110	

*The formulas given are for the typical characteristics only.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

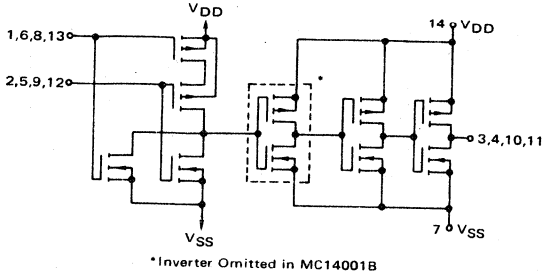


*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.



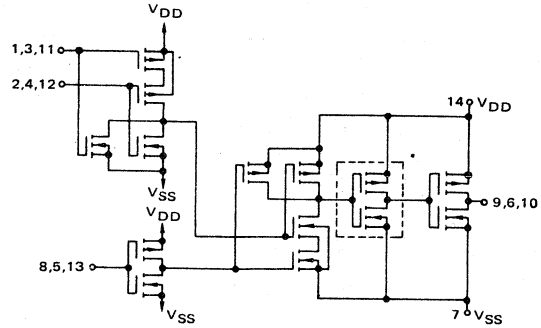
CIRCUIT SCHEMATIC
NOR, OR Gates

MC14001B
MC14071B
One of Four
Gates Shown



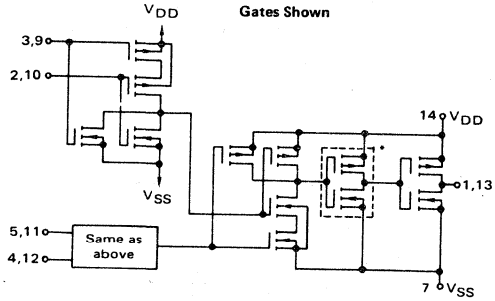
*Inverter Omitted in MC14001B

MC14025B
MC14075B
One of Three
Gates Shown



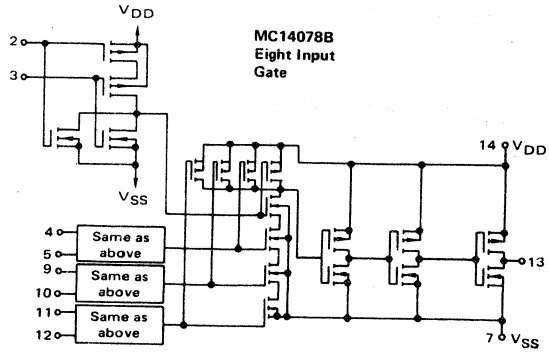
*Inverter Omitted in MC14025B

MC14002B
MC14072B
One of Two
Gates Shown



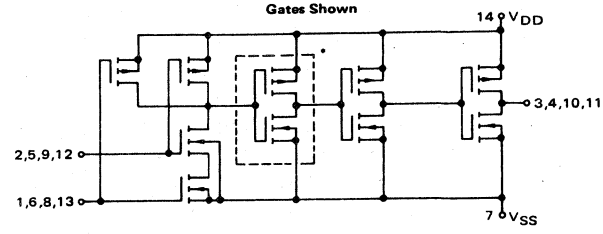
*Inverter Omitted in MC14002B

MC14078B
Eight Input
Gate



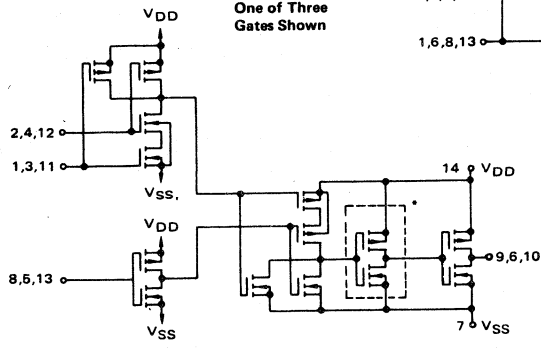
CIRCUIT SCHEMATICS
NAND, AND Gates

MC14011B
MC14081B
One of Four
Gates Shown



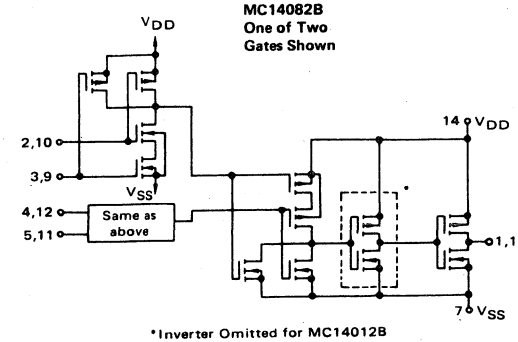
*Inverter Omitted in MC14011B

MC14023B
MC14073B
One of Three
Gates Shown



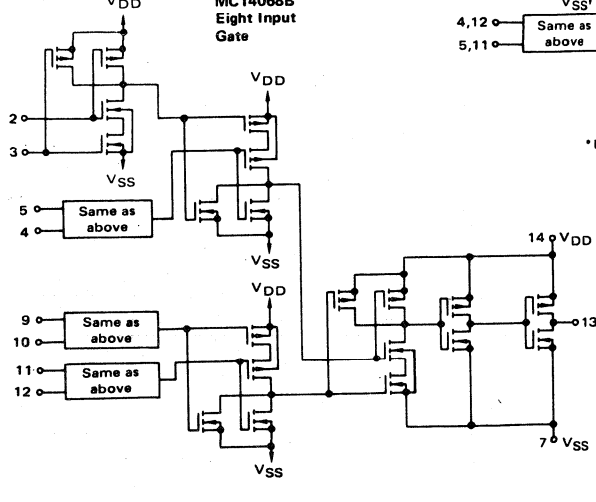
*Inverter Omitted in MC14023B

MC14012B
MC14082B
One of Two
Gates Shown



*Inverter Omitted for MC14012B

MC14068B
Eight Input
Gate



TYPICAL B-SERIES GATE CHARACTERISTICS

N-CHANNEL DRAIN CURRENT (SINK)

FIGURE 2 – V_{GS} = 5.0 Vdc

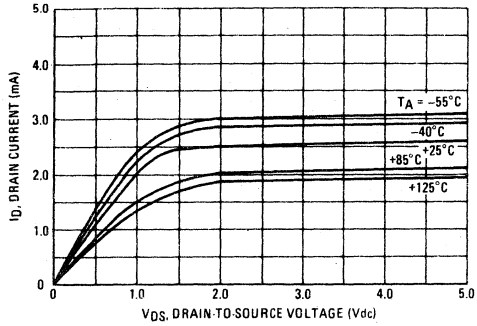


FIGURE 4 – V_{GS} = 10 Vdc

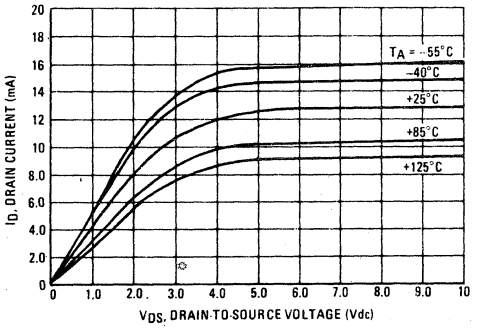
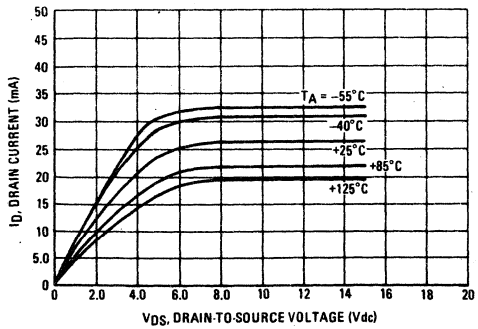


FIGURE 6 – V_{GS} = 15 Vdc



P-CHANNEL DRAIN CURRENT (SOURCE)

FIGURE 3 – V_{GS} = −5.0 Vdc

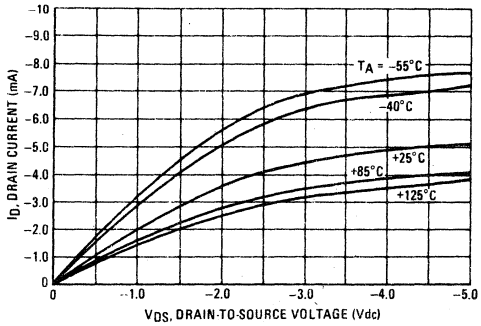


FIGURE 5 – V_{GS} = −10 Vdc

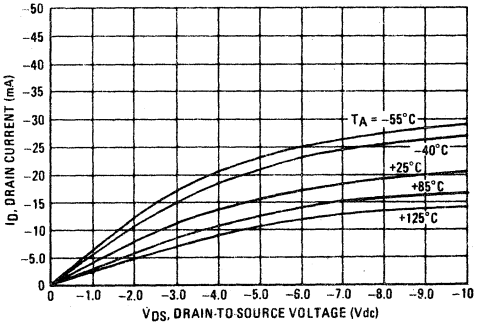
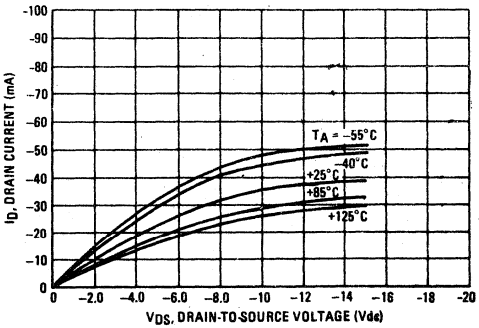


FIGURE 7 – V_{GS} = −15 Vdc



TYPICAL B-SERIES GATE CHARACTERISTICS (cont'd)

VOLTAGE TRANSFER CHARACTERISTICS

FIGURE 8 – V_{DD} = 5.0 Vdc

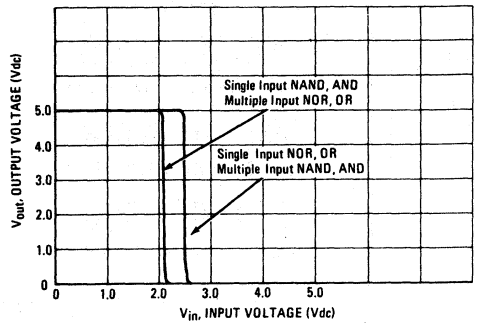


FIGURE 9 – V_{DD} = 10 Vdc

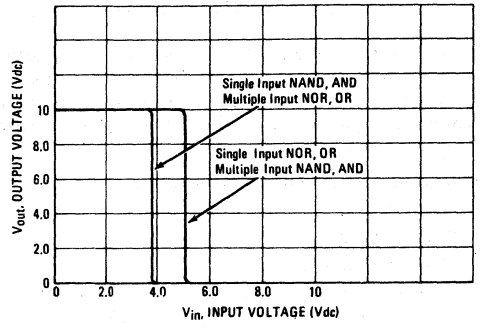
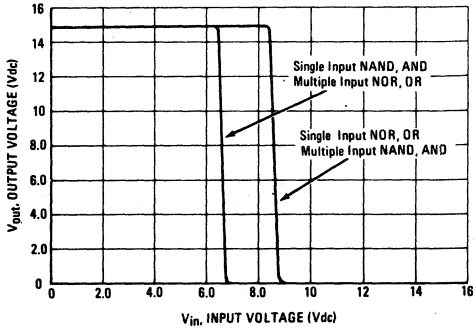


FIGURE 10 – V_{DD} = 15 Vdc

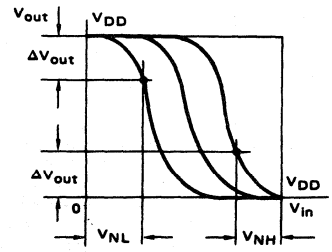


DC NOISE IMMUNITY (V_{NL} AND V_{NH})

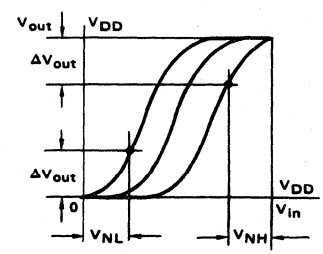
The dc noise immunity is defined as the input voltage range from an ideal "1" or "0" input level (assuming the previous CMOS driving state is unloaded which does not produce output state (combination) change(s). The typical and limit values of the input ranges V_{NL} and V_{NH} for the output to stay within a range ΔV_{out} from either V_{DD} or V_{SS} are given in the Electrical Characteristics table. The definitions of V_{NL}, V_{NH}, and ΔV_{out} are illustrated in Figure 11 for inverting and non-inverting functions.

FIGURE 11 – DC NOISE IMMUNITY

(a) Inverting Function



(b) Non-Inverting Function



V_{SS} = 0 volts dc

MOTOROLA

MC14001UB
Quad 2-Input NOR Gate

MC14002UB
Dual 4-Input NOR Gate

MC14011UB
Quad 2-Input NAND Gate

MC14012UB
Dual 4-Input NAND Gate

MC14023UB
Triple 3-Input NAND Gate

MC14025UB
Triple 3-Input NOR Gate

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

UB-SERIES GATES

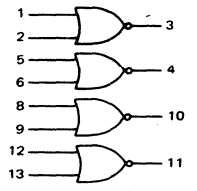
UB-SUFFIX SERIES CMOS GATES

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non-buffered functions.

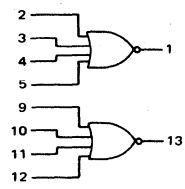
- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series UB Suffix Devices
- Formerly Listed without UB Suffix

LOGIC DIAGRAMS

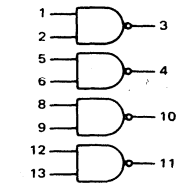
MC14001UB
Quad 2-Input NOR Gate



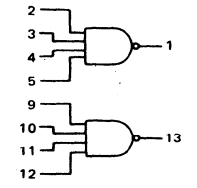
MC14002UB
Dual 4-Input NOR Gate



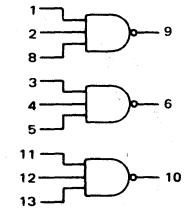
MC14011UB
Quad 2-Input NAND Gate



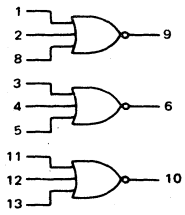
MC14012UB
Dual 4-Input NAND Gate



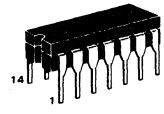
MC14023UB
Triple 3-Input NAND Gate



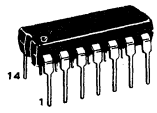
MC14025UB
Triple 3-Input NOR Gate



V_{DD} = Pin 14
V_{SS} = Pin 7
for All Devices



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXUB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5 Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0 Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}/N							µAdc
		10	I_T = (0.6 µA/kHz) f + I_{DD}/N							
		15	I_T = (0.8 µA/kHz) f + I_{DD}/N							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1"and "0" level =
0.5 Vdc min @ V_{DD} = 5.0 Vdc
1.0 Vdc min @ V_{DD} = 10 Vdc
1.0 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + N \times 10^{-3}(C_L - 50)V_{DD}f$$

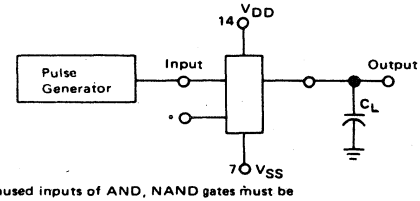
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency and N is number of gates per package.

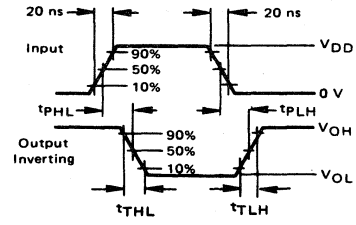
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns		5.0	–	90	180	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	–	50	100	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 15 ns		15	–	40	80	

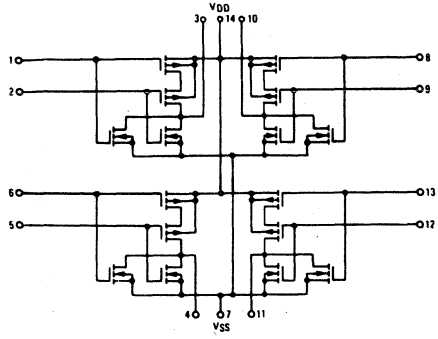
FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



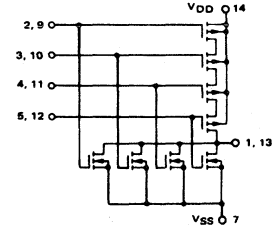


*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.

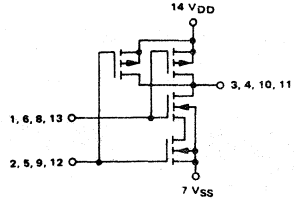
MC14001UB CIRCUIT SCHEMATIC



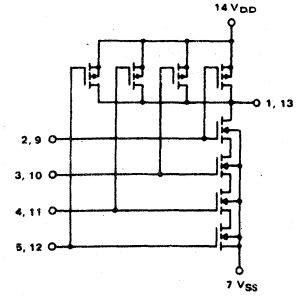
MC14002UB CIRCUIT SCHEMATIC
(1/2 of Device Shown)



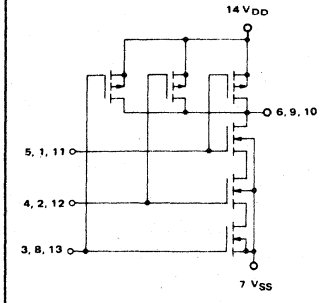
MC14011UB CIRCUIT SCHEMATIC
(1/4 of Device Shown)



MC14012UB CIRCUIT SCHEMATIC
(1/2 of Device Shown)



MC14023UB CIRCUIT SCHEMATIC
(1/3 of Device Shown)



MC14025UB CIRCUIT SCHEMATIC
(1/3 of Device Shown)

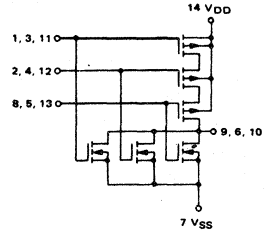


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

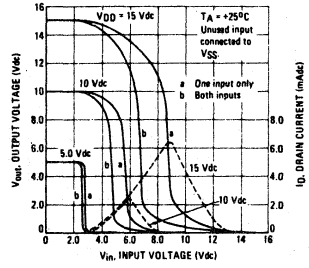


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

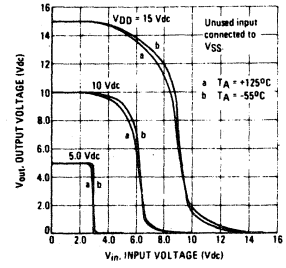


FIGURE 4 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

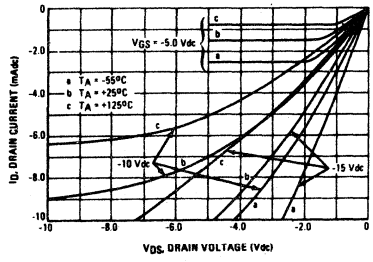
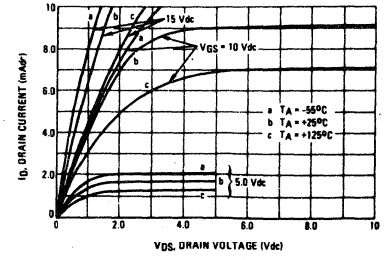


FIGURE 5 – TYPICAL OUTPUT SINK CHARACTERISTICS



MOTOROLA

MC14002B
MC14002UB

DUAL 4-INPUT "NOR" GATE

The MC14002B and MC14002UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14002B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14002B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4002B and CD4002UB

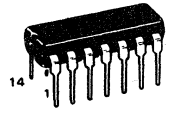
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

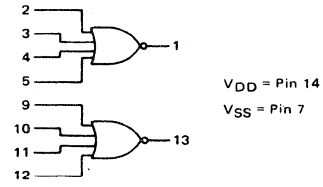
or UB as Applicable

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

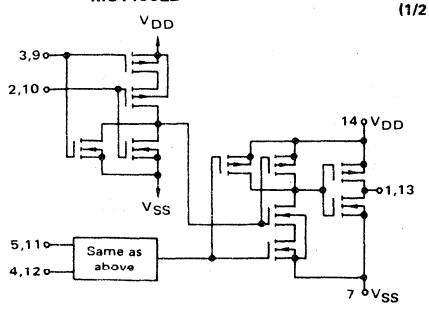
See the MC14001B data sheet for complete characteristics of the B-Series device.
See the MC14001UB data sheet for complete characteristics for the UB device.

LOGIC DIAGRAM

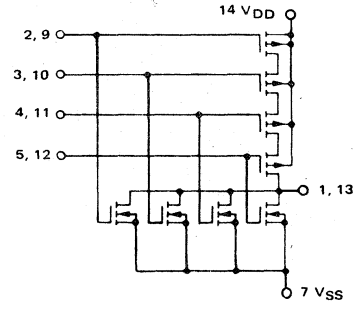


CIRCUIT SCHEMATICS
(1/2 of Device Shown)

MC14002B



MC14002UB



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14006B

CMOS MSI

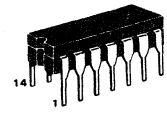
(LOW-POWER COMPLEMENTARY MOS)

18-BIT STATIC SHIFT REGISTER

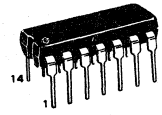
18-BIT STATIC SHIFT REGISTER

The MC14006B shift register is comprised of four separate shift register sections sharing a common clock: two sections have four stages, and two sections have five stages with an output tap on both the fourth and fifth stages. This makes it possible to obtain a shift register of 4, 5, 8, 9, 10, 12, 13, 14, 16, 17, or 18 bits by appropriate selection of inputs and outputs. This part is particularly useful in serial shift registers and time delay circuits.

- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Quiescent Current - 5nA/package typical @ 5 Vdc
- Fully Static Operation
- 8-MHz Shift Rate typical
- Can be Cascaded to Provide Longer Shift Register Lengths
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4006B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

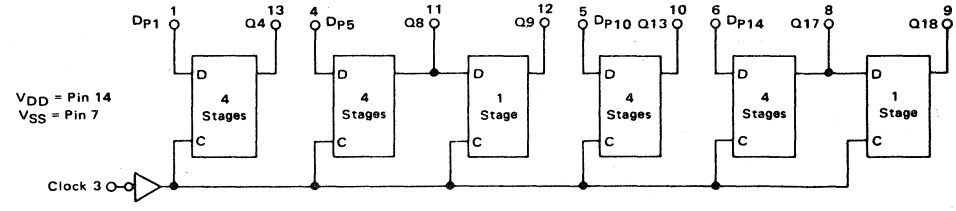
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE
(Single Stage)

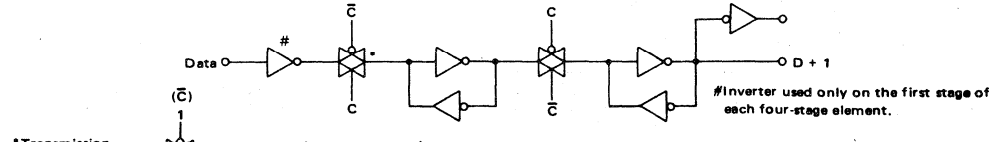
D_n	C	Q_{n+1}
0	⌐	0
1	⌐	1
X	⌐	Q_n

X = Don't Care

BLOCK DIAGRAM



LOGIC DIAGRAM
(ONE REGISTER STAGE)



*Transmission Gate

Input to output is
(A) A bidirectional low impedance when control input 1 is "low" and control input 2 is "high".
(B) An open circuit when control input 1 is "high" and control input 2 is "low".

#Inverter used only on the first stage of each four-stage element.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.3 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.6 µA/kHz) f + I_{DD}							
		15	I_T = (3.9 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 220 ns	t_{PHL}	5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 77 ns		10	–	110	220	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 55 ns		15	–	80	160	
Clock Pulse Width	t_{WH}	5.0	200	100	–	ns
		10	120	60	–	
		15	80	40	–	
Clock Pulse Frequency	f_{cl}	5.0	–	5.0	2.5	MHz
		10	–	8.3	4.2	
		15	–	12	6.0	
Clock Pulse Rise and Fall Time#	t_{TLH}	5.0	–	–	15	μs
	t_{THL}	10	–	–	15	
		15	–	–	15	
Setup Time	t_{su}	5.0	0	-50	–	ns
		10	0	-15	–	
		15	0	-8.0	–	
Hold Time	t_h	5.0	180	75	–	ns
		10	90	25	–	
		15	75	20	–	

*The formula given is for the typical characteristics only at 25°C.

#When shift register sections are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the rise and fall times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitance load.

FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

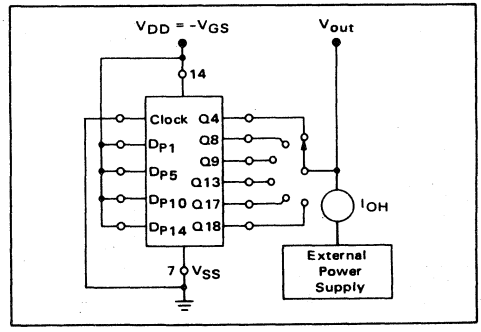


FIGURE 2 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT

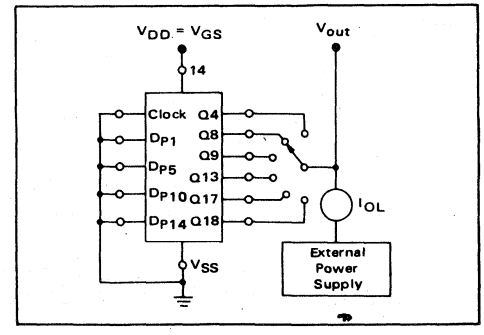


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

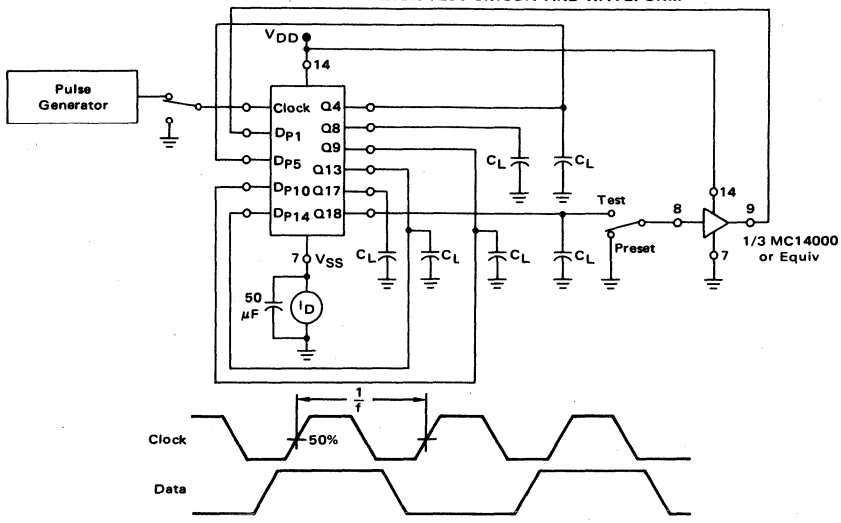
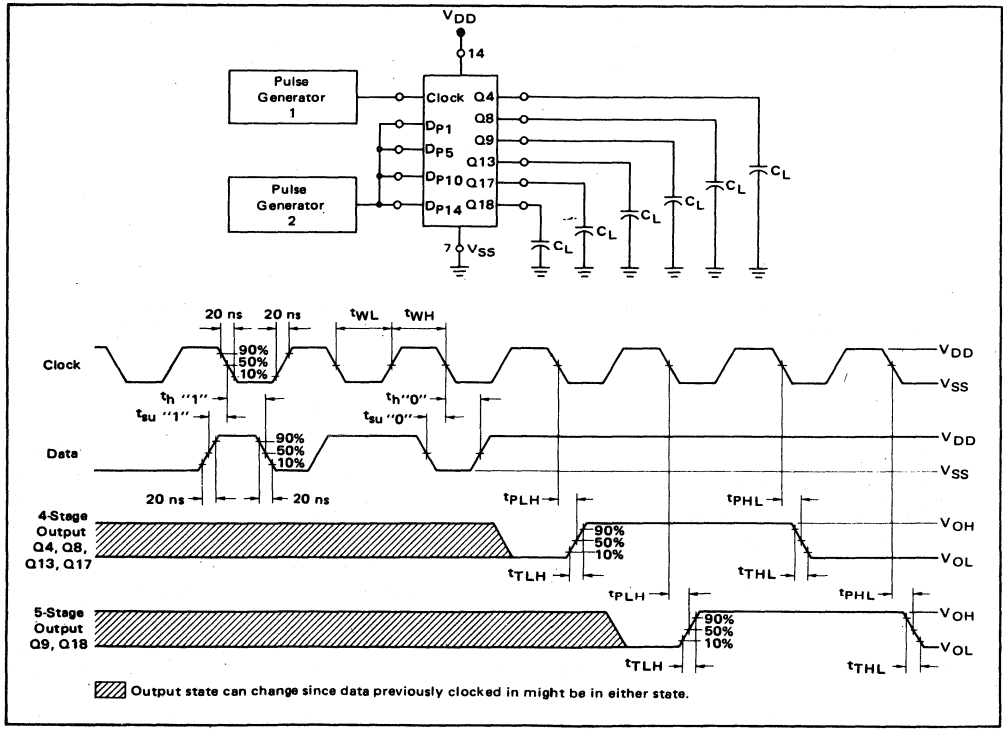


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MOTOROLA

MC14007UB

DUAL COMPLEMENTARY PAIR PLUS INVERTER

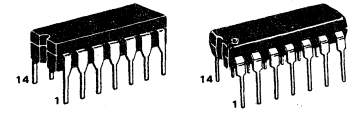
The MC14007UB multi-purpose device consists of three N-channel and three P-channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse-shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation = Positive or Negative
- Symmetrical Output Impedance — 200 ohms typical @ 10 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4007A or CD4007UB

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL COMPLEMENTARY PAIR PLUS INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

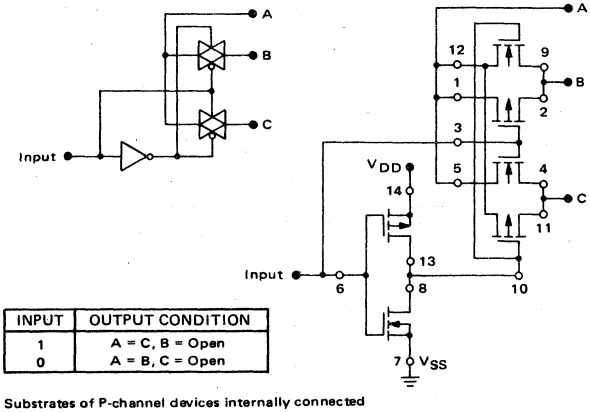
ORDERING INFORMATION

MC14XXXUB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

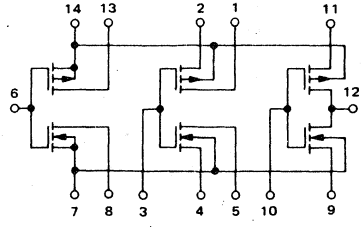
FIGURE 1 — TYPICAL APPLICATION: 2-INPUT ANALOG MULTIPLEXER



INPUT	OUTPUT CONDITION
1	A = C, B = Open
0	A = B, C = Open

Substrates of P-channel devices internally connected to V_{DD}; substrates of N-channel devices internally connected to V_{SS}.

SCHEMATIC



V_{DD} = Pin 14
V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS (Connected as Inverters)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-5.0	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-1.0	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.5	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-10	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	1.0	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.5	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	10	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-5.0	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-1.0	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.5	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-10	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	1.0	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.5	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	10	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)	I_T	5.0	I_T = (0.7 µA/kHz) f + I_{DD}/6							µAdc
		10	I_T = (1.4 µA/kHz) f + I_{DD}/6							
		15	I_T = (2.2 µA/kHz) f + I_{DD}/6							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device

†To calculate total supply current at loads other than 50 pF

$$I_T(C_L) = I_T(50\ pF) + 3 \times 10^{-3}(C_L - 50)V_{DD}f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

#Noise immunity specified for worst-case input combination. Noise Margin for both "1" and "0" level =
0.5 Vdc min @ V_{DD} = 5.0 Vdc
1.0 Vdc min @ V_{DD} = 10 Vdc
1.0 Vdc min @ V_{DD} = 15 Vdc

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.2 ns/pF) C_L + 30 ns		5.0	–	90	180	
t_{TLH} = (0.5 ns/pF) C_L + 20 ns		10	–	45	90	
t_{TLH} = (0.4 ns/pF) C_L + 15 ns		15	–	35	70	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.2 ns/pF) C_L + 15 ns		5.0	–	75	150	
t_{THL} = (0.5 ns/pF) C_L + 15 ns		10	–	40	80	
t_{THL} = (0.4 ns/pF) C_L + 10 ns		15	–	30	60	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.5 ns/pF) C_L + 35 ns		5.0	–	60	125	
t_{PLH} = (0.2 ns/pF) C_L + 20 ns		10	–	30	75	
t_{PLH} = (0.15 ns/pF) C_L + 17.5 ns		15	–	25	55	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.0 ns/pF) C_L + 10 ns		5.0	–	60	125	
t_{PHL} = (0.3 ns/pF) C_L + 15 ns		10	–	30	75	
t_{PHL} = (0.2 ns/pF) C_L + 15 ns		15	–	25	55	

*The formula given is for the typical characteristics only.
Switching specifications are for device connected as an inverter.

FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

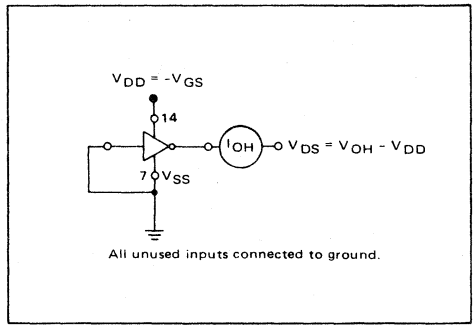
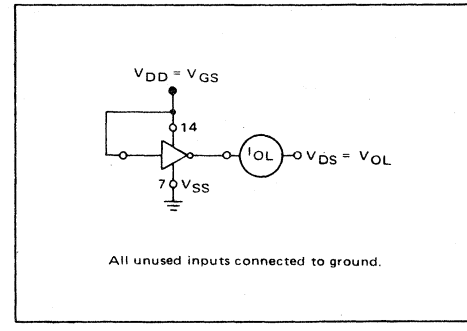
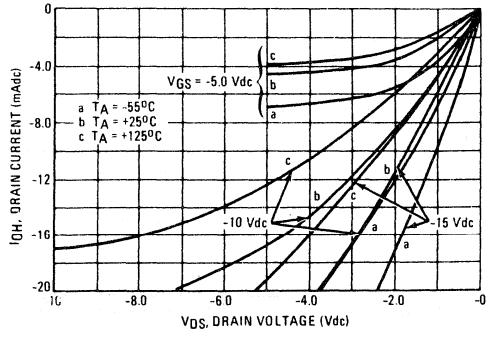


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS





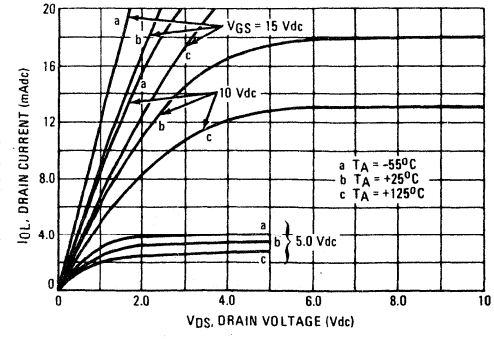
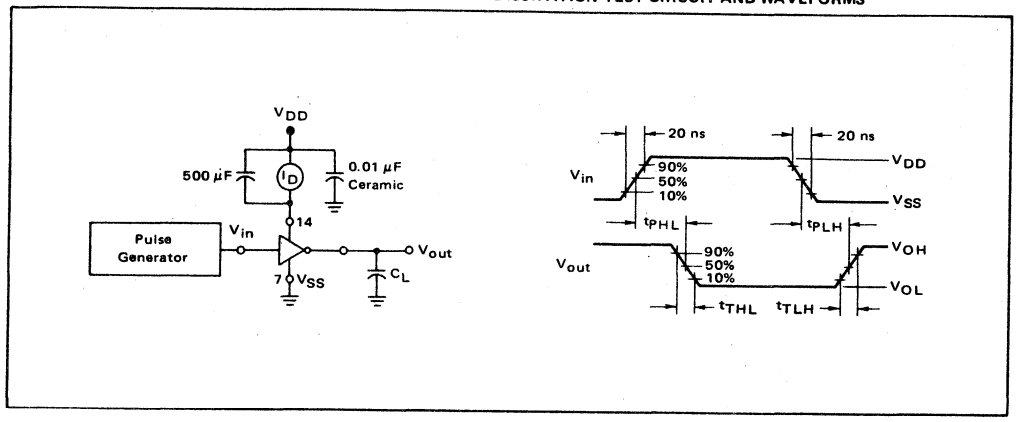


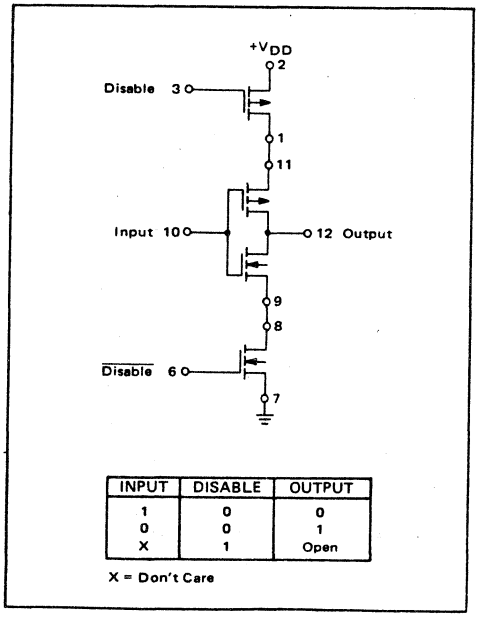
FIGURE 4 – SWITCHING TIME AND POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



APPLICATIONS

The MC14007UB dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 5, and 6 are a few examples of the device flexibility.

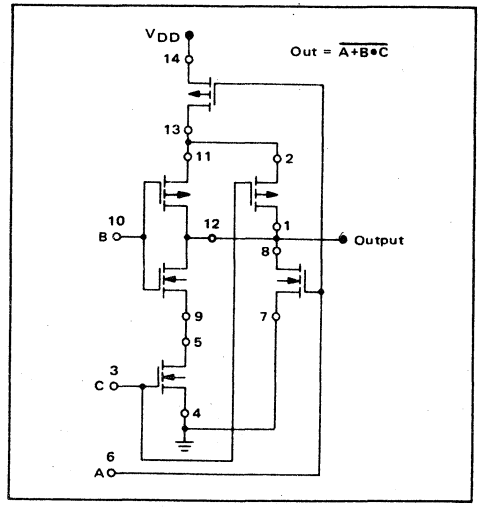
FIGURE 5 – 3-STATE BUFFER



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	Open

X = Don't Care

FIGURE 6 – AOI FUNCTIONS USING TREE LOGIC



Substrates of P-channel devices internally connected to V_{DD};
Substrates of N-channel devices internally connected to V_{SS}.

MOTOROLA

MC14008B

4-BIT FULL ADDER

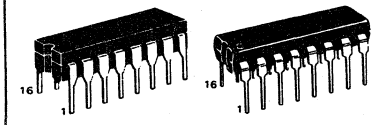
The MC14008B 4-bit full adder is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications.The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

- Look-Ahead Carry Output
- High-Speed Operation – 160 ns typical from Sum_{in} to Sum_{out}
- Quiescent Current – 5.0 nA/package typical @ 5 Vdc
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4008B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT FULL ADDER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

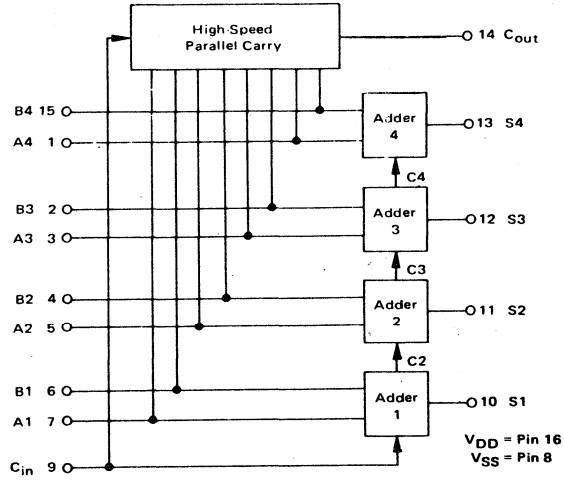
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



TRUTH TABLE
(One Stage)

C_{in}	B	A	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.7 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.4 μA/kHz) f + I_{DD}							
		15	I_T = (5.0 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time,	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time,	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Sum In to Sum Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 127 ns		10	–	160	320	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	–	115	230	
Sum In to Carry Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 220 ns		5.0	–	305	610	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 112 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Carry In to Sum Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 290 ns		5.0	–	375	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	–	155	310	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	–	115	230	
Carry In to Carry Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 85 ns		5.0	–	170	340	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 30 ns		15	–	55	110	

*The formula is for the typical characteristics only.

FIGURE 1 – TYPICAL SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

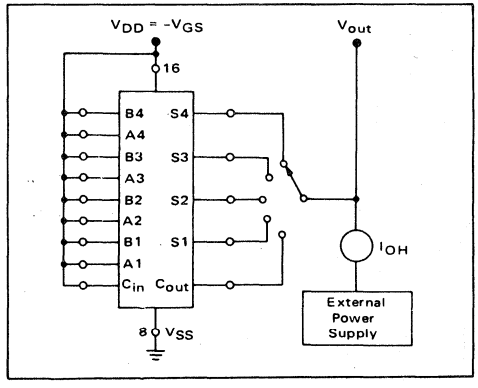


FIGURE 2 – TYPICAL SINK CURRENT CHARACTERISTICS TEST CIRCUIT

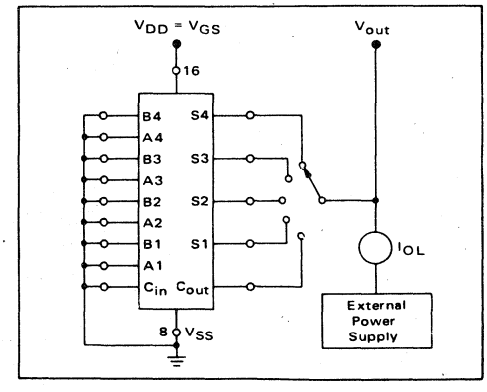


FIGURE 3 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

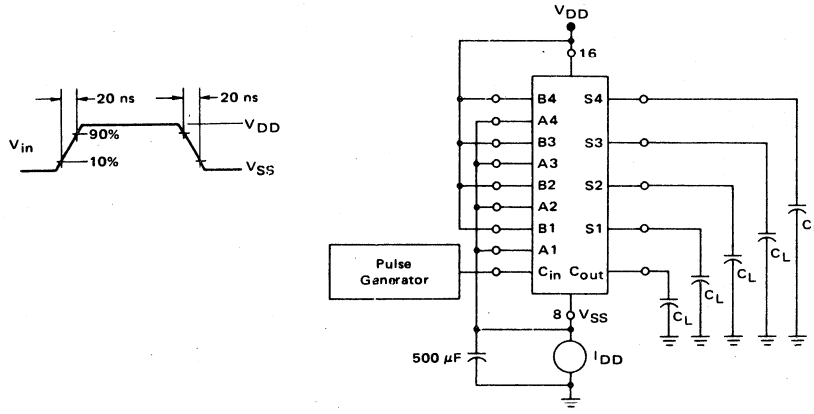


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

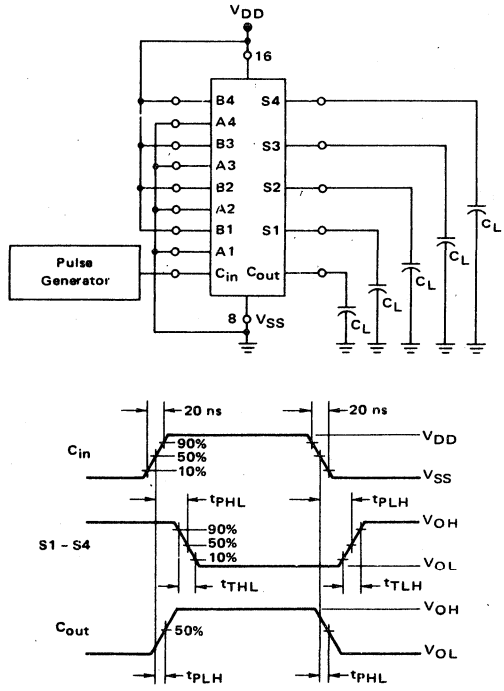
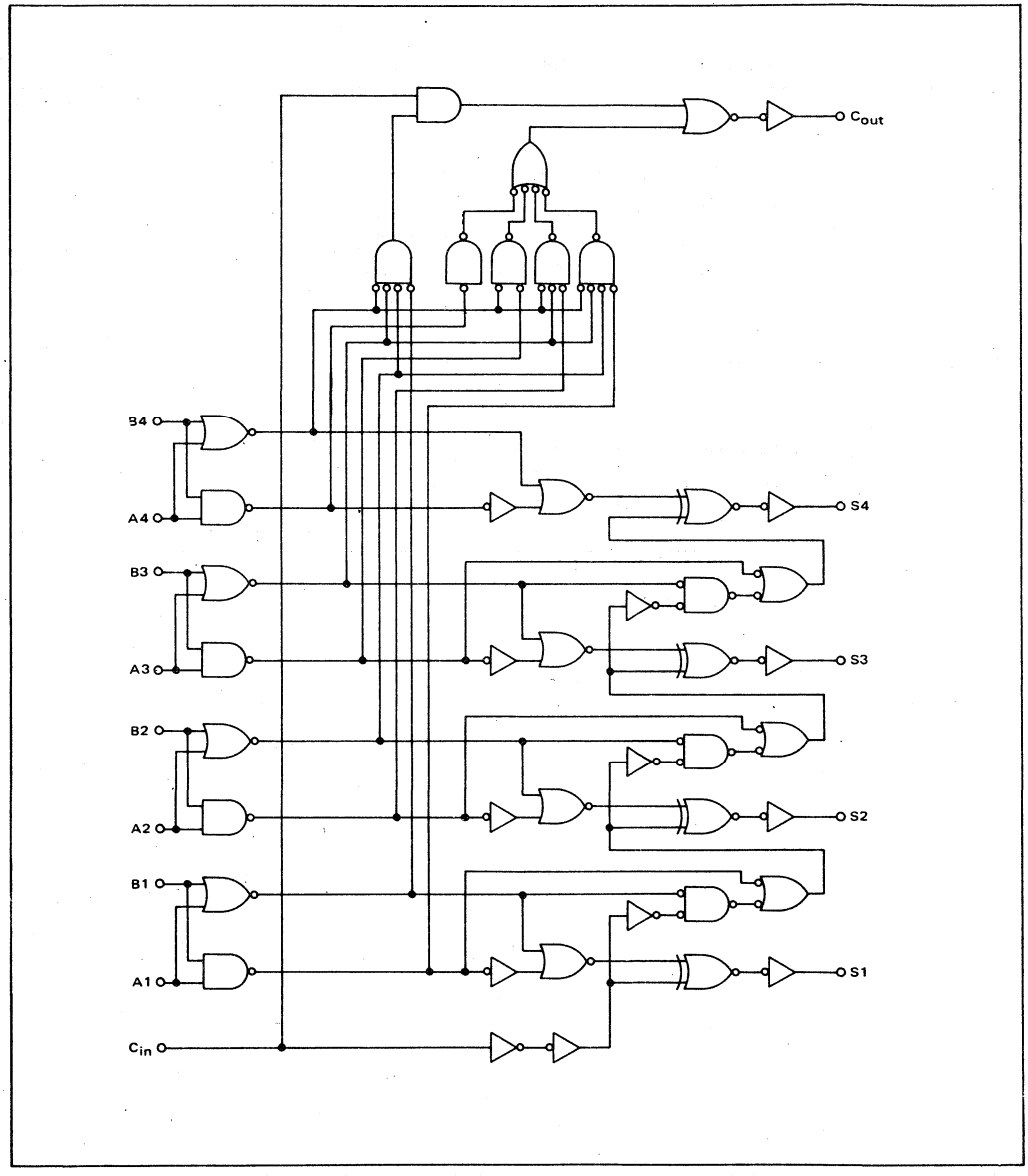
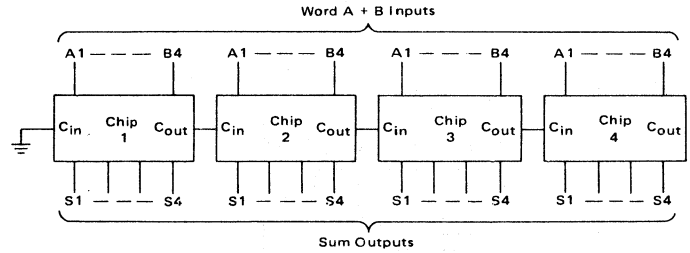


FIGURE 5 – LOGIC DIAGRAM



TYPICAL APPLICATION

FIGURE 6 – USING THE MC14008B IN A 16-BIT ADDER CONFIGURATION



Calculation of 16-bit adder speed:

t_p total = t_p (Sum to Carry) + t_p (Carry to Sum) + 2 t_p (Carry to Carry)

Typically, the overall 16-bit adder speed at 10 V is:

t_p total = 115 + 125 + 90 = 330 ns typ

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14009UB
MC14010B

HEX BUFFERS

The MC14009UB hex inverter/buffer and MC14010B noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. Both devices can be used as current "sink" or "source" drivers, as CMOS-to-CMOS or CMOS-to-TTL logic level converters, or as multiplexers (1-to-6). MC14049UB and MC14050B are preferred replacements for MC14009UB and MC14010B in buffer applications.

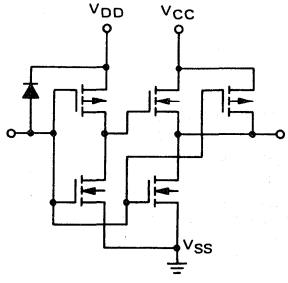
- High Source and Sink Currents
- Low-to-High Level Converter
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Meets JEDEC UB Specifications – MC14009UB
  Meets JEDEC B Specification – MC14010B

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to +18	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	45	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

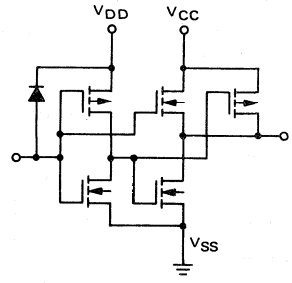
CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)

MC14009UB



All P-Channel substrates = V_{DD}

MC14010B



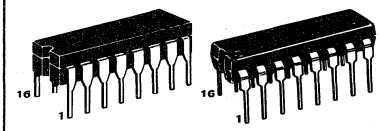
All N-Channel substrates = V_{SS}

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX BUFFERS

Inverting – MC14009UB
Noninverting – MC14010B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

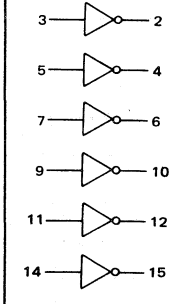
ORDERING INFORMATION

MC14XXXUB
MC14XXXB

Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

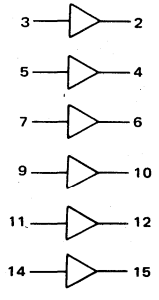
LOGIC DIAGRAMS

MC14009UB



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{CC} = Pin 1

MC14010B



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{CC} = Pin 1

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage #MC14009UB	"0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)			5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)			10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)			15	–	2.5	–	6.75	2.5	–	2.5	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 Vdc)			5.0	4.0	–	4.0	2.75	–	4.0	–	
(V_O = 1.0 Vdc)			10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 Vdc)			15	12.5	–	12.5	8.25	–	12.5	–	
Input Voltage #MC14010B	"0" Level	V_{IL}									Vdc
(V_O = 0.5 Vdc)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 1.0 Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 1.5 Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									Vdc
(V_O = 4.5 Vdc)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 9.0 Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 13.5 Vdc)			15	11	–	11	8.25	–	11	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-1.85	–	-1.25	-1.7	–	-0.9	–	
(V_{OH} = 9.5 Vdc)			10	-0.90	–	-0.6	-0.9	–	-0.4	–	
(V_{OH} = 13.5 Vdc)			15	-2.25	–	-1.8	-3.5	–	-1.5	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	3.75	–	3.2	4	–	2.1	–	mAdc
(V_{OL} = 0.5 Vdc)			10	10	–	8.0	10	–	5.6	–	
(V_{OL} = 1.5 Vdc)			15	30	–	24	30	–	16.8	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-1.5	–	-1.25	-1.7	–	-1.0	–	
(V_{OH} = 9.5 Vdc)			10	-0.72	–	-0.6	-0.9	–	-0.48	–	
(V_{OH} = 13.5 Vdc)			15	-2.15	–	-1.8	-3.5	–	-1.4	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	3.6	–	3.2	4	–	2.5	–	mAdc
(V_{OL} = 0.5 Vdc)			10	9.6	–	8.0	10	–	6.6	–	
(V_{OL} = 1.5 Vdc)			15	28	–	24	35	–	19	–	
Input Current (AL Device)		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)		I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance	MC14009UB	C_{in}	–	–	–	–	10	15	–	–	pF
(V_{in} = 0)	MC14010B						5	7.5			
Quiescent Current (AL Device)		I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
(Per Package)			10	–	2.0	–	0.004	2.0	–	60	
			15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)		I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
(Per Package)			10	–	8.0	–	0.004	8.0	–	60	
			15	–	16	–	0.006	16	–	120	
Total Supply Current**†		I_T	5.0	$I_T = (1.8\ \mu A/kHz)f + I_{DD}$							μAdc
(Dynamic plus Quiescent, Per Package)			10	$I_T = (3.5\ \mu A/kHz)f + I_{DD}$							
(C_L 50 pF on all outputs, all buffers switching)			15	$I_T = (5.3\ \mu A/kHz)f + I_{DD}$							

*T_{low} = 55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

†To Calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

#Noise immunity specified for worst-case input combination
B Suffix Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
UB Suffix Noise Margin for both "1" and "0" level =
0.5 Vdc min @ V_{DD} = 5.0 Vdc
1.0 Vdc min @ V_{DD} = 10 Vdc
1.0 Vdc min @ V_{DD} = 15 Vdc

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25 °C)

Characteristic	Symbol	V_{DD} Vdc	V_{CC} Vdc	All Types Typ	All Types Max	Unit
MC14009UB						
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	5.0	180	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	10	90	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	15	65	130	
Output Fall Time	t_f					ns
t_f = (0.3 ns/pF) C_L + 25 ns		5.0	5.0	40	80	
t_f = (0.12 ns/pF) C_L + 14 ns		10	10	20	40	
t_f = (0.1 ns/pF) C_L + 10 ns		15	15	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 30 ns		5.0	5.0	90	180	
t_{PLH} = (0.66 ns/pF) C_L + 22 ns		10	10	50	100	
t_{PLH} = (0.5 ns/pF) C_L + 15 ns		15	15	40	80	
t_{PLH} = (0.66 ns/pF) C_L + 20 ns		10	5.0	45	90	
t_{PLH} = (0.24 ns/pF) C_L + 18 ns		15	5.0	30	70	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.16 ns/pF) C_L + 12 ns		5.0	5.0	20	60	
t_{PHL} = (0.10 ns/pF) C_L + 8 ns		10	10	15	40	
t_{PHL} = (0.08 ns/pF) C_L + 6 ns		15	15	10	30	
t_{PHL} = (0.05 ns/pF) C_L + 7 ns		10	5.0	10	30	
t_{PHL} = (0.03 ns/pF) C_L + 6 ns		15	5.0	8	20	
MC14010B						
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	5.0	180	360	
t_r = (1.5 ns/pF) C_L + 15 ns		10	10	90	180	
t_r = (1.1 ns/pF) C_L + 10 ns		15	15	65	130	
Output Fall Time	t_f					ns
t_f = (0.2 ns/pF) C_L + 30 ns		5.0	5.0	40	80	
t_f = (0.06 ns/pF) C_L + 17 ns		10	10	20	40	
t_f = (0.04 ns/pF) C_L + 13 ns		15	15	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 30 ns		5.0	5.0	90	180	
t_{PLH} = (0.66 ns/pF) C_L + 22 ns		10	10	50	100	
t_{PLH} = (0.5 ns/pF) C_L + 15 ns		15	15	40	80	
t_{PLH} = (0.66 ns/pF) C_L + 20 ns		10	5.0	45	90	
t_{PLH} = (0.24 ns/pF) C_L + 18 ns		15	5.0	30	70	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.4 ns/pF) C_L + 20 ns		5.0	5.0	40	130	
t_{PHL} = (0.08 ns/pF) C_L + 20 ns		10	10	25	70	
t_{PHL} = (0.06 ns/pF) C_L + 15 ns		15	15	20	70	
t_{PHL} = (0.08 ns/pF) C_L + 15 ns		10	5.0	20	50	
t_{PHL} = (0.09 ns/pF) C_L + 10 ns		15	5.0	15	40	

* The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS VERSUS TEMPERATURE

MC14009UB

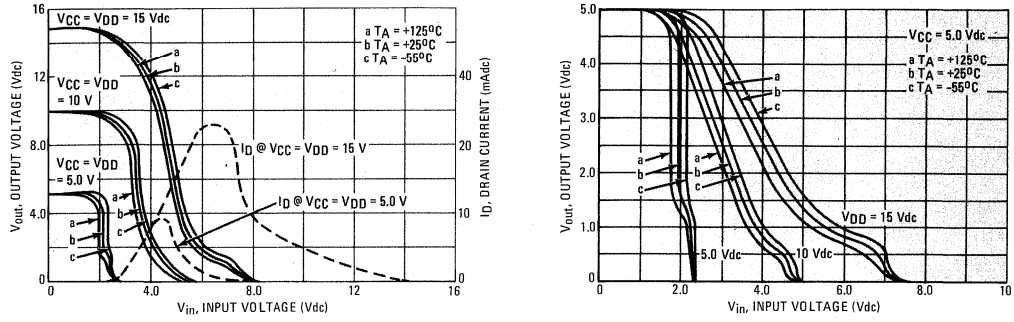


FIGURE 2 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS VERSUS TEMPERATURE

MC14010B

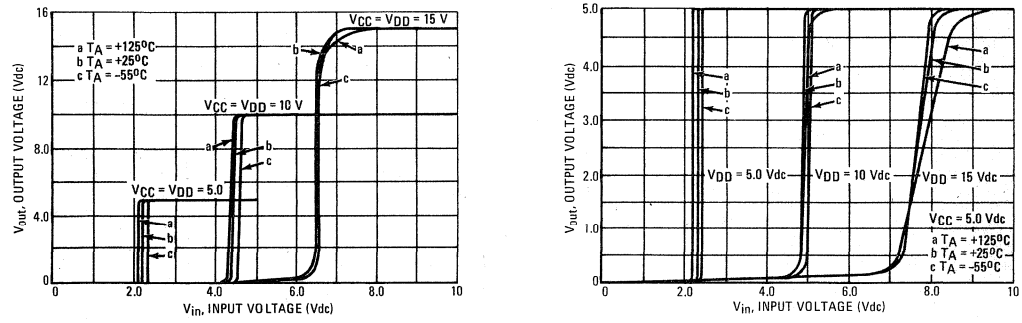


FIGURE 3 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

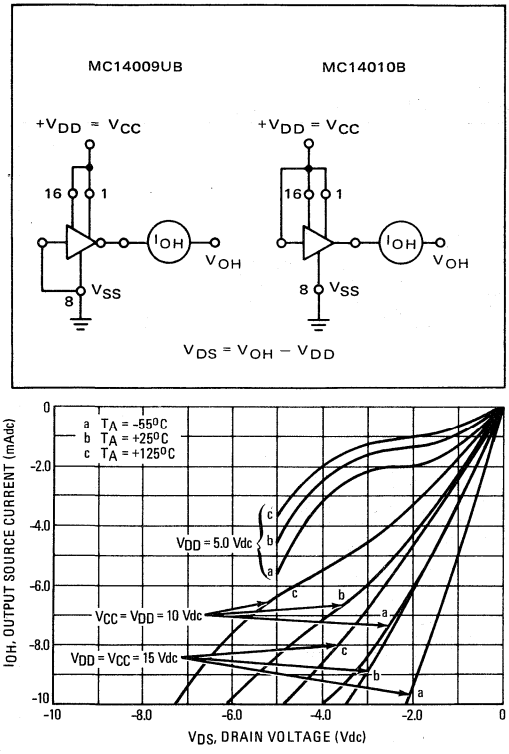


FIGURE 4 – TYPICAL OUTPUT SINK CHARACTERISTICS

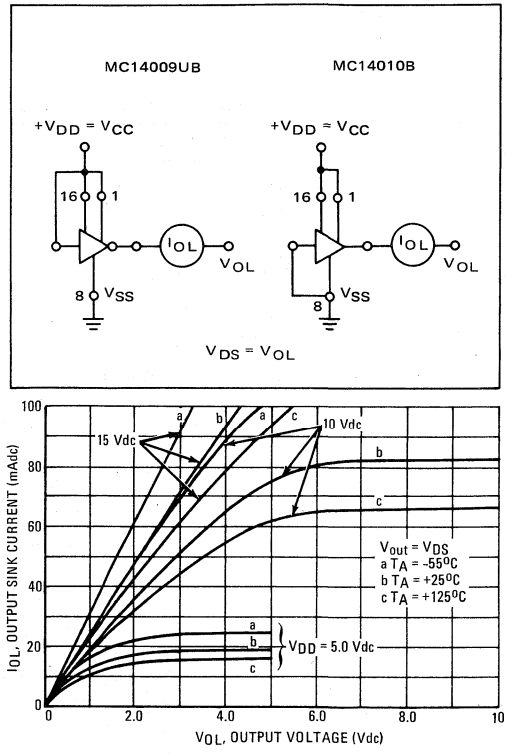
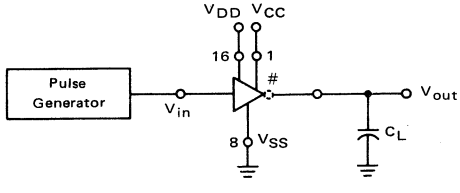


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



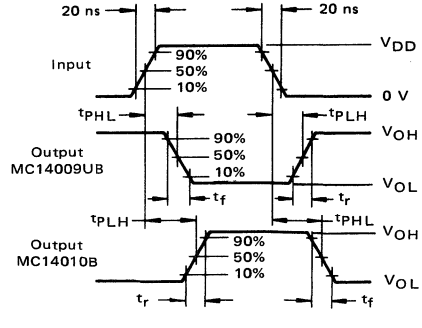
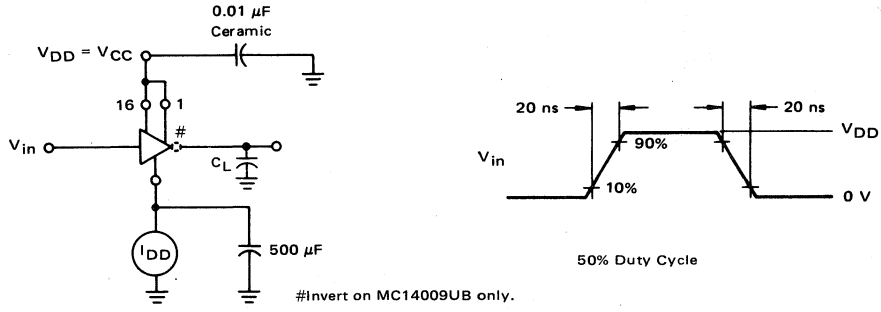


FIGURE 6 – TYPICAL DYNAMIC POWER DISSIPATION CHARACTERISTICS



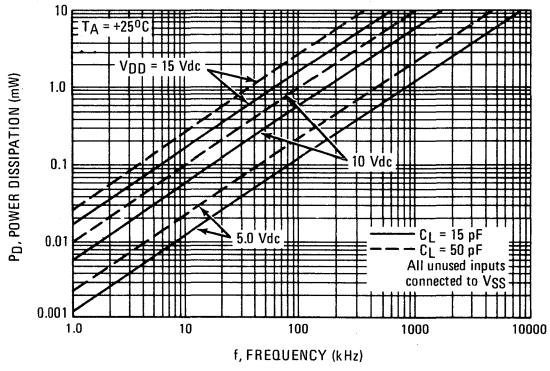
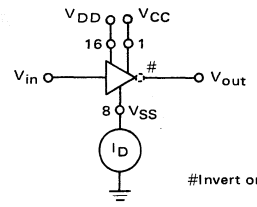


FIGURE 7 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT



#Invert on MC14009UB only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

MOTOROLA

MC14011B
MC14011UB

QUAD 2-INPUT "NAND" GATE

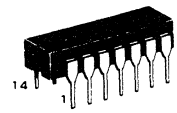
The MC14011B and MC14011UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14011B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14011B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4011B and CD4011UB

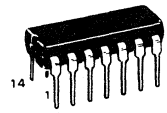
CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

or UB, as applicable

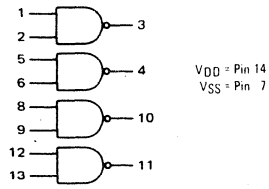
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

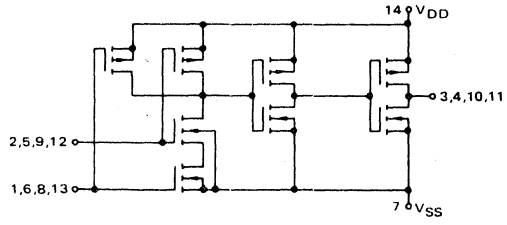
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

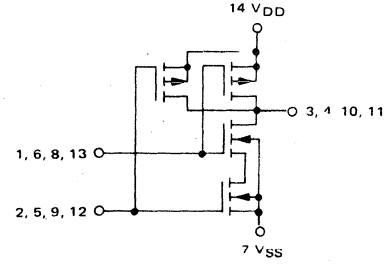
See the MC14001B data sheet for complete characteristics of the B-Series device.
See the MC14001UB data sheet for complete characteristics for the UB device.

LOGIC DIAGRAM



MC14011B — **CIRCUIT SCHEMATICS (1/4 of Device Shown)** — **MC14011UB**





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14012B
MC14012UB

CMOS SSI

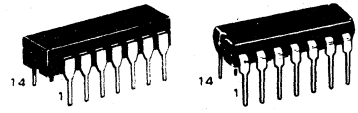
(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NAND" GATE

DUAL 4-INPUT "NAND" GATE

The MC14012B and MC14012UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14012B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14012B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4012B and CD4012UB



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

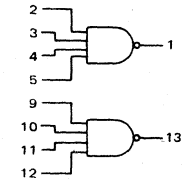
MC14XXXB — Suffix — Denotes
or UB as applicable
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics of the B-Series device.
See the MC14001UB data sheet for complete characteristics for the UB device.

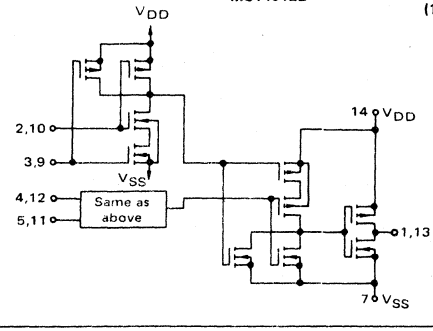
LOGIC DIAGRAM



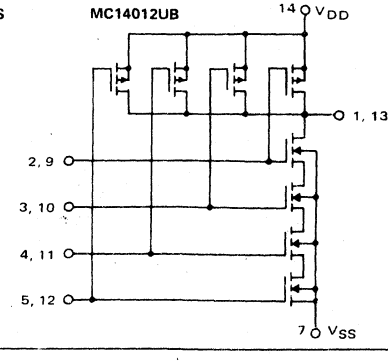
V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATICS
(1/2 of Device Shown)

MC14012B



MC14012UB



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14013B

DUAL TYPE D FLIP-FLOP

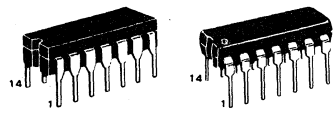
The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Toggle Rate = 4 MHz typical @ 5 Vdc
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL TYPE D FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

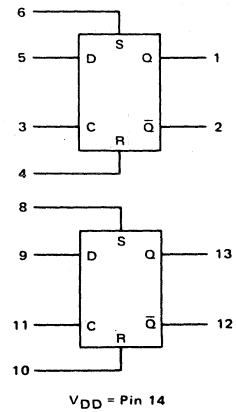
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS				OUTPUTS		
CLOCK†	DATA	RESET	SET	Q	$\overline{Q}$	
↑	0	0	0	0	1	
↑	1	0	0	1	0	
↓	X	0	0	Q	$\overline{Q}$	No Change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = Don't Care
† = Level Change

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage‡ "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.1	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.5 μA/kHz) f + I_{DD}							
		15	I_T = (2.3 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
‡Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
Clock to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Set to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	350	450	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 50 ns		15	–	75	150	
Setup Times	t_{su}	5.0	40	20	–	ns
		10	20	10	–	
		15	15	7.5	–	
Hold Times	t_h	5.0	40	20	–	ns
		10	20	10	–	
		15	15	7.5	–	
Clock Pulse Width	t_{WL}, t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	70	35	–	
Clock Pulse Frequency	f_{cl}	5.0	–	4.0	2.0	MHz
		10	–	10	5.0	
		15	–	14	7.0	
Clock Pulse Rise and Fall Time	t_{TLH}	5.0	–	–	15	μs
	t_{THL}	10	–	–	5.0	
		15	–	–	4.0	
Set and Reset Pulse Width	t_{WL}, t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	70	35	–	

*The formula given is for the typical characteristics only.

LOGIC DIAGRAM
(1/2 of Device Shown)

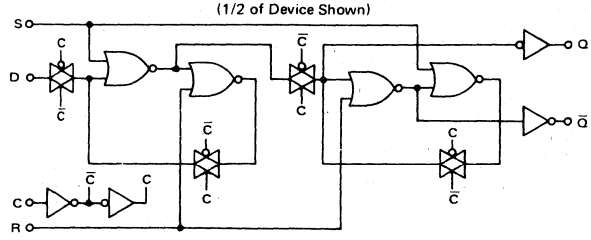


FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS
(Data, Clock, and Output)

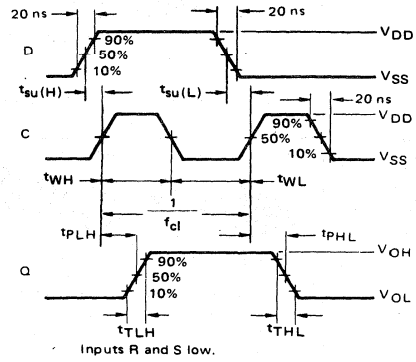
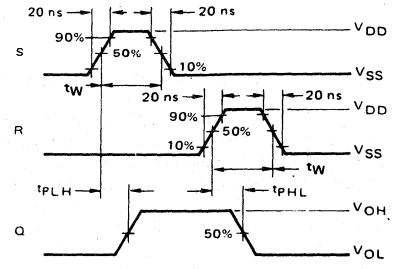
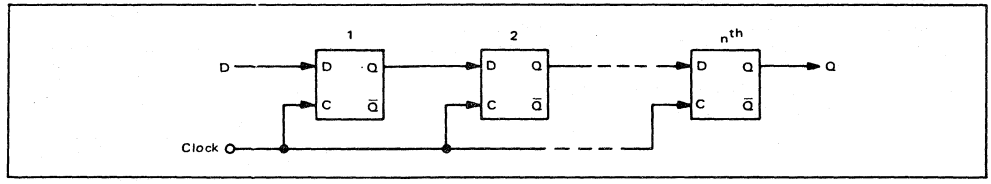


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, and Output)

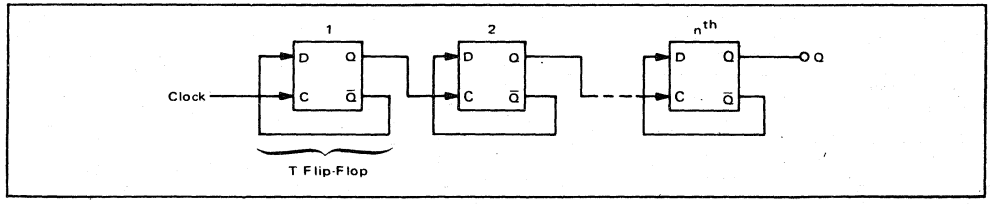


TYPICAL APPLICATIONS

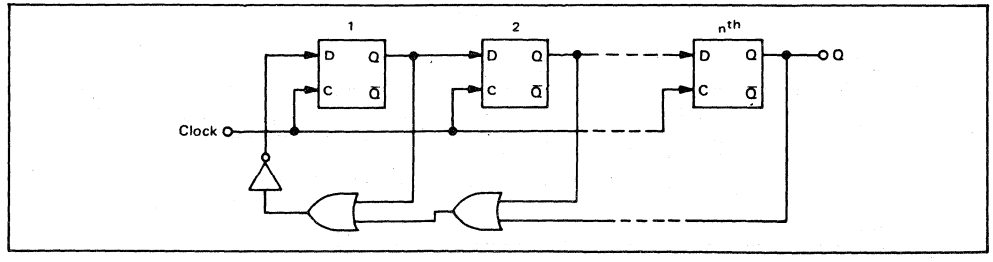
n-STAGE SHIFT REGISTER



BINARY RIPPLE UP-COUNTER (Divide-by-2^n)



MODIFIED RING COUNTER (Divide-by-(n + 1))



MOTOROLA

MC14014B
MC14021B

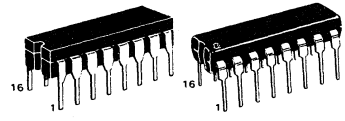
CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER

8-BIT STATIC SHIFT REGISTER

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation from DC to 7.0 MHz
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range -- AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

SERIAL OPERATION:

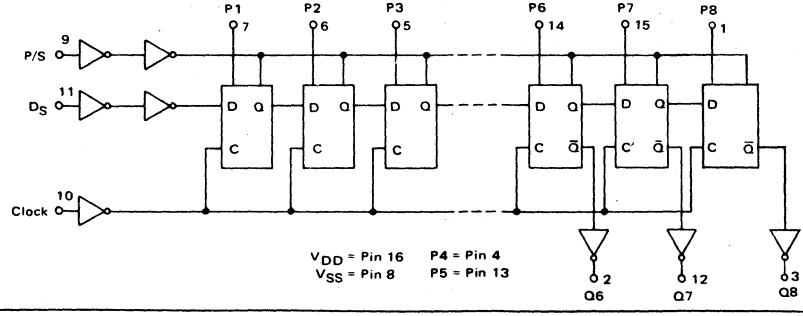
t	CLOCK	D_S	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n		0	0	0	?	?
n+1		1	0	1	0	?
n+2		0	0	0	1	0
n+3		1	0	1	0	1
		X	0	Q6	Q7	Q8

PARALLEL OPERATION:

CLOCK MC14014B	CLOCK MC14021B	D_S	P/S	D_M	$*Q_M$
	X	X	1	0	0
	X	X	1	1	1

*Q6, Q7, & Q8 are available externally
X = Don't Care

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05		0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.50 μA/kHz) f + I_{DD}							
		15	I_T = (2.25 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

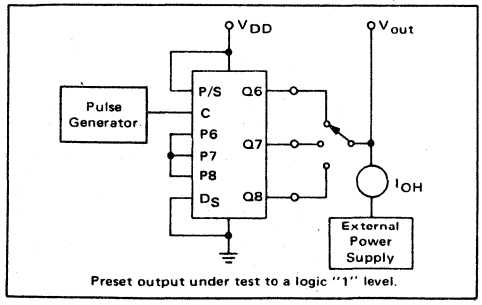
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time (Clock to Q, P/S to Q)	t_{PLH}, t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns		10	–	170	340	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 90 ns		15	–	115	230	
Clock Pulse Width	t_{WH}	5.0	400	150	–	ns
		10	175	75	–	
		15	135	40	–	
Clock Frequency	f_{cl}	5.0	1.5	3.0	–	MHz
		10	3.0	6.0	–	
		15	4.0	8.0	–	
Parallel/Serial Control Pulse Width	t_{WH}	5.0	400	150	–	ns
		10	175	75	–	
		15	135	40	–	
Setup Time	t_{su}	5.0	350	150	–	ns
		10	80	50	–	
		15	60	30	–	
Input Clock Rise Time	$t_{r(cl)}$	5.0	–	–	15	μs
		10	–	–	15	
		15	–	–	15	

*The formula given is for the typical characteristics only.

FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT



Preset output under test to a logic "1" level.

FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT

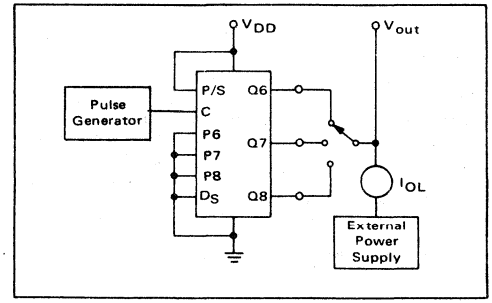


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

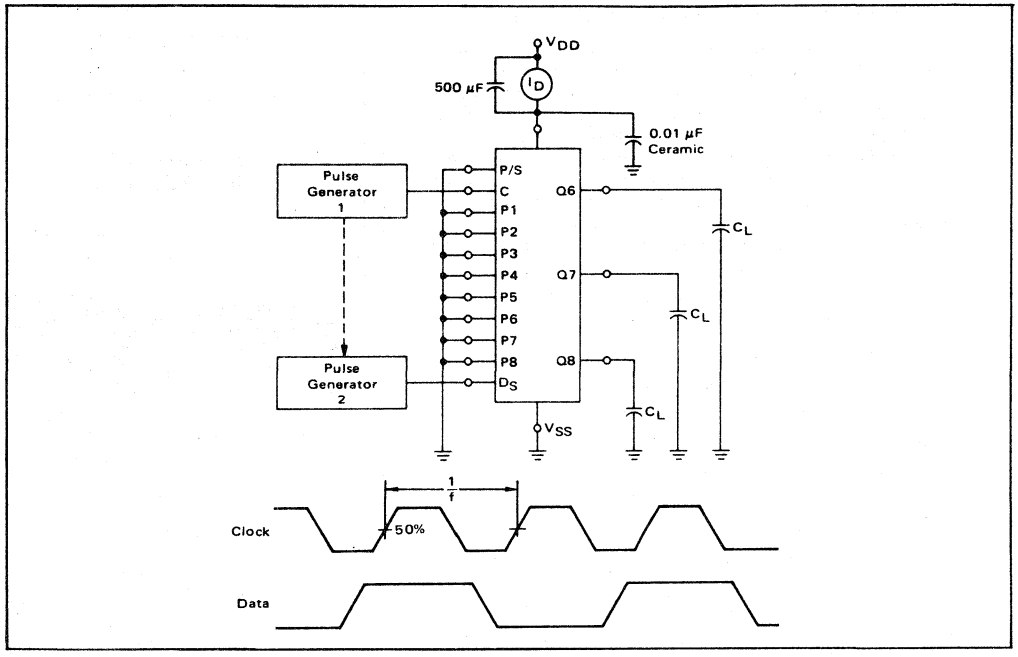
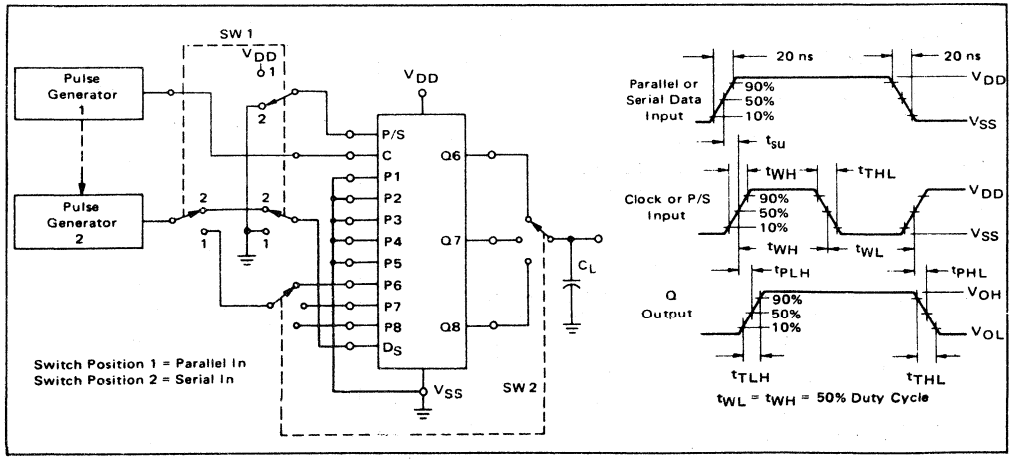


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MOTOROLA

MC14015B

DUAL 4-BIT STATIC SHIFT REGISTER

The MC14015B dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-state serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. There complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation -- Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Low Input Capacitance – 5.0 pF typical
- Logic Swing Independent of Fanout
- Toggle Rate = 6.0 MHz @ 10 Vdc
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive going edge of the clock pulse.
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range -- AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLES

CLOCKED OPERATION (SYNCHRONOUS)

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$Q_{n+1} = D_n$, R = 0

DIRECT OPERATION (ASYNCHRONOUS)

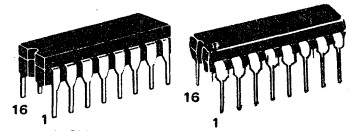
R	Q
0	Q
1	0

C = D = Don't Care

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-BIT STATIC SHIFT REGISTER



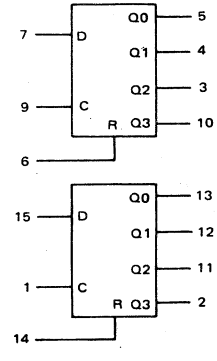
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage≠ "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.4 μA/kHz) f + I_{DD}							
		15	I_T = (3.6 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
≠Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pf, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock, Data to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 225 ns		5.0	–	310	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	170	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 375 ns		5.0	–	460	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	120	170	
Clock Pulse Width	t_{WH}	5.0	–	185	400	ns
		10	–	85	175	
		15	–	55	135	
Clock Pulse Frequency	f_{cl}	5.0	–	2.0	1.5	MHz
		10	–	6.0	3.0	
		15	–	7.5	3.75	
Clock Pulse Rise and Fall Times	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
Reset Pulse Width	t_{WH}	5.0	400	200	–	ns
		10	160	80	–	
		15	120	60	–	
Setup Time	t_{su}	5.0	350	100	–	ns
		10	100	50	–	
		15	75	40	–	

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

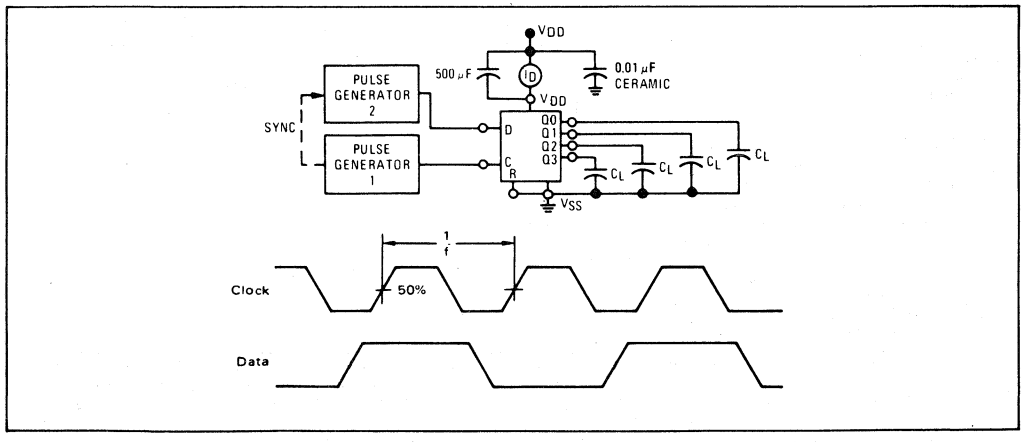


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

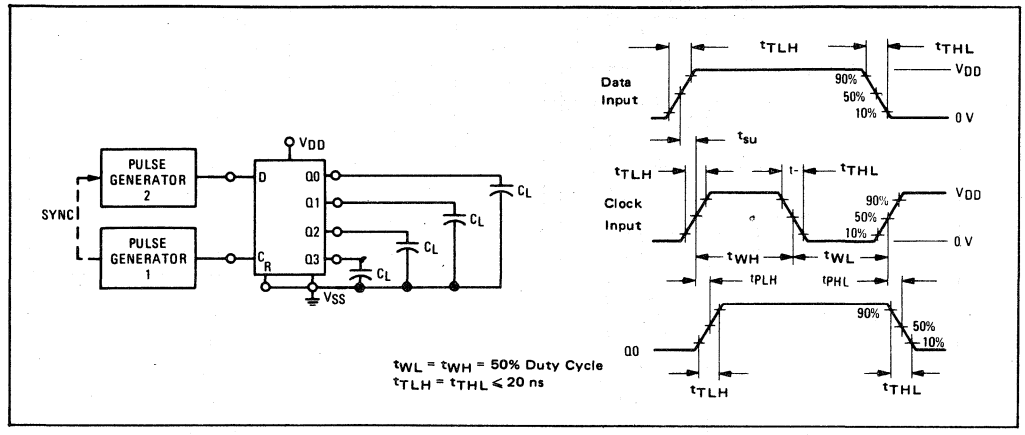
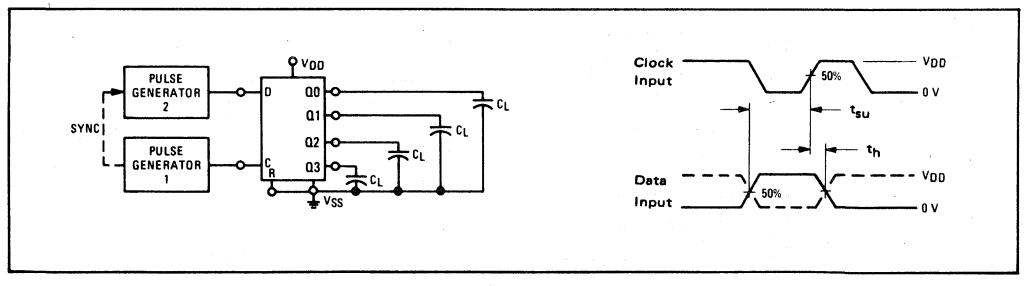
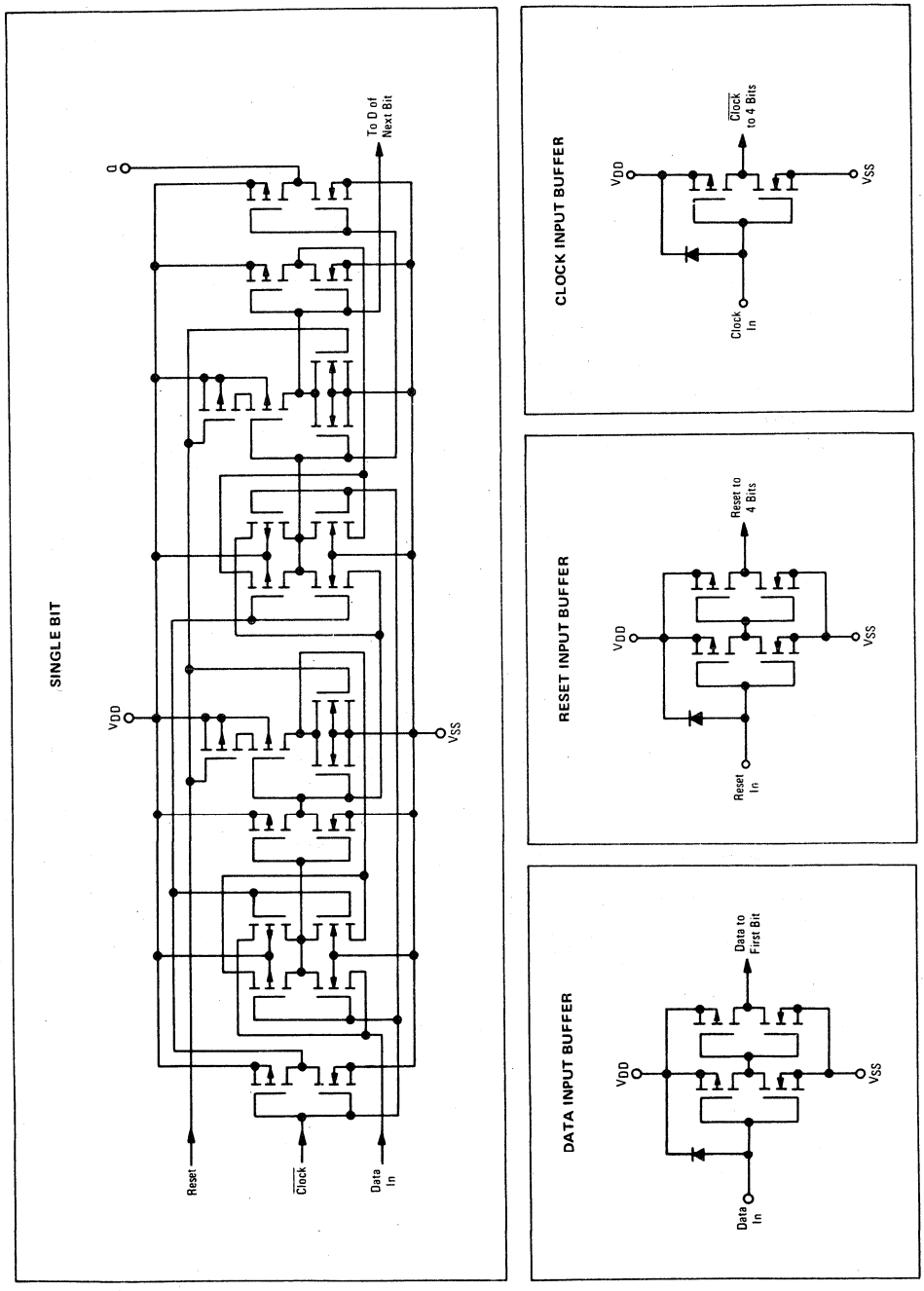


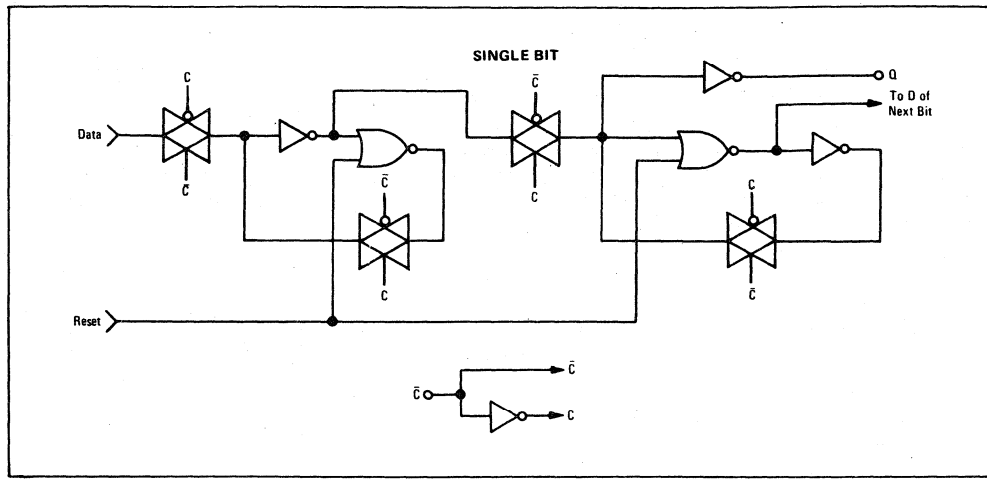
FIGURE 3 – SETUP AND HOLD TIME TEST CIRCUIT AND WAVEFORMS

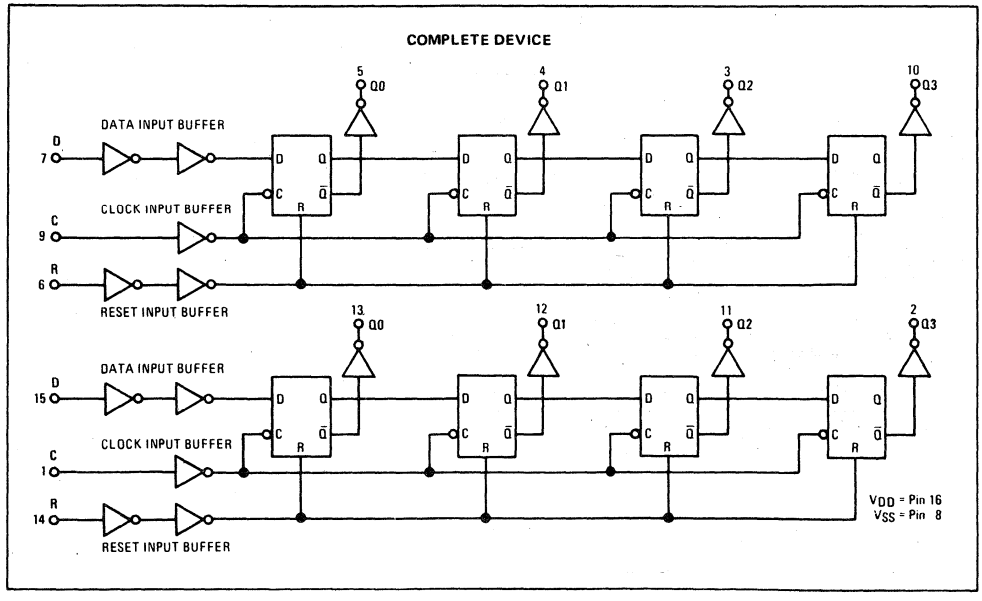


CIRCUIT SCHEMATICS



LOGIC DIAGRAMS





MOTOROLA

MC14016B

CMOS SSI

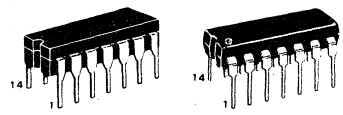
(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH
QUAD MULTIPLEXER

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14016B quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logis implementation.

- High On/Off Output Voltage Ratio – 65 dB Typical
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches – 80 dB typical @ 1.0 MHz
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 54 MHz @ 5 Vdc
- Linearized Transfer Characteristics
- Low Noise – $12nV/\sqrt{Cycle}$, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4016B, CD4066B



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

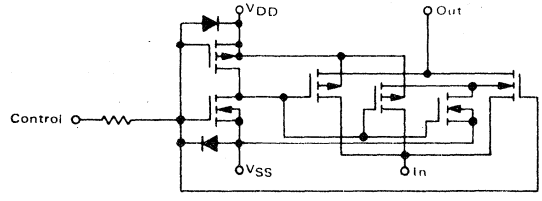
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

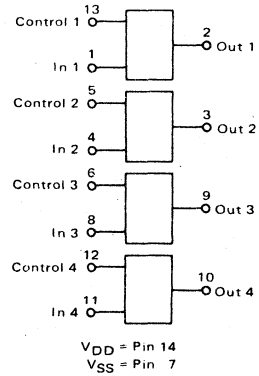
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
Through Current	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the control inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} and V_{out} is not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)



BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS

Characteristics	Figure	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Voltage#	1	V_{IL}	5.0	–	–	–	1.5	0.9	–	–	Vdc
Control Input			10	–	–	–	1.5	0.9	–	–	
			15	–	–	–	1.5	0.9	–	–	
		V_{IH}	5.0	–	–	3.0	2.0	–	–	–	Vdc
			10	–	–	8.0	6.0	–	–	–	
			15	–	–	13	11	–	–	–	
Input Current (AL Device) Control	–	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device) Control	–	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance	–	C_{in}									pF
Control			–	–	–	–	5.0	–	–	–	
Switch Input			–	–	–	–	5.0	–	–	–	
Switch Output			–	–	–	–	5.0	–	–	–	
Feed Through			–	–	–	–	0.2	–	–	–	
Quiescent Current (AL Device)	2,3	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)			10	–	0.50	–	0.0010	0.50	–	15	
			15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	2,3	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)			10	–	2.0	–	0.0010	2.0	–	15	
			15	–	4.0	–	0.0015	4.0	–	30	
"ON" Resistance (AL Device)	4,5,6	R_{ON}									Ohms
($V_C = V_{DD}$, $R_L = 10\ k\Omega$)											
(V_{in} = +5.0 Vdc)			5.0	–	600	–	300	660	–	960	
(V_{in} = –5.0 Vdc) V_{SS} = –5 Vdc				–	600	–	300	660	–	960	
(V_{in} = ±0.25 Vdc)				–	600	–	280	660	–	960	
(V_{in} = +7.5 Vdc)			7.5	–	360	–	240	400	–	600	
(V_{in} = –7.5 Vdc) V_{SS} = –7.5 Vdc				–	360	–	240	400	–	600	
(V_{in} = ±0.25 Vdc)				–	360	–	180	400	–	600	
(V_{in} = +10 Vdc)			10	–	600	–	260	660	–	960	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	600	–	310	660	–	960	
(V_{in} = +5.6 Vdc)				–	600	–	310	660	–	960	
(V_{in} = +15 Vdc)			15	–	360	–	260	400	–	600	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	360	–	260	400	–	600	
(V_{in} = +9.3 Vdc)				–	360	–	300	400	–	600	
"ON" Resistance (CL/CP Device)	4,5,6	R_{ON}									Ohms
($V_C = V_{DD}$, $R_L = 10\ k\Omega$)											
(V_{in} = +5.0 Vdc)			5.0	–	610	–	300	660	–	840	
(V_{in} = –5.0 Vdc) V_{SS} = –5 Vdc				–	610	–	300	660	–	840	
(V_{in} = ±0.25 Vdc)				–	610	–	280	660	–	840	
(V_{in} = +7.5 Vdc)			7.5	–	370	–	240	400	–	520	
(V_{in} = –7.5 Vdc) V_{SS} = –7.5 Vdc				–	370	–	240	400	–	520	
(V_{in} = ±0.25 Vdc)				–	370	–	180	400	–	520	
(V_{in} = +10 Vdc)			10	–	610	–	260	660	–	840	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	610	–	260	660	–	840	
(V_{in} = +5.6 Vdc)				–	610	–	310	660	–	840	
(V_{in} = +15 Vdc)			15	–	370	–	260	400	–	520	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	370	–	260	400	–	520	
(V_{in} = +9.3 Vdc)				–	370	–	300	400	–	520	
Δ"ON" Resistance	–	ΔR_{ON}									Ohms
Between any 2 circuits in a common package											
($V_C = V_{DD}$)											
(V_{in} = ±5.0 Vdc) V_{SS} = –5 Vdc			5.0	–	–	–	15	–	–	–	
(V_{in} = ±7.5 Vdc) V_{SS} = –7.5 Vdc			7.5	–	–	–	10	–	–	–	
Input/Output Leakage Current ($V_C = V_{SS}$)	–	–									µAdc
(V_{in} = +7.5, V_{out} = –7.5 Vdc)			7.5	–	±0.100	–	±0.0015	±0.100	–	±1.0	
(V_{in} = –7.5, V_{out} = +7.5 Vdc)			7.5	–	±0.100	–	±0.0015	±0.100	–	±1.0	

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Input Voltage Specified as the voltage required at the Control Input for a 10 µA current through the transmission gate with an input-to-output stress of V_{DD}–V_{SS} for V_{IL} and V_{IH}.

NOTE: All unused control inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Propagation Delay Time (V_{SS} = 0 Vdc)	7	t_{PLH},	5.0	–	15	45	ns
V_{in} to V_{out}		t_{PHL}	10	–	7.0	15	
(V_C = V_{DD}, R_L = 10 kΩ)			15	–	6.0	12	
Control to Output	8		5.0	–	34	90	ns
(V_{in} ≤ 10 Vdc, R_L = 1.0 kΩ)			10	–	20	45	
			15	–	15	35	
Crosstalk, Control to Output (V_{SS} = 0 Vdc)	9	–	5.0	–	30	–	mV
(V_C = V_{DD}, R_{in} = 1.0 kΩ, R_{out} = 10 kΩ,			10	–	50	–	
f = 1kHz)			15	–	100	–	
Crosstalk between any two switches (V_{SS} = 0 Vdc)	–	–	5.0	–	–80	–	dB
(R_L = 1.0 kΩ, f = 1.0 MHz,							
crosstalk = $20 \log_{10} \frac{V_{out1}}{V_{out2}}$)							
Maximum Control Input Pulse Frequency (V_{SS} = 0 Vdc)	–	–	5.0	–	5.0	–	MHz
(R_L = 1.0 kΩ)			10	–	10	–	
			15	–	12	–	
Noise Voltage (V_{SS} = 0 Vdc)	10,11	–	5.0	–	24	–	nV/√Cycle
(V_C = V_{DD}, f = 100 Hz)			10	–	25	–	
			15	–	30	–	
(V_C = V_{DD}, f = 100 kHz)			5.0	–	12	–	
			10	–	12	–	
			15	–	15	–	
Sine Wave (Distortion) (V_{SS} = –5 Vdc)	–	–	5.0	–	0.16	–	%
(V_{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc,							
R_L = 10 kΩ, f = 1.0 kHz)							
Insertion Loss (V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = –5 Vdc,	12	–	5.0	–			dB
RMS centered = 0.0 Vdc, f = 1.0 MHz)							
$I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$)							
(R_L = 1.0 kΩ)				–	2.3	–	
(R_L = 10 kΩ)				–	0.2	–	
(R_L = 100 kΩ)				–	0.1	–	
(R_L = 1.0 MΩ)				–	0.05	–	
Bandwidth (–3 dB)	12,13	BW	5.0	–			MHz
(V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = –5 Vdc,							
RMS centered @ 0.0 Vdc)							
(R_L = 1.0 kΩ)				–	54	–	
(R_L = 10 kΩ)				–	40	–	
(R_L = 100 kΩ)				–	38	–	
(R_L = 1.0 MΩ)				–	37	–	
Feedthrough (V_{SS} = –5 Vdc)	–	–	5.0	–			kHz
(V_C = V_{SS}, $20 \log_{10} \frac{V_{out}}{V_{in}}$ = –50 dB)							
(R_L = 1.0 kΩ)				–	1250	–	
(R_L = 10 kΩ)				–	140	–	
(R_L = 100 kΩ)				–	18	–	
(R_L = 1.0 MΩ)				–	2.0	–	

*The formula is for the typical characteristics only.

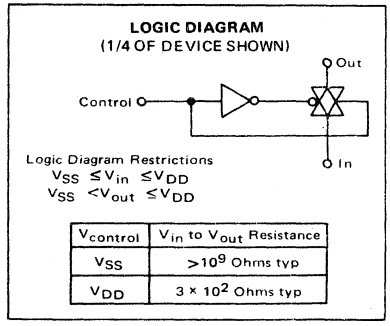


FIGURE 1 – INPUT VOLTAGE TEST CIRCUIT

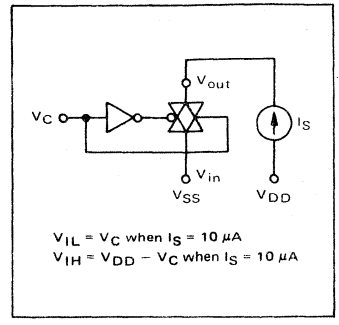


FIGURE 2 – QUIESCENT POWER DISSIPATION TEST CIRCUIT

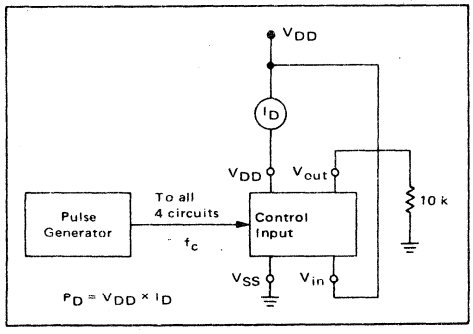
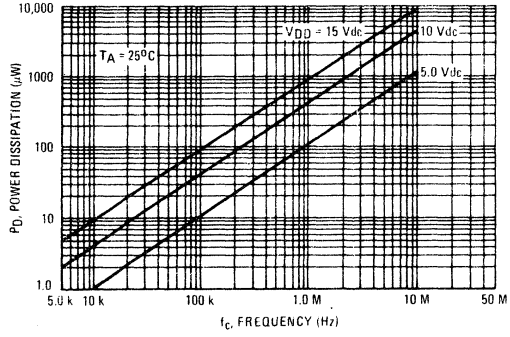


FIGURE 3 – TYPICAL POWER DISSIPATION PER CIRCUIT (1/4 OF DEVICE SHOWN)



TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 4 – V_{SS} = –5.0 V AND –7.5 V

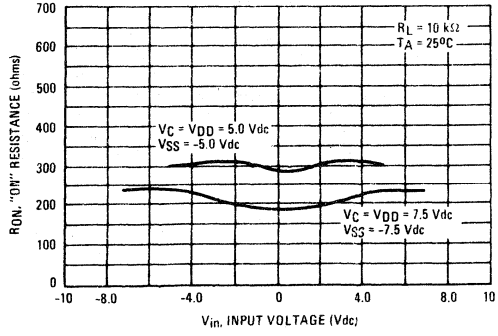


FIGURE 5 – V_{SS} = 0 V

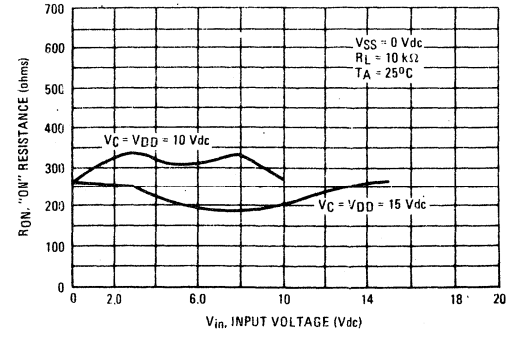


FIGURE 6 – R_{ON} CHARACTERISTICS TEST CIRCUIT

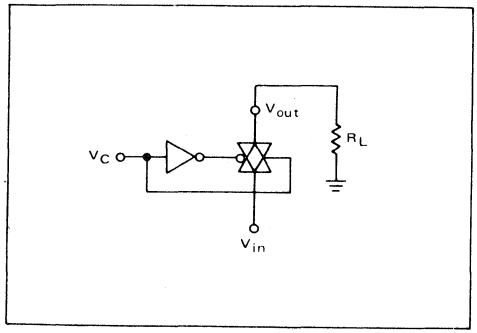


FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

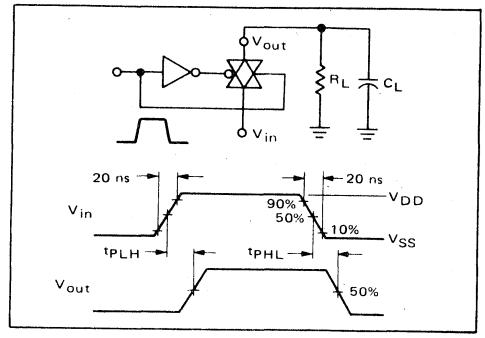


FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

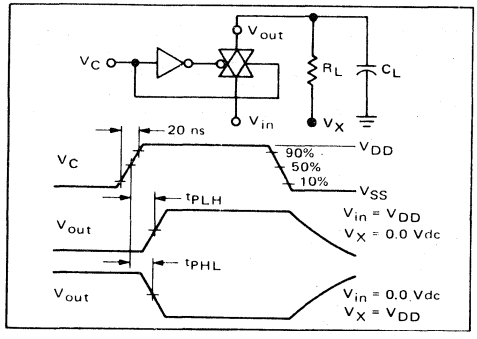


FIGURE 9 – CROSSTALK TEST CIRCUIT

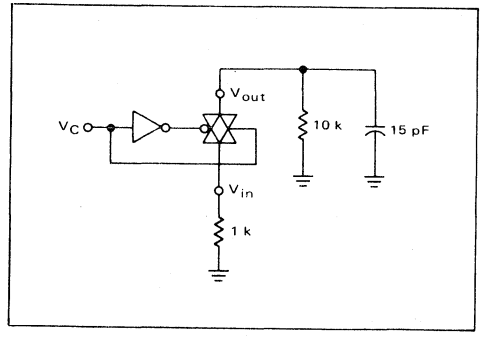


FIGURE 10 – NOISE VOLTAGE TEST CIRCUIT

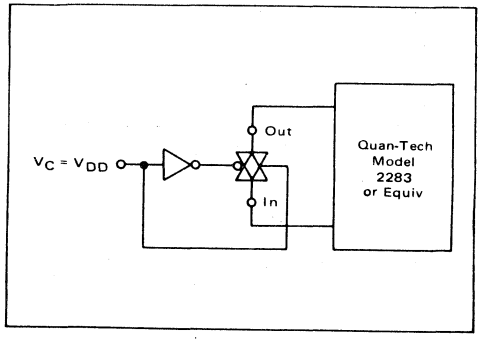


FIGURE 11 – TYPICAL NOISE CHARACTERISTICS

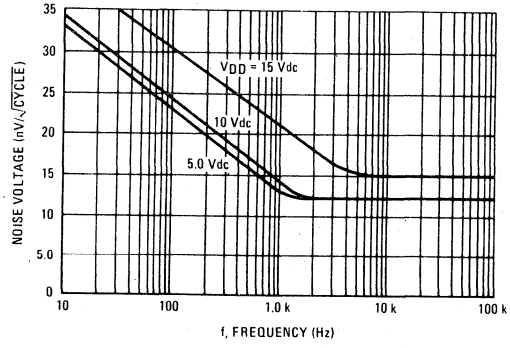


FIGURE 12 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS

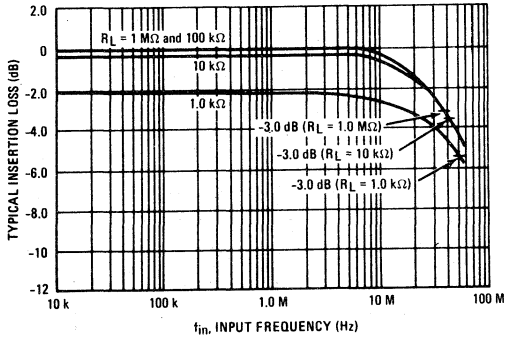
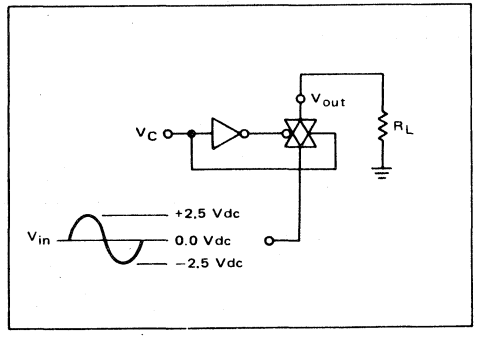


FIGURE 13 – FREQUENCY RESPONSE TEST CIRCUIT



MOTOROLA

MC14017B

CMOS MSI

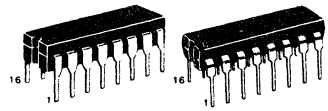
(LOW-POWER COMPLEMENTARY MOS)

DECADE COUNTER/DIVIDER

DECADE COUNTER/DIVIDER

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ V_{DD} = 10 Vdc
- Divide-by-N Counting
- Quiescent Current = 5.0 nA/package Typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

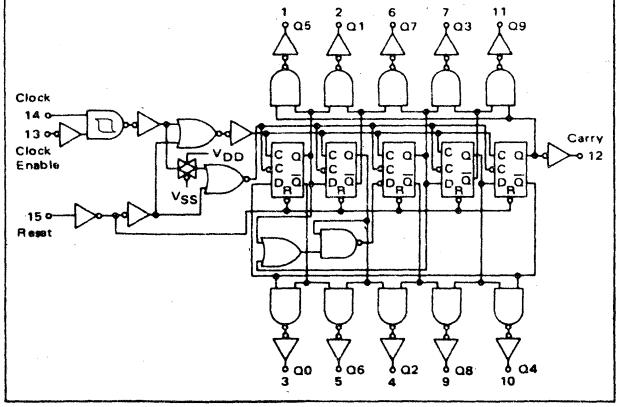
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM

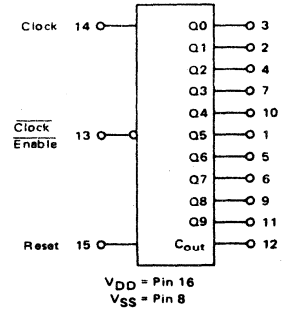


FUNCTIONAL TRUTH TABLE
(Positive Logic)

CLOCK	$\overline{\text{CLOCK ENABLE}}$	RESET	DECODE OUTPUT = n
0	X	0	n
X	1	0	n
X	X	1	Q0
⌐	0	0	n+1
⌐	X	0	n
X	⌐	0	n
1	⌐	0	n+1

X = Don't Care If n < 5 Carry = "1", Otherwise = "0"

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.27 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.55 µA/kHz) f + I_{DD}							
		15	I_T = (0.83 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1.1 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

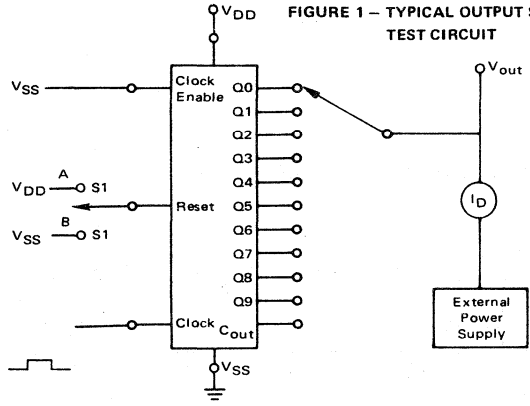
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Reset to Decade Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns		15	–	175	350	
Propagation Delay Time	t_{PLH},					ns
Clock to C_{out}	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 142 ns		10	–	175	350	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 100 ns		15	–	125	250	
Propagation Delay Time	t_{PLH},					ns
Clock to Decode Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns		15	–	175	350	
Turn-Off Delay Time	t_{PLH}					ns
Reset to C_{out}						
t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH} = (0.66 ns/pF) C_L + 142 ns		10	–	175	350	
t_{PLH} = (0.5 ns/pF) C_L + 100 ns		15	–	125	250	
Clock Pulse Width	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	75	35	–	
Clock Frequency	f_{cl}	5.0	–	5.0	2.0	MHz
		10	–	12	5.0	
		15	–	16	6.7	
Reset Pulse Width	t_{WH}	5.0	500	250	–	ns
		10	250	125	–	
		15	190	95	–	
Reset Removal Time	t_{rem}	5.0	750	375	–	ns
		10	275	135	–	
		15	210	105	–	
Clock Input Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Clock Enable Setup Time	t_{su}	5.0	350	175	–	ns
		10	150	75	–	
		15	115	52	–	
Clock Enable Removal Time	t_{rem}	5.0	420	260	–	ns
		10	200	100	–	
		15	140	70	–	

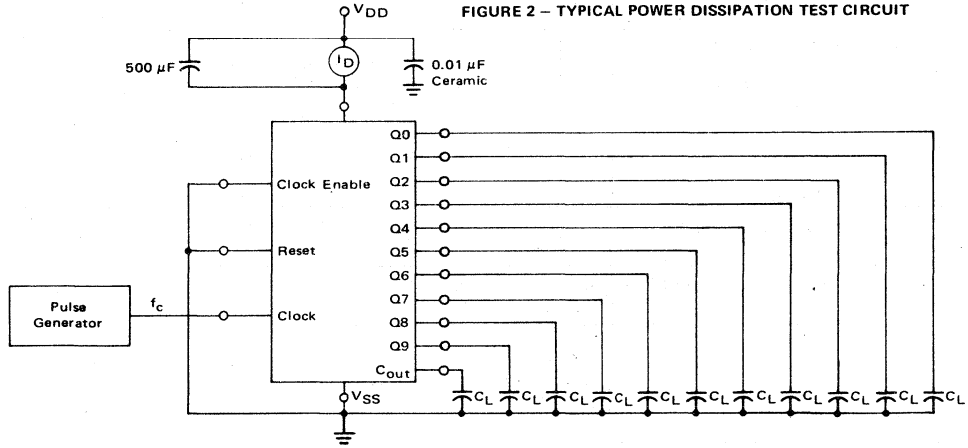
*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



	OUTPUT SINK DRIVE	OUTPUT SOURCE DRIVE
DECODE OUTPUTS	(S1 to A)	Clock to desired outputs (S1 to B)
Carry	Clock to 5 thru 9 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT



APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 3 – COUNTER EXPANSION

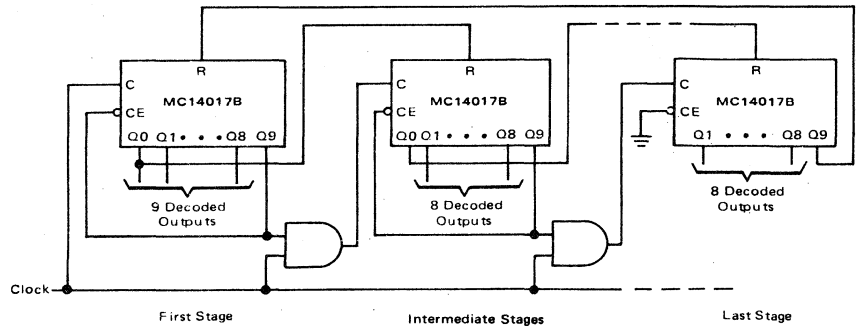
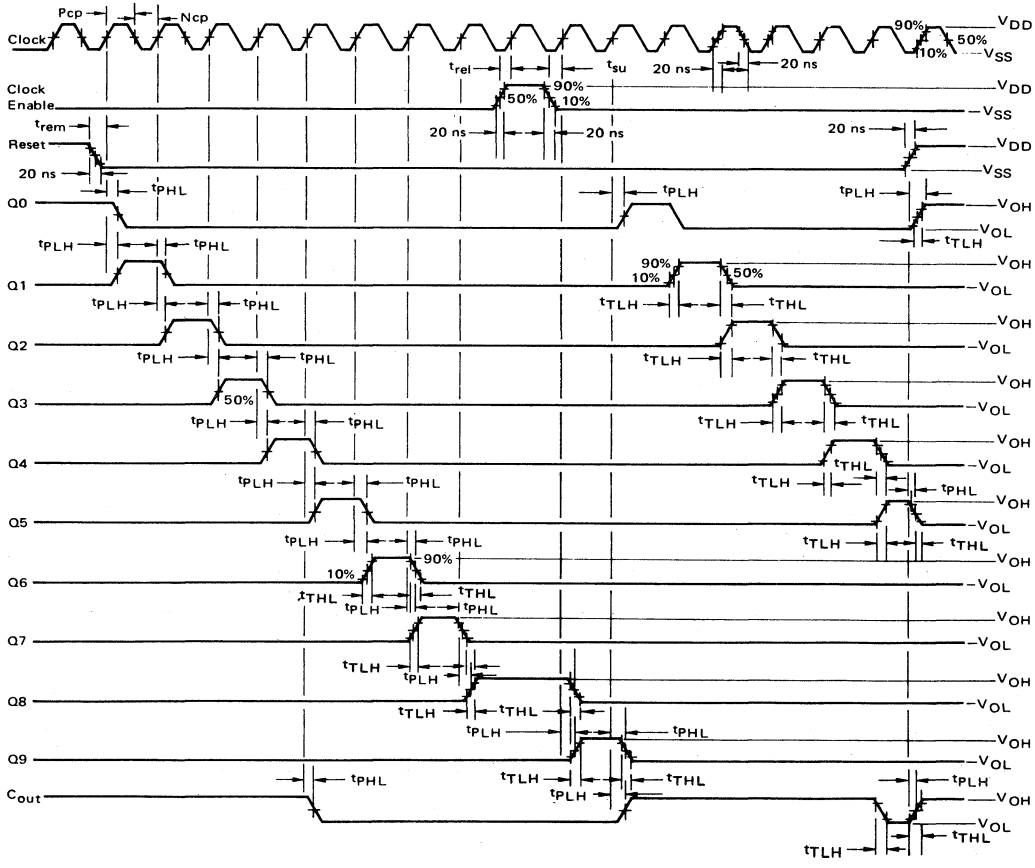


FIGURE 4 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



MOTOROLA

MC14018B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PRESETTABLE DIVIDE-BY-N COUNTER

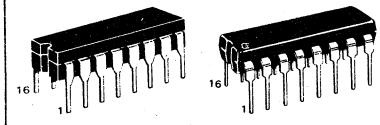
PRESETTABLE DIVIDE-BY-N COUNTER

The MC14018B contains five Johnson counter stages which are asynchronously presettable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

Presetting is accomplished by a logic 1 on the preset enable input. Data on the Jam inputs will then be transferred to their respective $\overline{Q}$ outputs (inverted). A logic 1 on the reset input will cause all $\overline{Q}$ outputs to go to a logic 1 state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate $\overline{Q}$ outputs to the data input, as shown in the Function Selection table. Anti-lock gating is included in the MC14018B to assure proper counting sequence.

- Fully Static Operation
- Medium Speed — 6.5 MHz typical @ 10 V
- Schmitt Trigger on Clock Input
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4018B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

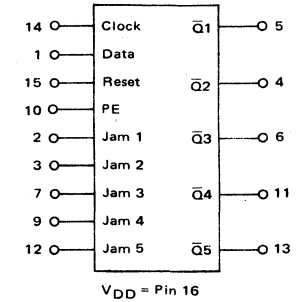
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FUNCTIONAL TRUTH TABLE

Clock	Reset	Preset Enable	Jam Input	$\overline{Q}_n$
↓	0	0	X	$\overline{Q}_n$
↑	0	0	X	$\overline{D}_n$*
X	0	1	0	1
X	0	1	1	0
X	1	X	X	1

*D_n is the Data input for that stage. Stage 1 has Data brought out to Pin 1.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.7 µA/kHz) f + I_{DD}							
		15	I_T = (1.0 µA/kHz) f + I_{DD}							

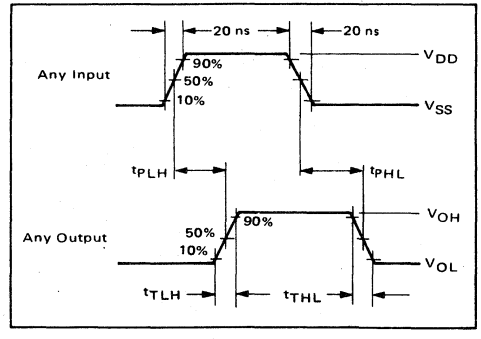
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

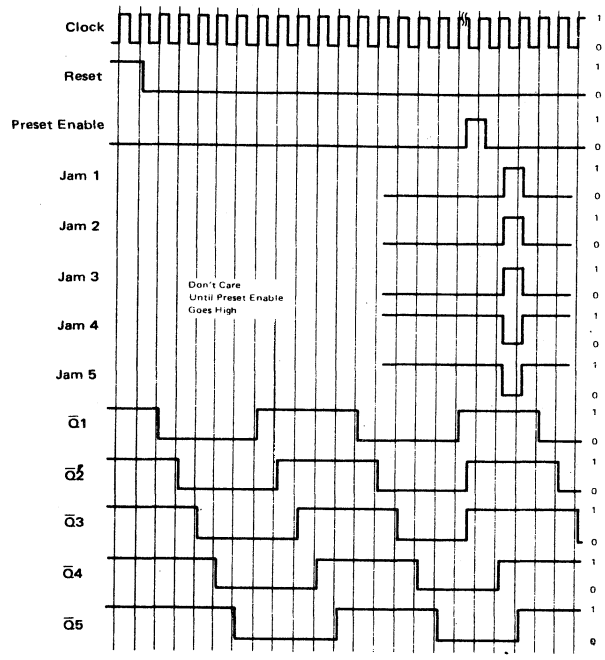
Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to $\overline{Q}$						
t_{PLH},t_{PHL} = (0.90 ns/pF) C_L + 265 ns		5.0	–	310	620	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 102 ns		10	–	120	240	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 72 ns		15	–	85	170	
Reset to $\overline{Q}$						ns
t_{PLH} = (0.90 ns/pF) C_L + 325 ns		5.0	–	370	740	
t_{PLH} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH} = (0.26 ns/pF) C_L + 81 ns		15	–	100	200	
Preset Enable to $\overline{Q}$						ns
t_{PLH},t_{PHL} = (0.90 ns/pF) C_L + 325 ns		5.0	–	370	740	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 81 ns		15	–	100	200	
Setup Time	t_{su}					ns
Data (Pin 1) to Clock		5.0	200	0	–	
		10	100	0	–	
		15	80	0	–	
Jam Inputs to Preset Enable		5.0	200	0	–	ns
		10	100	0	–	
		15	80	0	–	
Data (Jam Inputs)-to-Preset Enable Hold Time	t_h	5.0	540	270	–	ns
		10	500	250	–	
		15	480	240	–	
Clock Pulse Width	t_{WH}	5.0	400	200	–	ns
		10	200	100	–	
		15	160	80	–	
Reset or Preset Enable Pulse Width	t_{WH}	5.0	290	145	–	ns
		10	130	65	–	
		15	110	55	–	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			ns
		10				
		15				
Clock Pulse Frequency	f_{cl}					MHz
		5.0	–	2.5	1.25	
		10	–	6.5	3.25	
		15	–	8.0	4.0	

*The formulas given are for the typical characteristics only.

FIGURE 1 – SWITCHING TIME WAVEFORMS



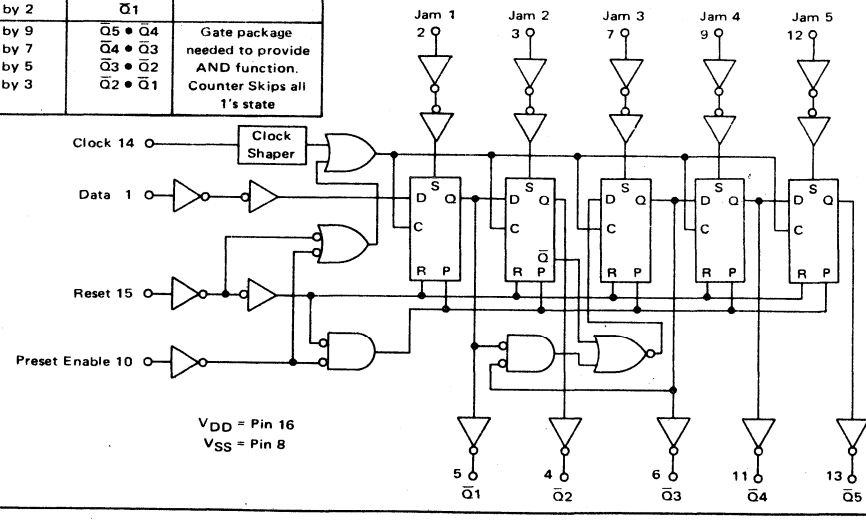
TIMING DIAGRAM
($\overline{Q}$5 Connected to Data Input)



FUNCTION SELECTION

Counter Mode	Connect Data Input (Pin 1) to:	Comments
Divide by 10	$\overline{Q}$5	No external components needed.
Divide by 8	$\overline{Q}$4	
Divide by 6	$\overline{Q}$3	
Divide by 4	$\overline{Q}$2	
Divide by 2	$\overline{Q}$1	
Divide by 9	$\overline{Q}$5 • $\overline{Q}$4	Gate package needed to provide AND function. Counter Skips all 1's state
Divide by 7	$\overline{Q}$4 • $\overline{Q}$3	
Divide by 5	$\overline{Q}$3 • $\overline{Q}$2	
Divide by 3	$\overline{Q}$2 • $\overline{Q}$1	

LOGIC DIAGRAM



MOTOROLA

MC14020B

14-BIT BINARY COUNTER

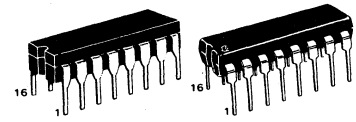
The MC14020B 14-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

- Fully Static Operation
- Quiescent Current =5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Low Input Capacitance = 5.0pF typical
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- 13 MHz Typical Counting Rate @ V_{DD} = 15V
- Pin-for-Pin Replacement for CD4020B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

14-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

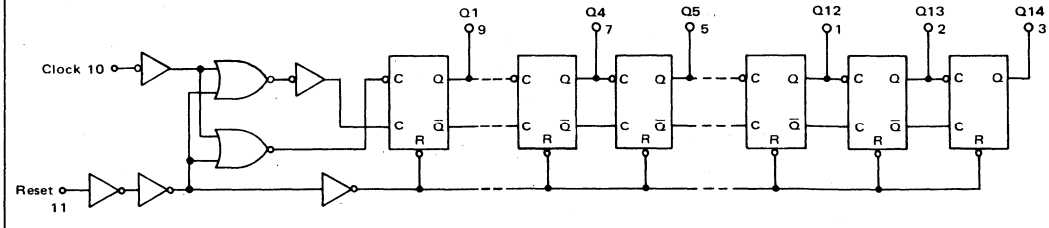
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
↓	0	No Change
↑	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



Q6 = Pin 4
Q7 = Pin 6
Q8 = Pin 13
Q9 = Pin 12
Q10 = Pin 14
Q11 = Pin 15
V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.42 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.85 µA/kHz) f + I_{DD}							
		15	I_T = (1.43 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICE* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q1	t_{PHL}					
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	750	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns		10	–	170	300	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 95 ns		15	–	120	230	
Clock to Q14						μs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 2715 ns		5.0	–	2.8	2.8	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 967 ns		10	–	1.0	2.0	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 575 ns		15	–	0.6	1.5	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 510 ns		5.0	–	595	3500	
t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	900	
t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	180	680	
Clock Pulse Width	t_{WH}	5.0	500	140	–	ns
		10	165	55	–	
		15	125	38	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.5	1.0	MHz
		10	–	9.0	3.0	
		15	–	13	4.0	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Reset Pulse Width	t_{WL}	5.0	3000	320	–	ns
		10	550	120	–	
		15	420	80	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

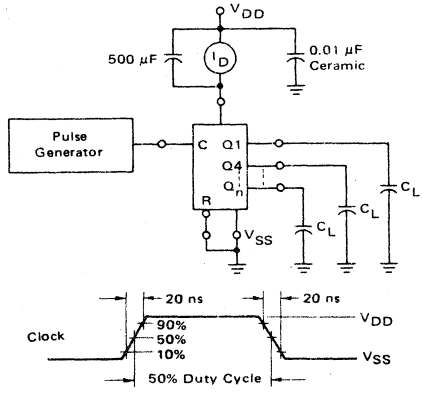


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

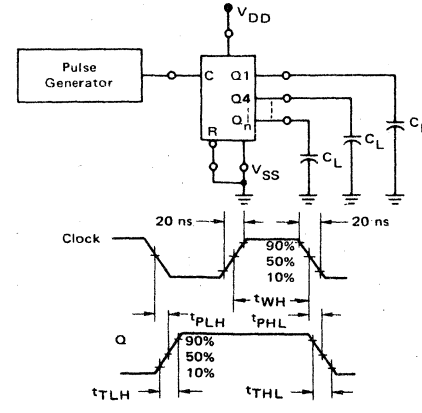
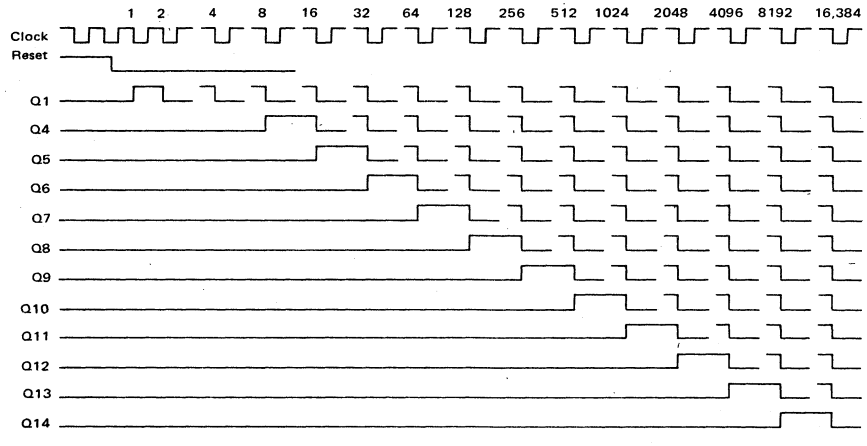


FIGURE 3 – TIMING DIAGRAM



MOTOROLA

MC14021B

FOR COMPLETE DATA
SEE MC14014B

CMOS MSI

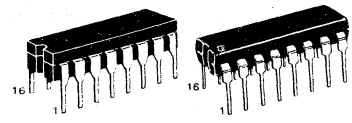
(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER

8-BIT STATIC SHIFT REGISTER

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation from DC to 7.0 MHz
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

SERIAL OPERATION:

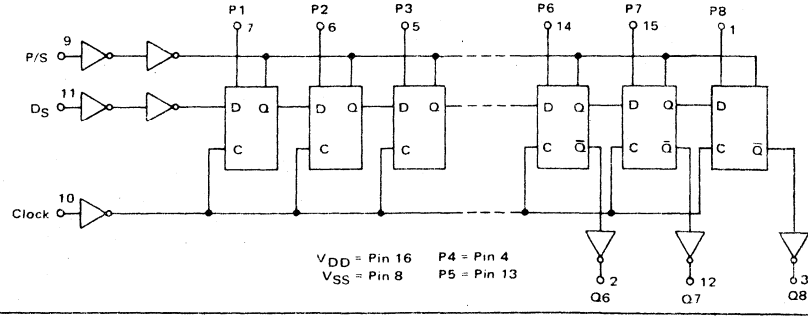
t	CLOCK	D_S	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n		0	0	0	?	?
n+1		1	0	1	0	?
n+2		0	0	0	1	0
n+3		1	0	1	0	1
		X	0	Q6	Q7	Q8

PARALLEL OPERATION:

CLOCK		D_S	P/S	D_M	$*Q_M$
MC14014B	MC14021B				
	X	X	1	0	0
	X	X	1	1	1

*Q6, Q7, & Q8 are available externally
X = Don't Care

LOGIC DIAGRAM



MOTOROLA

MC14022B

CMOS MSI

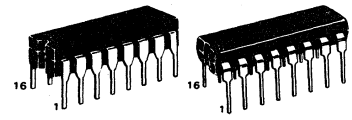
(LOW-POWER COMPLEMENTARY MOS)

OCTAL COUNTER/DIVIDER

OCTAL COUNTER/DIVIDER

The MC14022B is a four-stage Johnson octal counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ V_{DD} = 10 Vdc
- Divide-by-N Counting
- Quiescent Current = 5.0 nA/package Typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4022B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

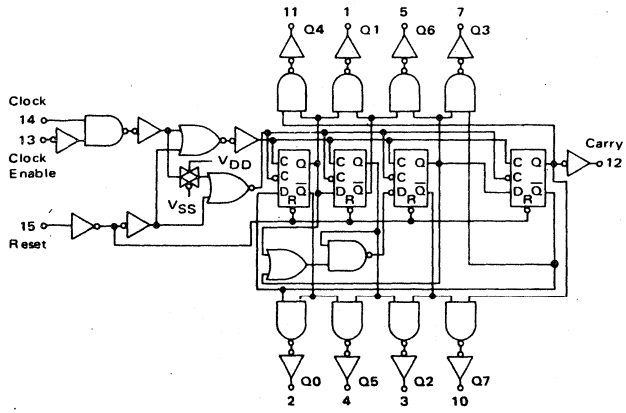
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FUNCTIONAL TRUTH TABLE
(Positive Logic)

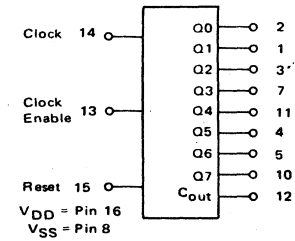
CLOCK	CLOCK ENABLE	RESET	OUTPUT = n
0	X	0	n
X	1	0	n
⌐	0	0	n+1
¬	X	0	n
1	¬	0	n+1
X	⌐	0	n
X	X	1	Q0

X Don't Care If n< 4 Carry = 1, Otherwise = 0

LOGIC DIAGRAM



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.28 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.56 μA/kHz) f + I_{DD}							
		15	I_T = (0.85 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1.25 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

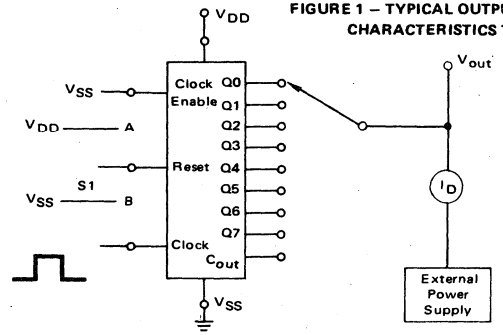
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Reset to Decode Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns		15	–	175	350	
Propagation Delay Time	t_{PLH},					ns
Clock to C_{out}	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 142 ns		10	–	175	350	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 100 ns		15	–	125	250	
Propagation Delay Time	t_{PLH},					ns
Clock to Decode Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = 0.5 ns/pF) C_L + 150 ns		15	–	175	350	
Turn-Off Delay Time	t_{PLH}					ns
Reset to C_{out}						
t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH} = (0.66 ns/pF) C_L + 142 ns		10	–	175	350	
t_{PLH} = (0.5 ns/pF) C_L + 100 ns		15	–	125	250	
Clock Pulse Width	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	75	35	–	
Clock Frequency	f_{cl}	5.0	–	5.0	2.0	MHz
		10	–	12	5.0	
		15	–	16	6.7	
Reset Pulse Width	t_{WH}	5.0	500	250	–	ns
		10	250	125	–	
		15	190	95	–	
Reset Removal Time	t_{rem}	5.0	750	375	–	ns
		10	275	135	–	
		15	210	105	–	
Clock Input Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Clock Enable Setup Time	t_{su}	5.0	350	175	–	ns
		10	150	75	–	
		15	115	52	–	
Clock Enable Removal Time	t_{rem}	5.0	420	260	–	ns
		10	200	100	–	
		15	140	70	–	

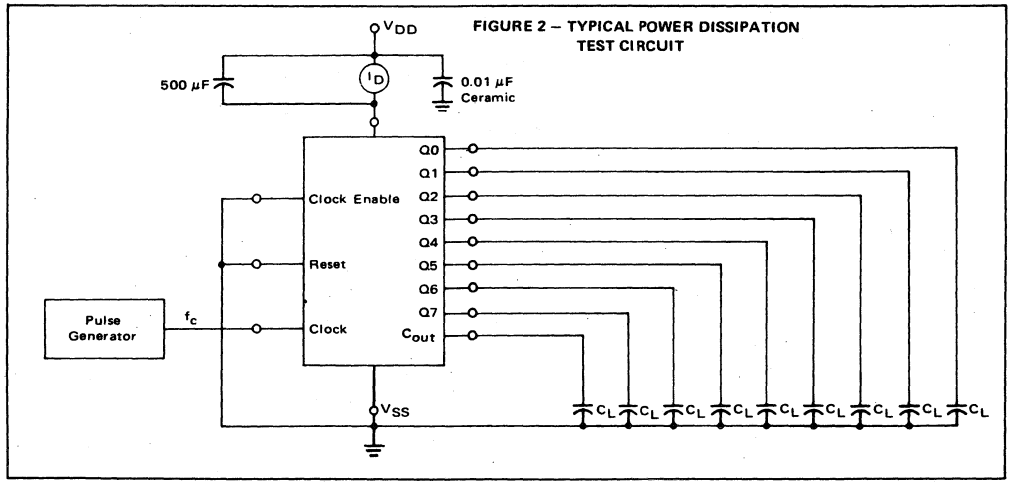
* The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



	Output Sink Drive	Output Source Drive
Outputs	(S1 to A)	Clock to desired Output (S1 to B)
Carry	Clock to Q5 thru Q7 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT



APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 3 – COUNTER EXPANSION

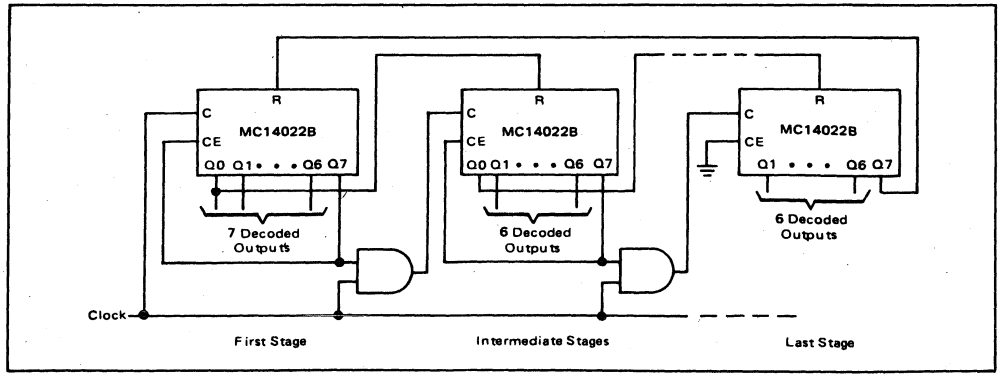
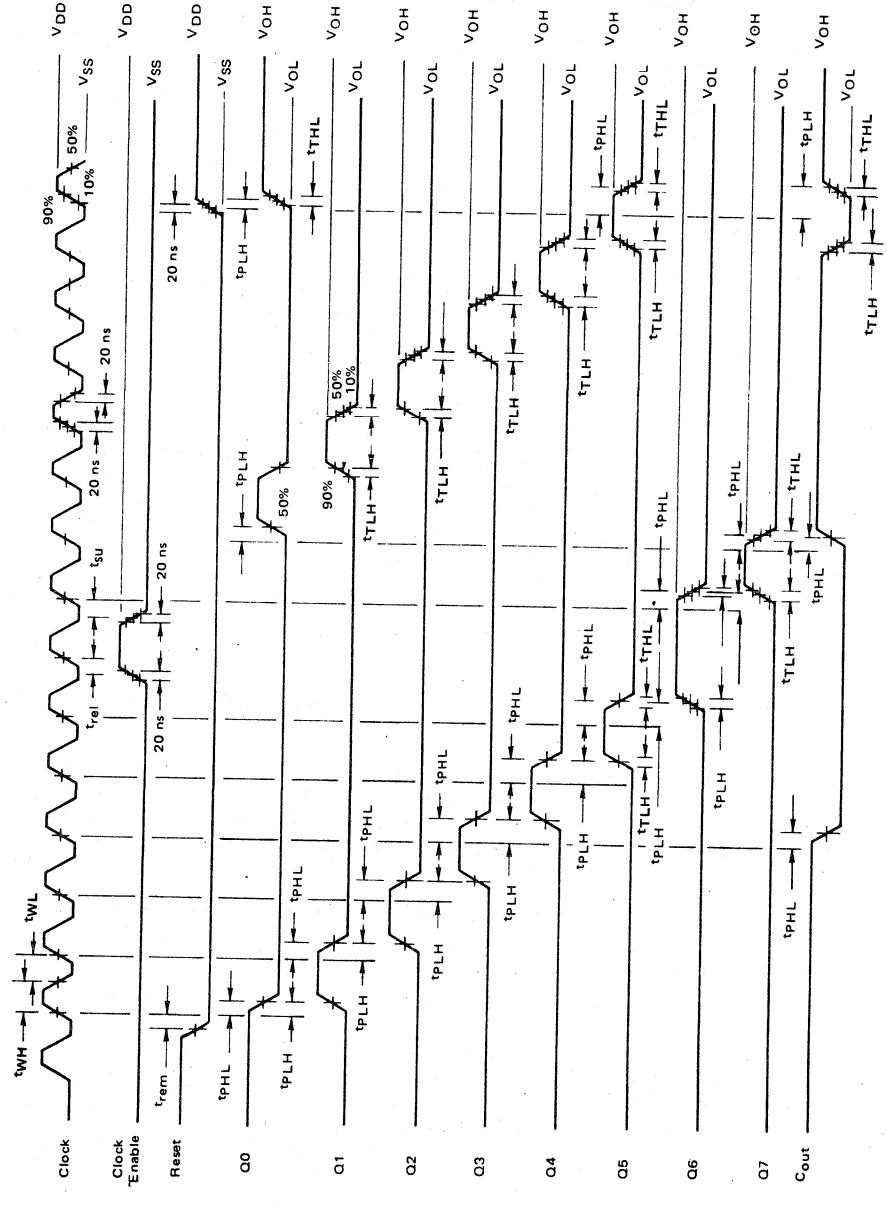


FIGURE 4 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



MOTOROLA

MC14023B
MC14023UB

CMOS SSI

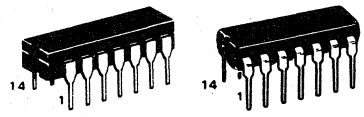
(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "NAND" GATE

TRIPLE 3-INPUT "NAND" GATE

The MC14023B and MC14023UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14023B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14023B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4023B and CD4023UB.



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes
or UB, as applicable
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

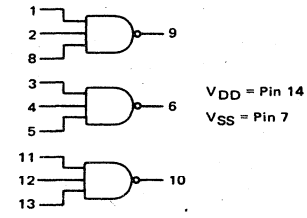
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

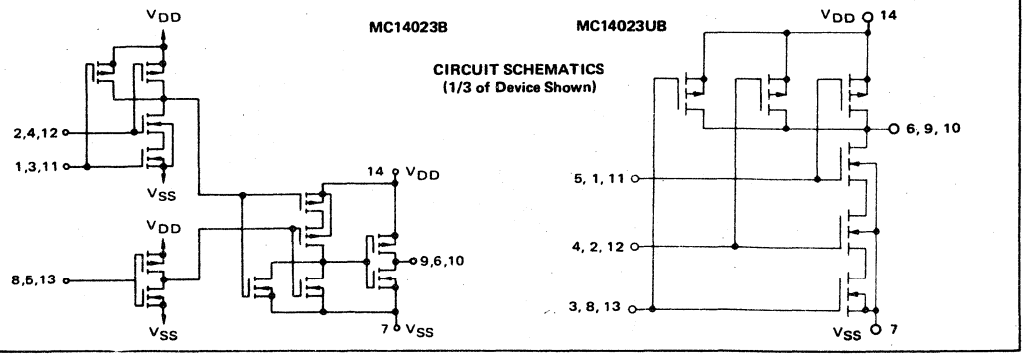
See the MC14001B data sheet for complete characteristics of the B-Series device.

See the MC14001UB data sheet for complete characteristics for the UB device.

LOGIC DIAGRAM



CIRCUIT SCHEMATICS
(1/3 of Device Shown)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14024B

CMOS SSI

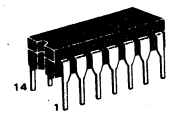
(LOW-POWER COMPLEMENTARY MOS)

SEVEN STAGE
RIPPLE COUNTER

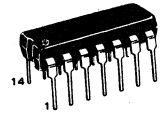
SEVEN STAGE RIPPLE COUNTER

The MC14024B is a seven stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity (typically 45% of V_{DD}), however the Clock input has increased noise immunity due to Hysterrsis, with no maximum Clock input rise or fall time. The output of each counter stage is buffered.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- 8-MHz Operation @ V_{DD} = 10 Vdc typical
- Exceedingly Slow Input Transition Rates may be Applied to the Clock Input
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4024B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

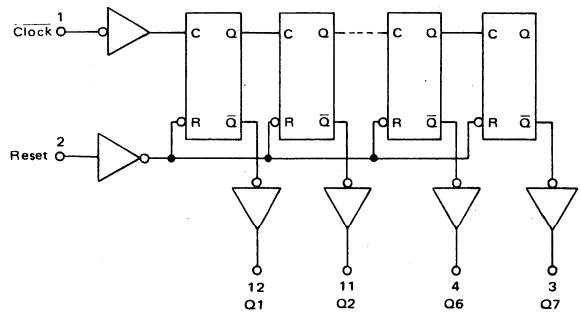
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

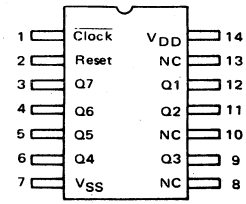
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



Q3 = Pin 9
Q4 = Pin 6
Q5 = Pin 5

PIN ASSIGNMENT



V_{DD} = Pin 14
V_{SS} = Pin 7

NC = No Connection

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.31 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.60 µA/kHz) f + I_{DD}							
		15	I_T = (0.89 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q1						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	–	380	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	150	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	175	
Clock to Q7						
t_{PLH}, t_{PHL} = (1,7 ns/pF) C_L + 915 ns		5.0	–	1000	3000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 367 ns		10	–	400	750	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 275 ns		15	–	300	565	
Reset to Q_n						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	–	250	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	180	300	
Clock Pulse Width	t_{WH}	5.0	500	200	–	ns
		10	165	60	–	
		15	125	40	–	
Reset Pulse Width	t_{WH}	5.0	600	375	–	ns
		10	350	200	–	
		15	260	150	–	
Reset Removal Time	t_{rem}	5.0	625	250	–	ns
		10	190	75	–	
		15	145	50	–	
Clock Input Rise and Fall Times	t_{TLH}, t_{THL}	5.0	No Limit			
		10				
		15				
Input Pulse Frequency	f_{cl}	5.0	–	2.5	1.0	MHz
		10	–	8.0	3.0	
		15	–	12	4.0	

* The formula given is for the typical characteristics only.

TRUTH TABLE

$\overline{CLOCK}$	RESET	STATE
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
⌐	0	No Change
⌐	1	All Outputs Low
⌐	0	Advance One Count
⌐	1	All Outputs Low

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

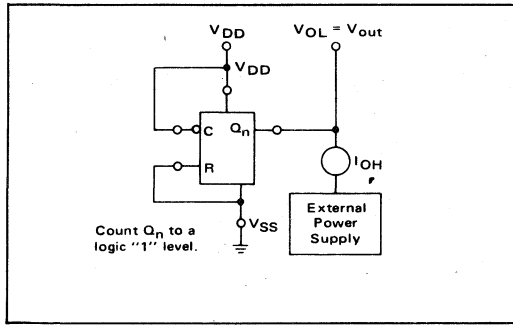


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

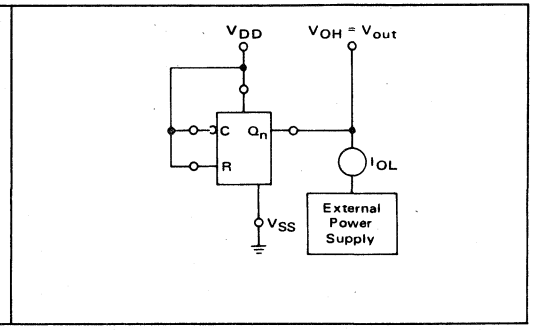


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT

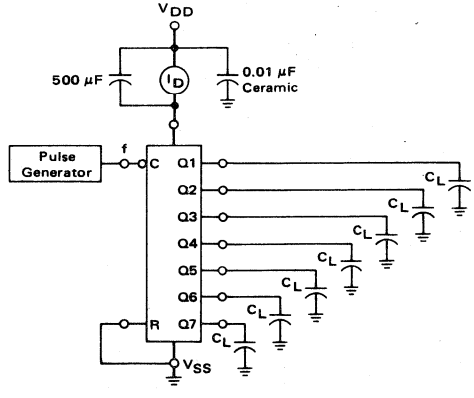
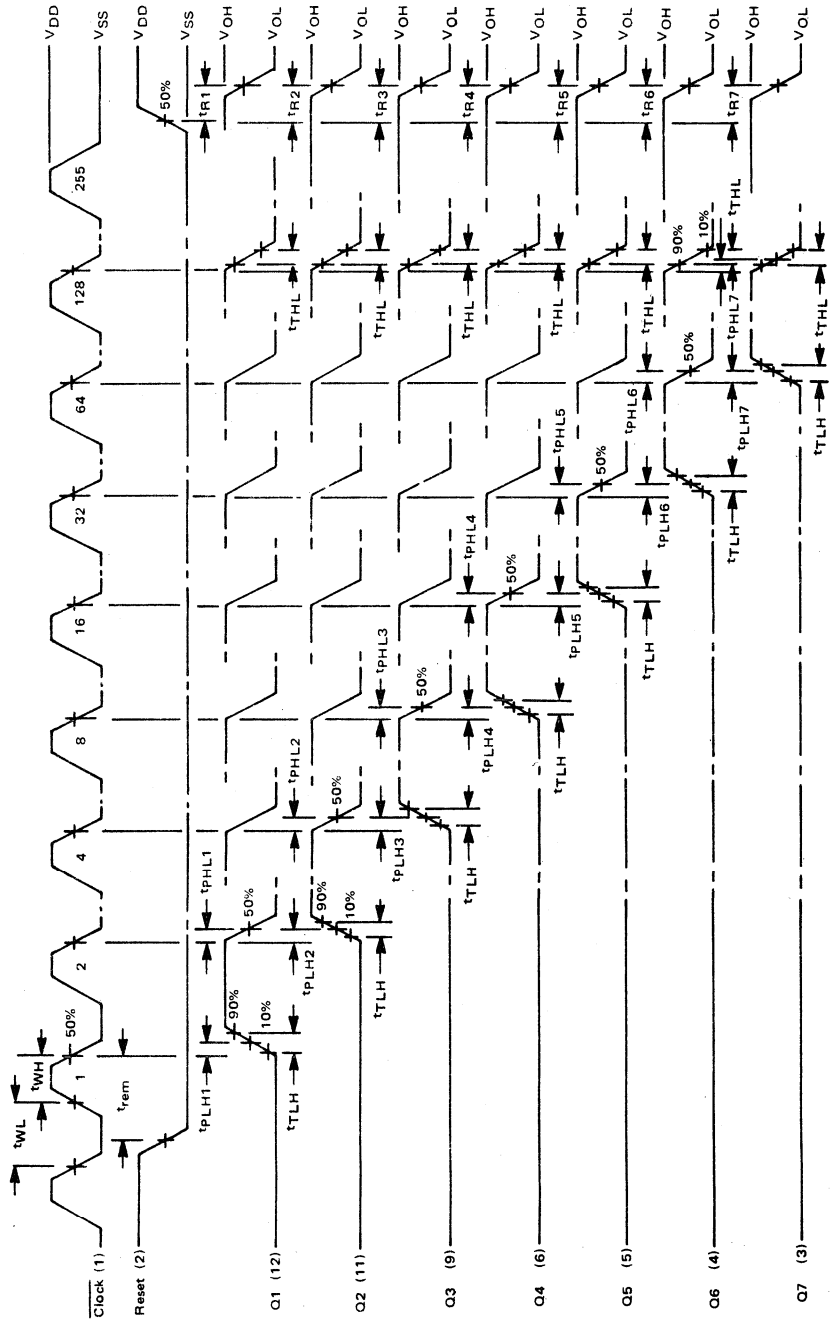


FIGURE 4 – FUNCTIONAL WAVEFORMS



MOTOROLA

MC14025B
MC14025UB

TRIPLE 3-INPUT "NOR" GATE

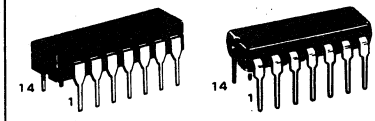
The MC14025B and MC14025UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14025B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14025B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4025B and CD4025UB.

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB ___ Suffix — Denotes

or UB, as applicable

- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

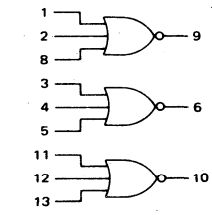
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics of the B-Series device.

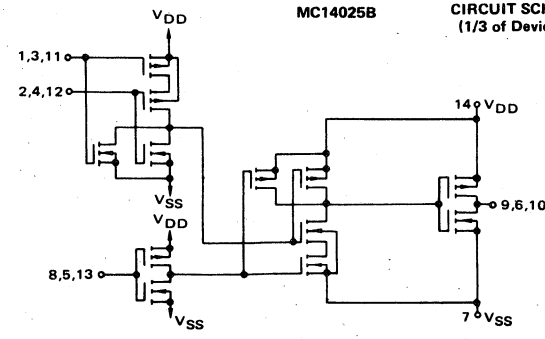
See the MC14001UB data sheet for complete characteristics for the non-B device.

LOGIC DIAGRAM

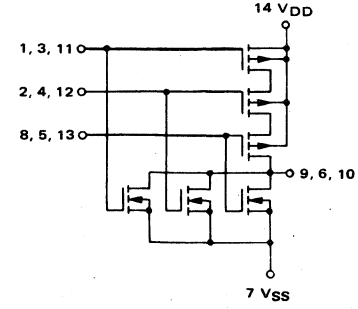


CIRCUIT SCHEMATICS
(1/3 of Device Shown)

MC14025B



MC14025UB



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14027B

DUAL J-K FLIP-FLOP

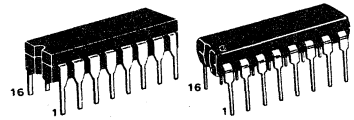
The MC14027B dual J-K flip-flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- Toggle Rate = 3.0 MHz typical @ 5 Vdc
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4027B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL J-K FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

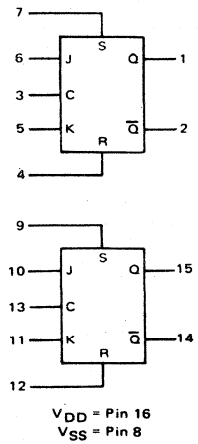
TRUTH TABLE

INPUTS						OUTPUTS*		
C†	J	K	S	R	Q_n‡	Q_{n+1}	$\overline{Q_{n+1}}$	
⎍	1	X	0	0	0	1	0	
⎍	X	0	0	0	1	1	0	
⎍	0	X	0	0	0	0	1	
⎍	X	1	0	0	1	0	1	
⎎	X	X	0	0	X	Q_n	$\overline{Q_n}$	No Change
X	X	X	1	0	X	1	0	
X	X	X	0	1	X	0	1	
X	X	X	1	1	X	1	1	

X = Don't Care
† = Level Change
‡ = Present State
* = Next State

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.80 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.60 µA/kHz) f + I_{DD}							
		15	I_T = (2.40 µA/kHz) f + I_{DD}							

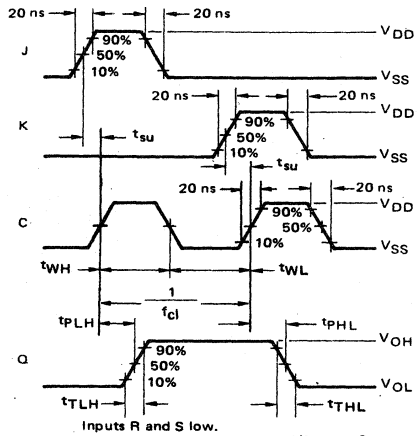
*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Set to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	ns
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	350	450	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	200	ns
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 50 ns		15	–	75	150	
Setup Times	t_{su}	5.0	140	70	–	ns
		10	50	25	–	
		15	35	17	–	
Minimum Hold Times	t_h	5.0	140	70	–	ns
		10	50	25	–	
		15	35	17	–	
Clock Pulse Width	t_{WH}, t_{WL}	5.0	330	165	–	ns
		10	110	55	–	
		15	75	38	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	9.0	4.5	
		15	–	13	6.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5.0	
		15	–	–	4.0	
Set and Reset Pulse Width	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	70	35	–	

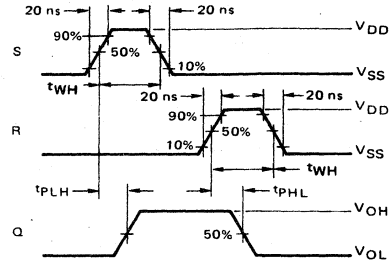
* The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS
(J, K, Clock, and Output)



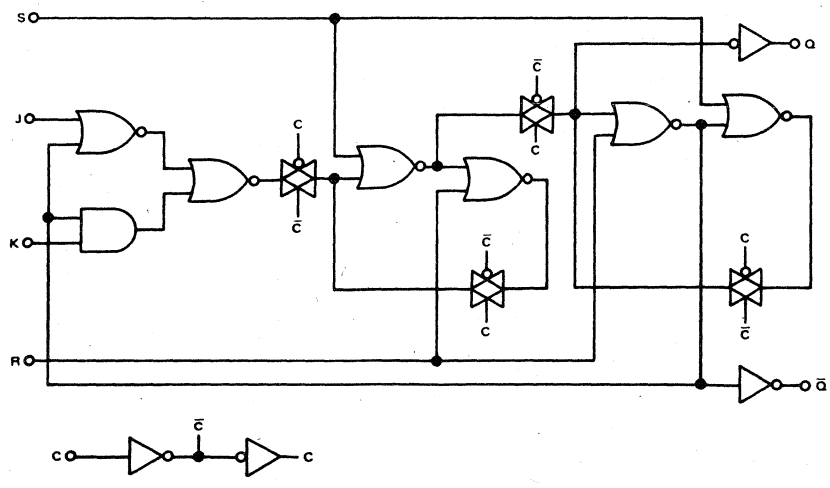
Inputs R and S low.
For the measurement of t_{WH}, $1/f_{cl}$, and P_D the Inputs J and K are kept high.

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, and Output)



Inputs J and K low.

LOGIC DIAGRAM
(1/2 of Device Shown)



MOTOROLA

MC14028B

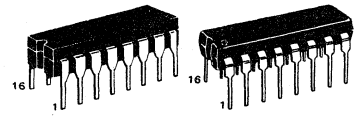
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-DECIMAL DECODER
BINARY-TO-OCTAL DECODER

The MC14028B decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0". Expanded decoding such as binary-to-hexadecimal (one-of-16), etc., can be achieved by using other MC14028B devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Positive Logic Design
- Quiescent Current 5.0 nA /package typical @ 5 Vdc
- Low Outputs on All Illegal Input Combinations
- Similar to CD4028B.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

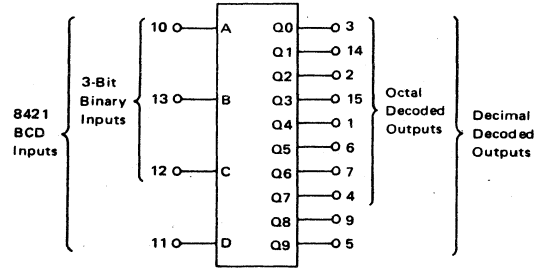
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUT				OUTPUT									
D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.6 µA/kHz) f + I_{DD}							
		15	I_T = (0.9 µA/kHz) f + I_{DD}							

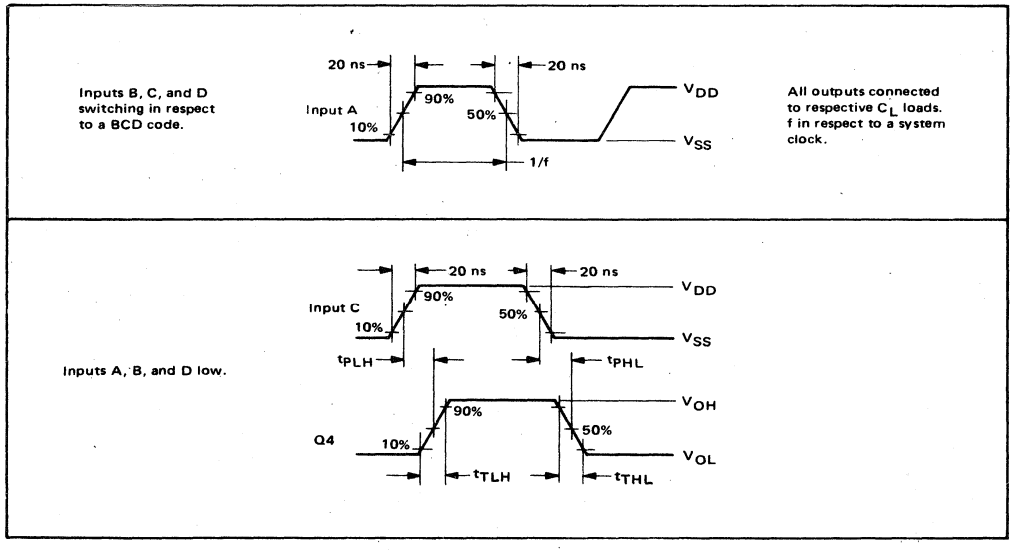
*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns	t_{PHL}	5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	

* The formula given is for the typical characteristics only.

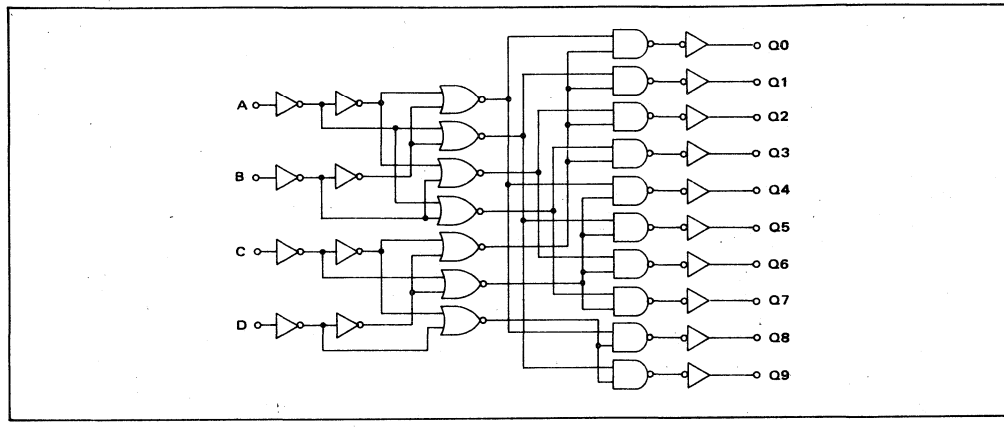
FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

LOGIC DIAGRAM

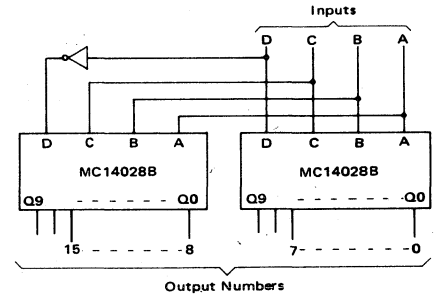


APPLICATION INFORMATION

Expanded decoding can be performed by using the MC14028B and other McMOS Integrated Circuits. The circuits in Figure 2 converts any 4-bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4-bit binary, 4-bit gray, excess-3, or excess-3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6-bit binary 1-of-64 decoder using nine MC14028B circuits and two MC14069B inverters.

The MC14028B can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

FIGURE 2 – CODE CONVERSION CIRCUIT AND TRUTH TABLE



INPUTS				OUTPUT NUMBERS																CODE AND REDEFINED OUTPUT NUMBERS					
																				Hexadecimal		Decimal			
D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4-Bit Binary	4-Bit Gray	Excess-3	Excess-3 Gray	Aiken	4221
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0			0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1			1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3		0	2	2
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	0	3	3	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4	4	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	5	6	2			3
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	6	4	3	1		4
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	7	5	4	2		
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8	15	5			
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	9	14	6			5
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	10	12	7	9		6
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11	13	8		5	
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6	
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7	7
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11		8	8	8
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9	9

FIGURE 3 – SIX-BIT BINARY 1-OF-64 DECODER

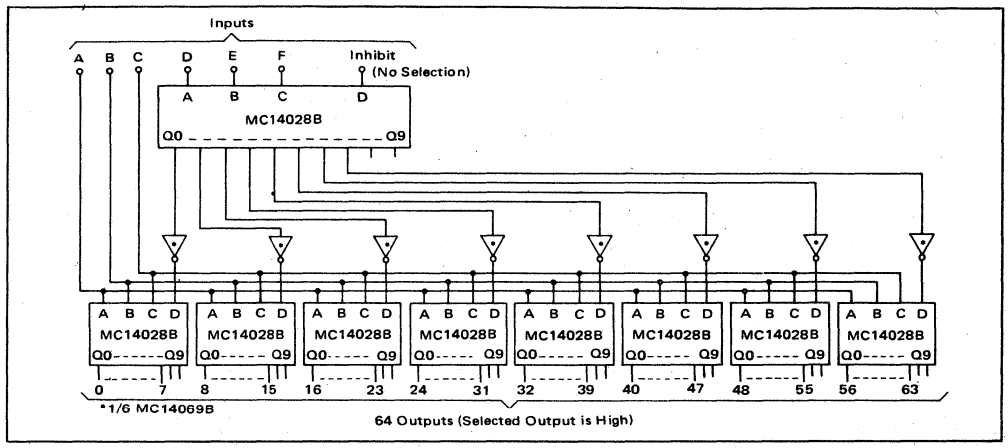
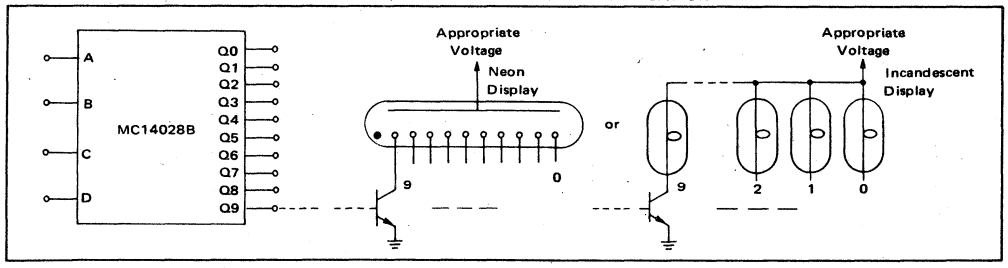


FIGURE 4 – DECIMAL DIGIT DISPLAY APPLICATION



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14029B

BINARY/DECADE UP/DOWN COUNTER

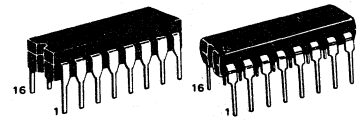
The MC14029B Binary/Decade up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide toggle flip-flop capability. The counter can be used in either Binary or BCD operation. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Quiescent Current = 5.0 nA/package typical @ 5.0 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Proection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance – 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design – Count Occurs on Positive Going Edge of Clock
- 8.0 MHz Counting Rate Typ at 10 Vdc
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin for Pin Replacment for CD4029B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BINARY/DECADE
UP/DOWN COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

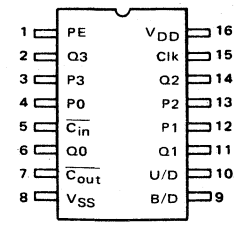
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN ASSIGNMENTS



TRUTH TABLE

$\overline{\text{Carry In}}$	Up/Down	Preset Enable	Action
1	X	0	No Count
0	1	0	Count Up
0	0	0	Count Down
X	X	1	Preset

X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.7	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types Min	All Types Typ	All Types Max	Unit
Output Rise Time	t_{TLH}					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_r = (1.5 ns/pF) C_L +15 ns		10	–	50	100	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clk to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	90	180	
Clk to $\overline{C_{out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	250	500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	85	190	
$\overline{C_{in}}$ to $\overline{C_{out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	–	50	100	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	50	100	
PE to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	235	470	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	80	160	
PE to $\overline{C_{out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	320	640	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	105	210	
Clock Pulse Width	$t_{W(cl)}$	5.0	–	90	180	ns
		10	–	40	80	
		15	–	30	60	
Clock Pulse Frequency	f_{cl}	5.0	2.0	4.0	–	MHz
		10	4.0	8.0	–	
		15	5.0	10	–	
Preset Removal Time**	t_{rem}	5.0	–	80	160	ns
		10	–	40	80	
		15	–	30	60	
Clock Rise and Fall Time	$t_{r(cl)}$	5.0	–	–	15	μs
	$t_{f(cl)}$	10	–	–	15	
		15	–	–	15	
$\overline{Carry}$ In Setup Time	t_{su}	5.0	140	70	–	ns
		10	60	30	–	
		15	40	20	–	
Up/Down Setup Time		5.0	340	170	–	ns
		10	140	70	–	
		15	100	50	–	
Binary/Decade Setup Time		5.0	320	160	–	ns
		10	140	70	–	
		15	100	50	–	
Preset Enable Pulse Width	t_W	5.0	130	65	–	ns
		10	70	35	–	
		15	50	25	–	

*The formula given is for the typical characteristics only.

**The Preset Signal must be low prior to a positive-going transition of the clock.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

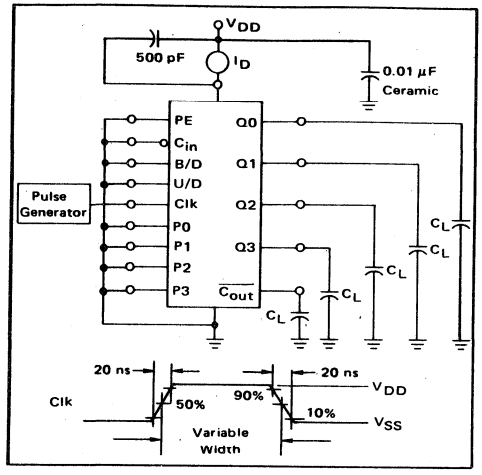
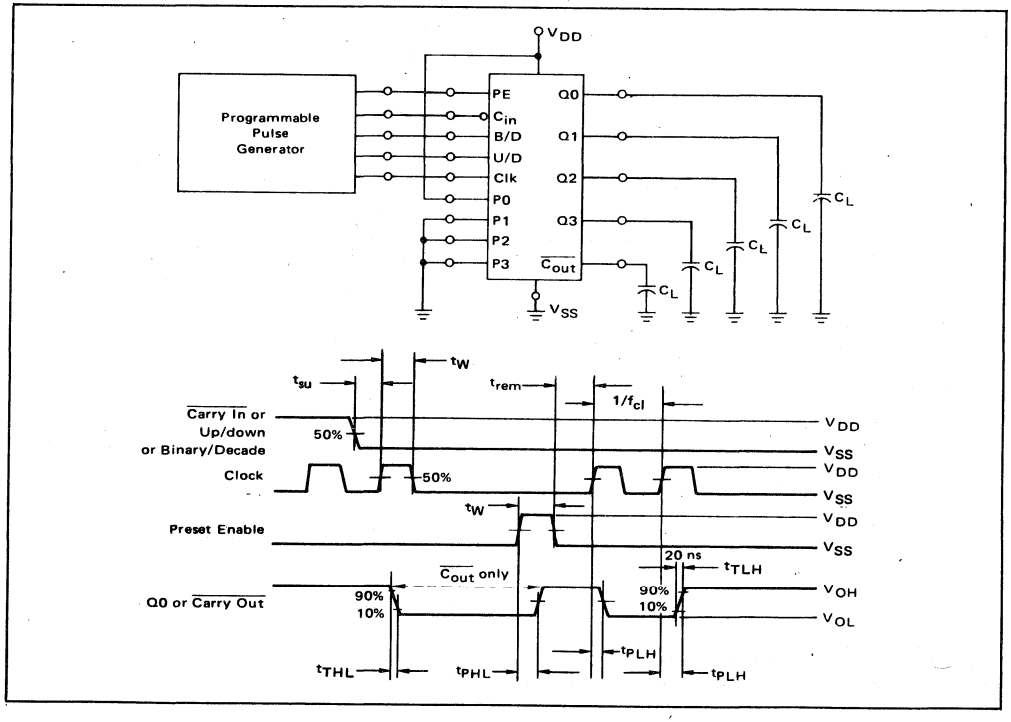


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TIMING DIAGRAM

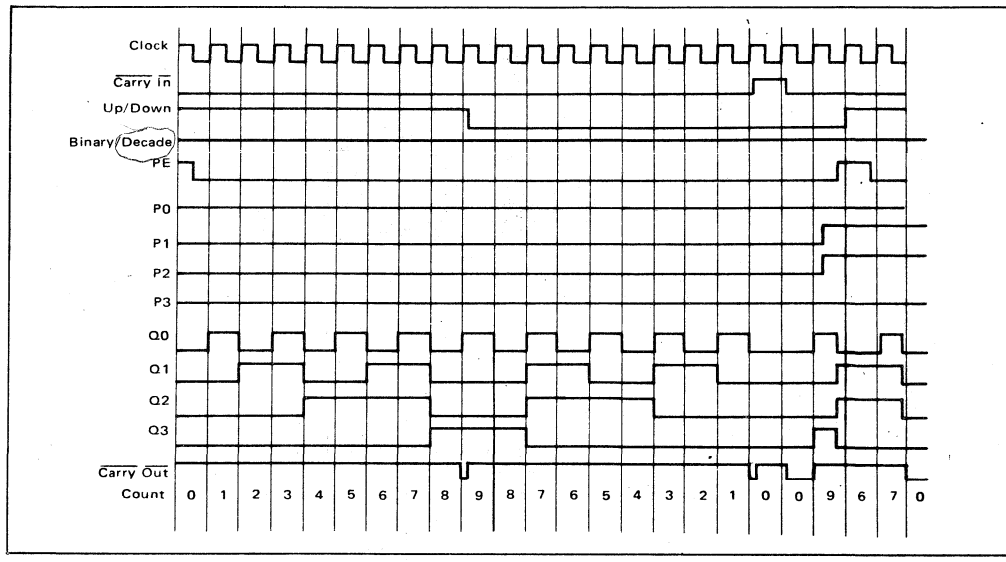
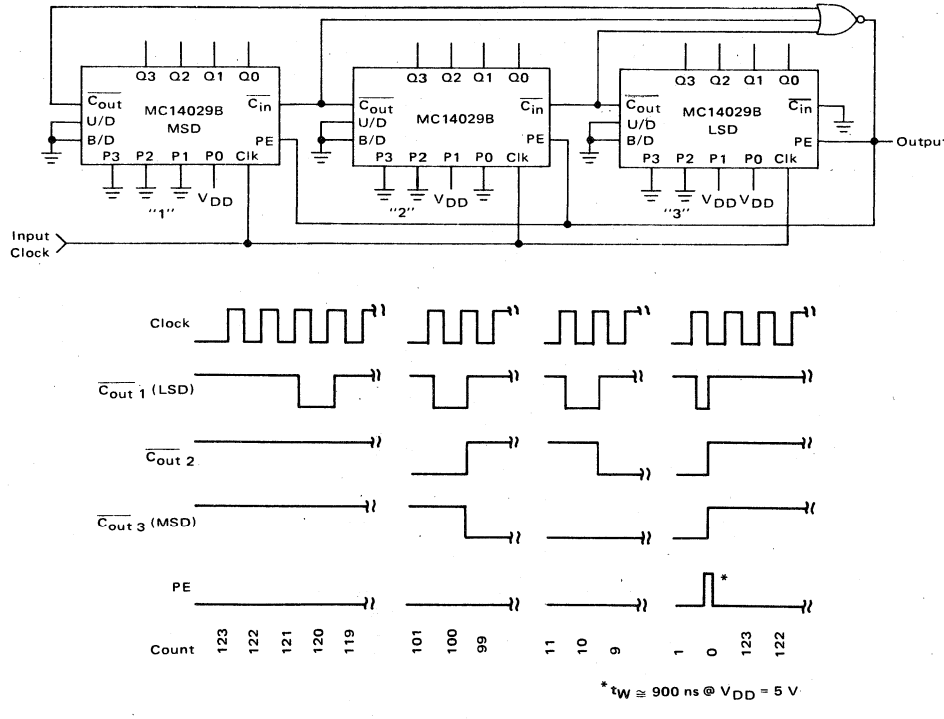
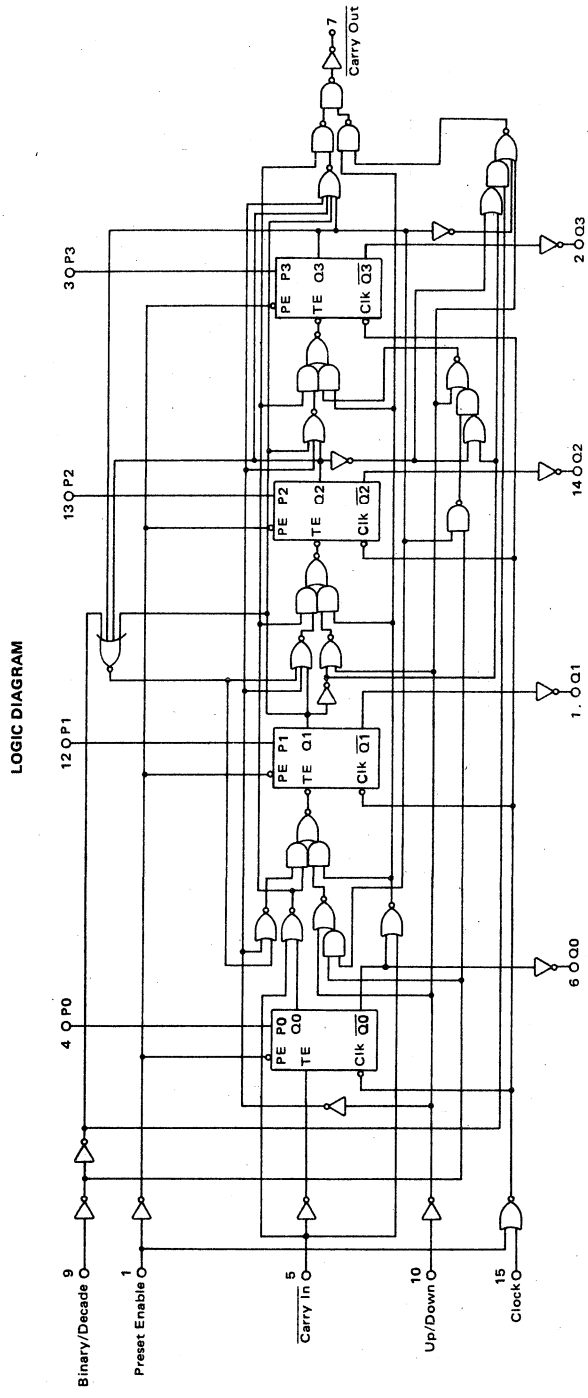


FIGURE 3 – DIVIDE BY N BCD DOWN COUNTER and TIMING DIAGRAM
(Shown for N = 123)



*$t_W \cong 900$ ns @ $V_{DD} = 5$ V

LOGIC DIAGRAM



MOTOROLA

MC14032B
MC14038B

CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

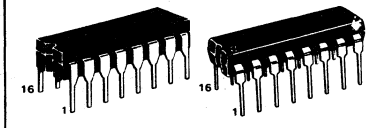
TRIPLE SERIAL ADDERS

Positive Logic — MC14032B
Negative Logic — MC14038B

TRIPLE SERIAL ADDERS

The MC14032B and MC14038B triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032B, and on the negative-going clock transition for the MC14038B. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

- Static Operation from dc to 5.0 MHz
- Buffered Outputs
- Single-Phase Clocking
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4032B and CD4038B.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

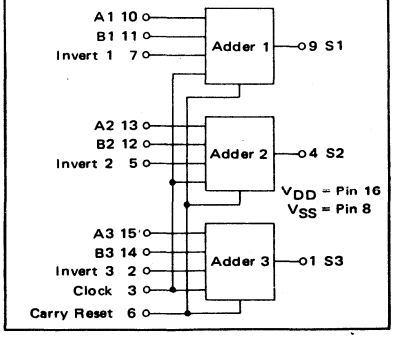
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

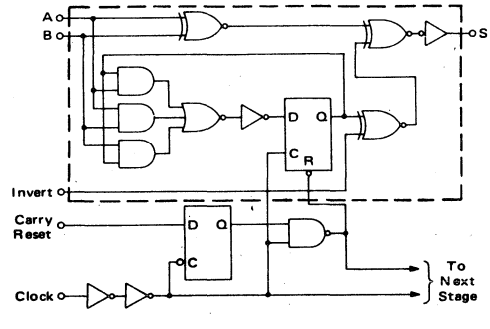
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM

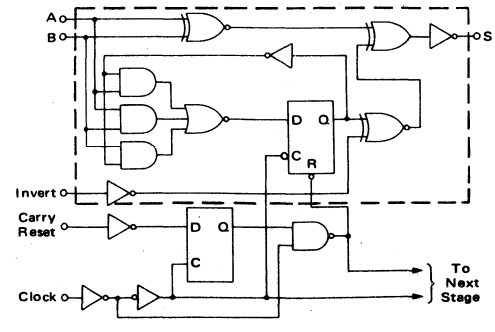


LOGIC DIAGRAMS
(ONE SECTION AND COMMON INPUTS SHOWN)

MC14032B



MC14038B



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.96 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.93 μA/kHz) f + I_{DD}							
		15	I_T = (2.8 μA/kHz) f + I_{DD}							

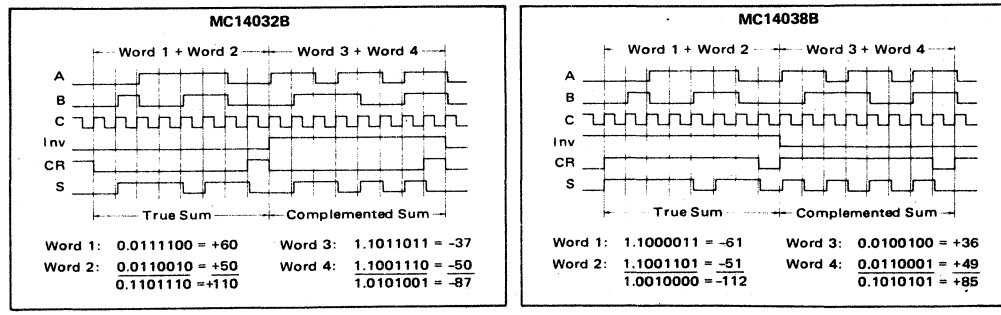
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
A, B or Invert to Sum						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 195 ns		5.0	–	280	1400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns		10	–	120	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	230	
Clock to Sum						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	2400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 110 ns		15	–	135	450	
Input Setup Time	t_{su}	5.0	10	-10	–	ns
		10	10	0	–	
		15	10	0	–	
Clock Pulse Frequency	f_{cl}	5.0	–	4.0	1.0	MHz
		10	–	10	2.5	
		15	–	12	4.0	
Clock Rise and Fall Times	t_{THL}, t_{TLH}	5.0	–	–	15	µs
		10	–	–	15	
		15	–	–	15	

* The formula given is for the typical characteristics only.

TIMING DIAGRAMS



Note: Unused input pins must be connected to either V_{DD} or V_{SS}.

FIGURE 1 – TYPICAL OUTPUT SOURCE TEST CIRCUIT

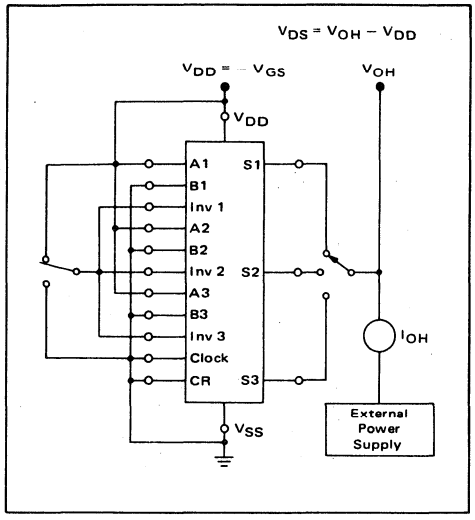


FIGURE 2 – TYPICAL OUTPUT SINK TEST CIRCUIT

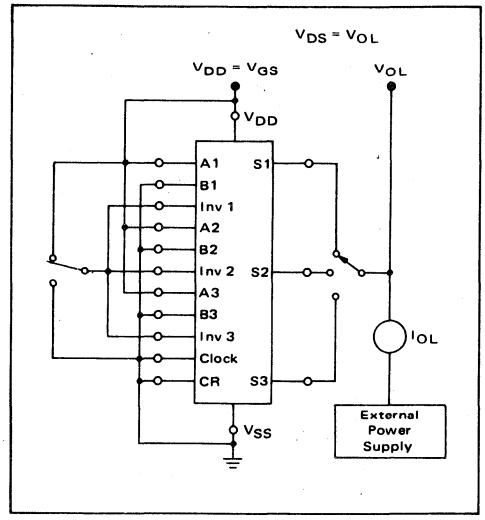


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

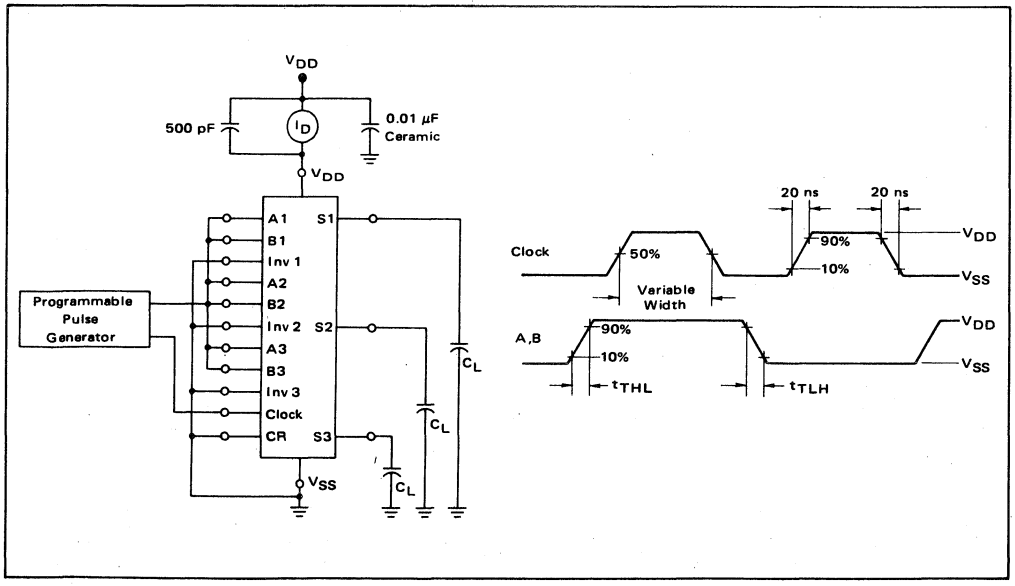
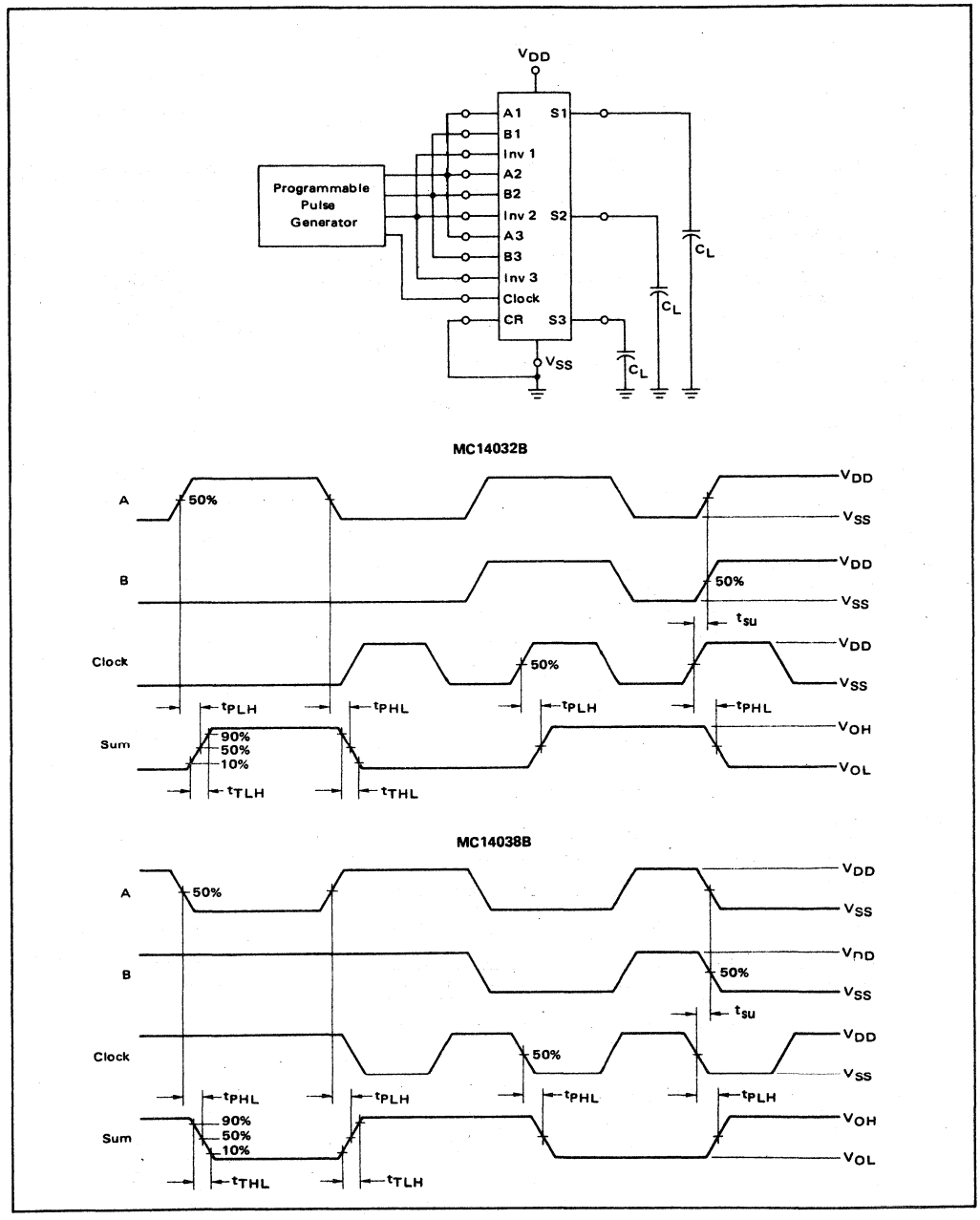


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MOTOROLA

MC14034B

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

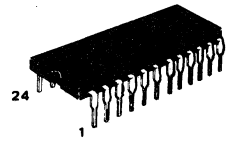
8-BIT UNIVERSAL BUS REGISTER

8-BIT UNIVERSAL BUS REGISTER

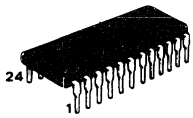
The MC14034B is a bidirectional 8-bit static parallel/serial, input/output bus register. The device contains two sets of input/output lines which allows the bidirectional transfer of data between two buses; the conversion of serial data to parallel form, or the conversion of parallel data to serial form. Additionally the serial data input allows data to be entered shift/right, while shift/left can be accompolished by hard-wiring each parallel output to the previous parallel bit input.

Other useful applications for this device include pseudo-random code generation, sample and hold register, frequency and phase-comparator, address or buffer register, and serial/parallel input/output conversions.

- Bidirectional Parallel Data Input
- Quiescent Current = 10 nA/package typical @ 5 Vdc
- Noise Immunity = 45 % of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Static Operation 0 to 5.0 MHz @ V_{DD} = 10 Vdc
- Single Supply Operation = Positive or Negative
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4034B.



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

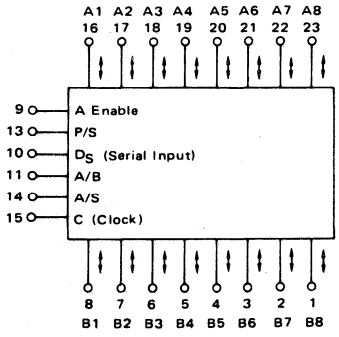
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	–0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (2.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (4.4 µA/kHz) f + I_{DD}							
		15	I_T = (6.6 µA/kHz) f + I_{DD}							
3-State Output Leakage Current (AL Device)	I_{TL}	15	– –	±0.1	– –	±0.0001	±0.1	– –	±3.0	µAdc
3-State Output Leakage Current (CL/CP Device)	I_{TL}	15	– –	±1.0	– –	±0.0001	±1.0	– –	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time A or B	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time A or B	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time						
A (B) Synchronous Paralles Data Input,	t_{PLH},					ns
B (A) Parallel Data Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 440 ns		5.0	–	525	1050	
t_{PHL}, t_{PHL} = (0.66 ns/pF) C_L + 172 ns		10	–	205	410	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 120 ns		15	–	145	290	
Propagation Delay Time						
A (B) Asynchronous Parallel Data Input	t_{PLH},					ns
B (A) Parallel Data Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 420 ns		5.0	–	505	1010	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	–	130	260	
Clock Pulse Width	t_{WH}	5.0	340	170	–	
		10	140	70	–	
		15	110	55	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.2	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Clock Pulse Rise	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
A, B Input Setup Time	t_{su}	5.0	100	35	–	ns
		10	45	15	–	
		15	35	12	–	
High Level SE, P/S, A/S Pulse Width	t_{WH}	5.0	600	200	–	ns
		10	270	90	–	
		15	200	80	–	

* The formula given is for the typical characteristics.

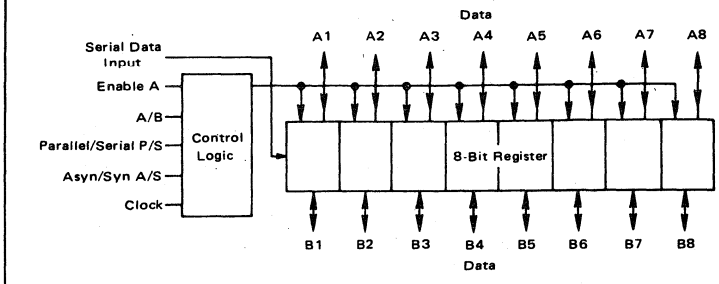
TRUTH TABLE

"A" Enable	P/S	A/B	A/S	MODE	OPERATION†
0	0	0	X	Serial	Synchronous Serial data input, A and B parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs.
1	0	0	X	Serial	Synchronous serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous serial data input, B-Parallel data output.
1	1	0	0	Parallel	B-Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B-Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A-Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A-Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

†Outputs change at positive transition of clock in the serial mode and when the A/S input is low in the parallel mode. During transfer from parallel to serial operation, A/S should remain low in order to prevent D_S transfer into flip-flops.

EXPANDED BLOCK DIAGRAM



OPERATING CHARACTERISTICS

The MC14034B is composed of eight register cells connected in cascade with additional control logic. Each register cell is composed of one "D" master-slave flip-flop with separate internal clocks, and two data transfer gates allowing the data to be transferred bidirectionally from bus A to bus B and from bus B to bus A, and to be memorized. Besides the single phase clock and the serial data inputs, the control logic provides four other features:

A Enable Input – When high, this input enables the bus A data lines.

A/B Input (Data A or B) – This input controls the direction of data flow: when high, the data flows from bus A to bus B; when low, the data flows from bus B to bus A.

P/S Input (Parallel/Serial) – This input controls the data input mode (parallel or serial). When high, the data is transferred to the register in a parallel asynchronous mode or a parallel synchronous mode (positive clock transition). When low, the data is entered into the register in a serial synchronous mode (positive clock transition).

A/S Input (Asynchronous/Synchronous to the Clock) – When this input is high, the data is transferred independently from the clock rate; when low, the clock is enabled and the data is transferred synchronously.

LOGIC DIAGRAM

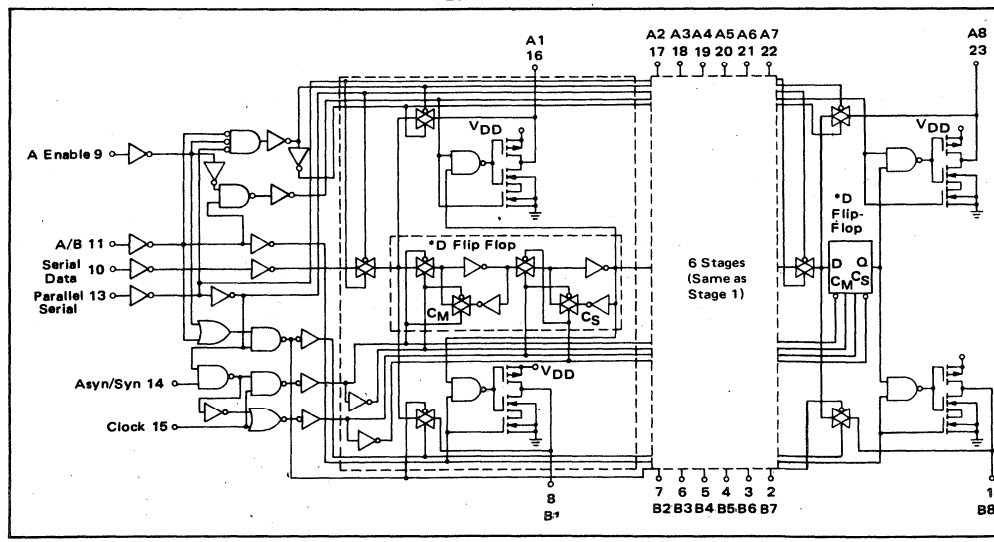
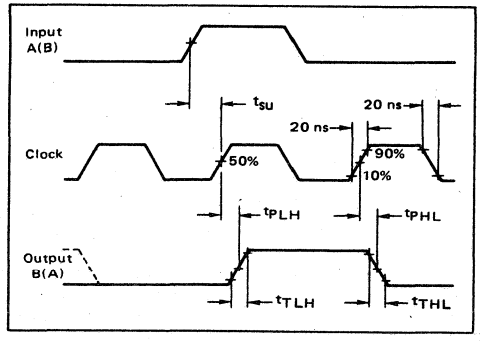


FIGURE 1 – PROPAGATION DELAY AND TRANSITION TIMES WAVEFORMS



PROPAGATION AND TRANSITION TIME TEST CIRCUITS

FIGURE 2 – A SYNCHRONOUS DATA INPUT, B PARALLEL DATA OUTPUT AND SETUP TIME

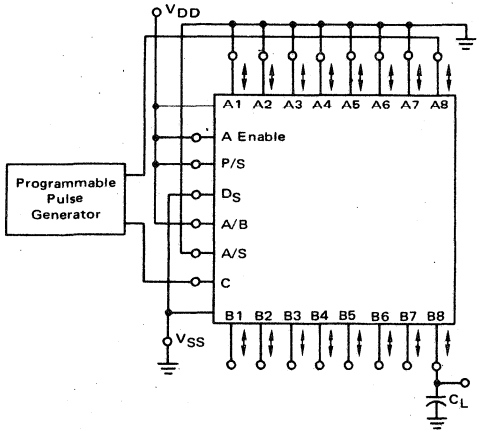


FIGURE 3 – B SYNCHRONOUS DATA INPUT, B PARALLEL DATA OUTPUT AND SETUP TIME

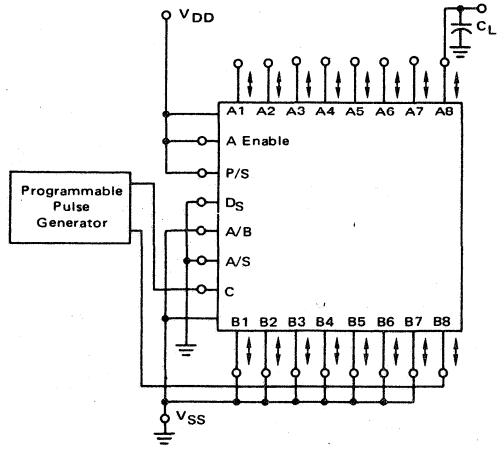


FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

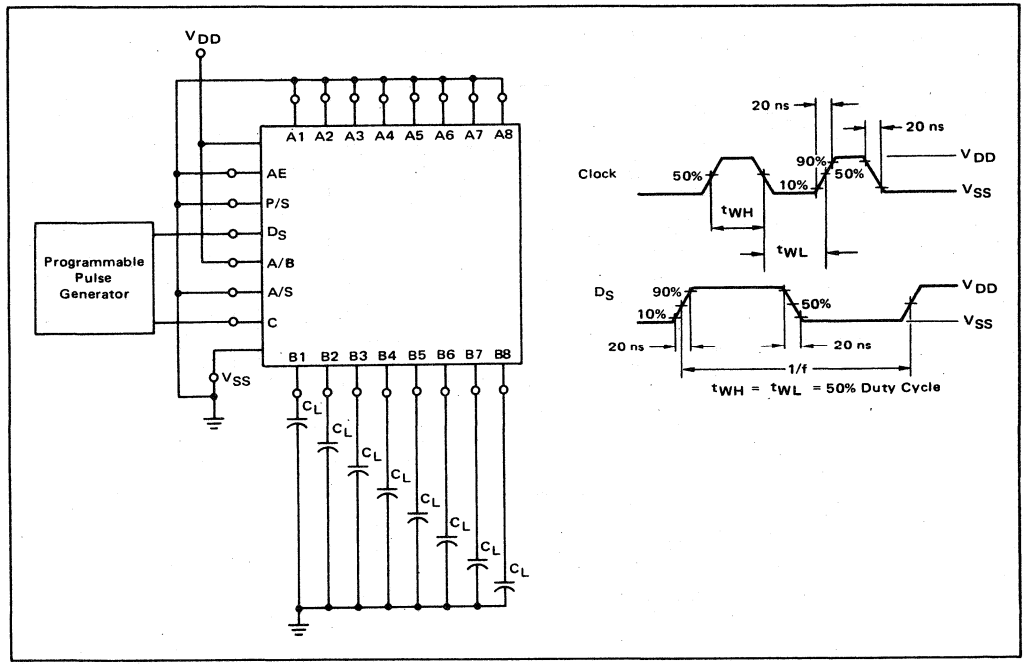


FIGURE 5 – 16-BIT PARALLEL IN/PARALLEL OUT, PARALLEL IN/SERIAL OUT, SERIAL IN/PARALLEL OUT, SERIAL IN/SERIAL OUT REGISTER

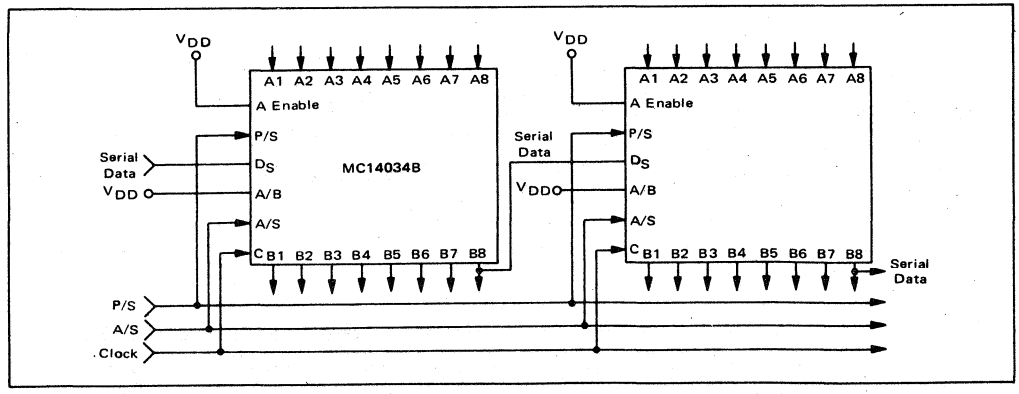
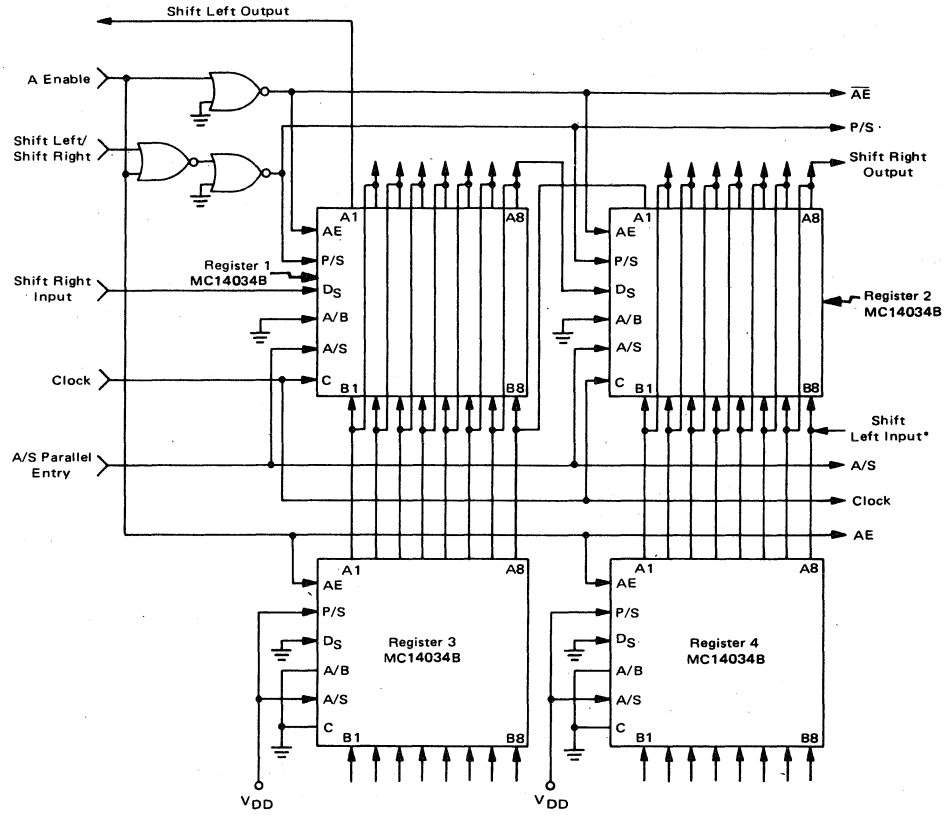


FIGURE 6 – SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUTS



A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

*Shift left input must be disabled during parallel entry.

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14035B

4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

The MC14035B 4-bit shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of a 4-stage clocked serial-shift register with synchronous parallel inputs and buffered parallel outputs. The Parallel/Serial (P/S) input allows serial-right shifting of data or synchronous parallel loading via inputs D_{P0} thru D_{P3}. The True/Complement (T/C) input determines whether the outputs display the Q or $\overline{Q}$ outputs of the flip-flop stages. J-K logic forms the serial input to the first stage. With the J and K inputs connected together they operate as a serial "D" input.

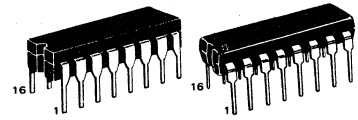
This device may be effectively used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, sample and hold registers, etc. . .

- 4-Stage Clocked Serial-Shift Operation
- Synchronous Parallel Loading of all Four Stages
- J-K Serial Inputs on First Stage
- Asynchronous True/Complement Control of all Outputs
- Fully Static Operation
- Asynchronous Master Reset
- Data Transfer Occurs on the Positive-Going Clock Transition
- No Limit on Clock Rise and Fall Times
- All Inputs are Buffered
- 6.0 MHz Operation @ V_{DD} = 10 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT
PARALLEL-IN/PARALLEL-OUT
SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

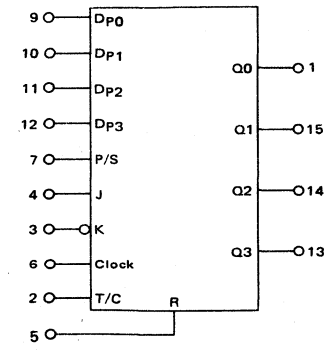
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS				t_n OUTPUT
C	J	$\overline{K}$	R	Q0
⎍	0	0	0	0
⎍	0	1	0	Q0 (n - 1)
⎍	1	0	0	$\overline{Q0}$ (n - 1)
⎍	1	1	0	1
⎎	x	x	0	Q0 (n - 1)
x	x	x	1	0

x = Don't Care
P/S = 0 = Serial Mode
T/C = 1 = True Outputs

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	**0.005**	5.0	–	150	μAdc
(Per Package)		10	–	10	–	**0.010**	10	–	300	
		15	–	20	–	**0.015**	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	**0.005**	20	–	150	μAdc
(Per Package)		10	–	40	–	**0.010**	40	–	300	
		15	–	80	–	**0.015**	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.0 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.0 μA/kHz) f + I_{DD}							
		15	I_T = (3.0 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

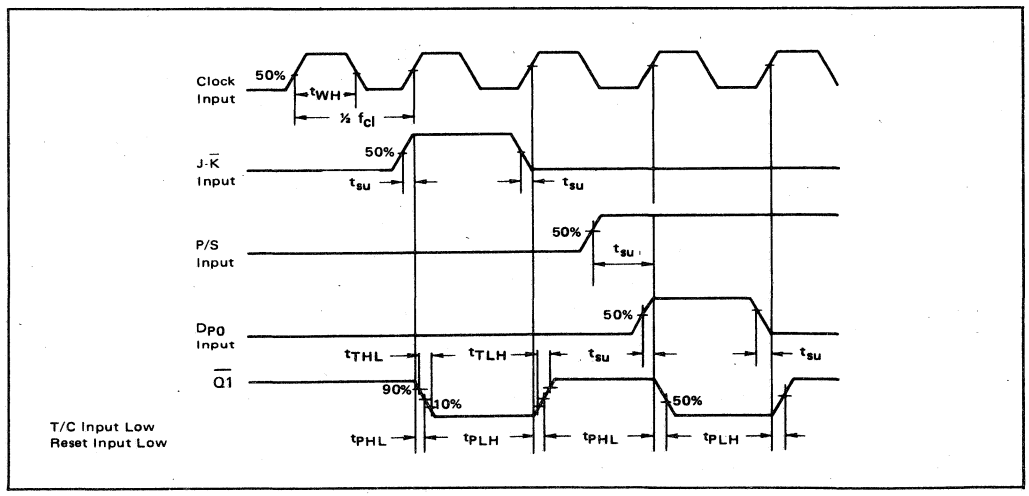
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

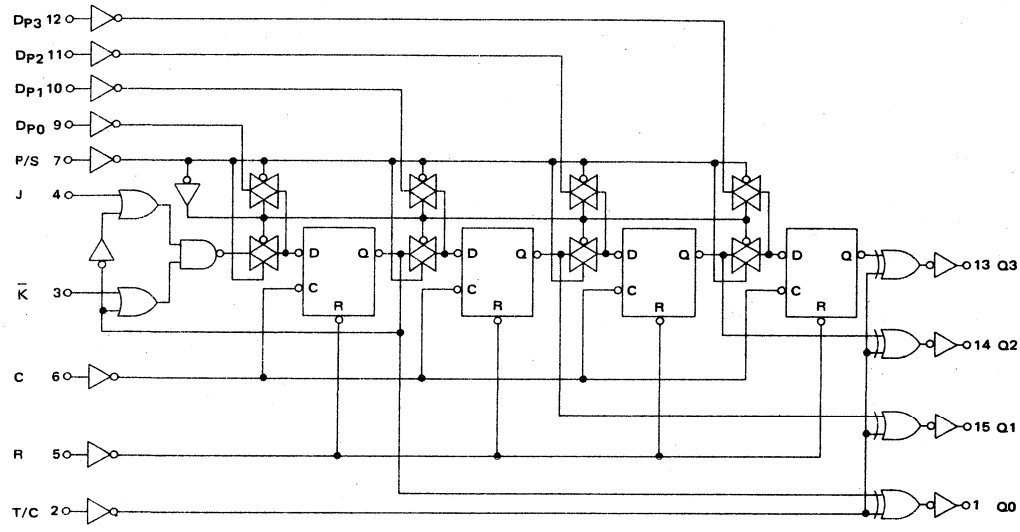
Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 25 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 12 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 8.0 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 47 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 24 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 17 ns		15	–	40	80	
Propagation Delay Time, Clock or Reset to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 223 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 89 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 67 ns		15	–	95	190	
Clock Pulse Width	t_{WH}	5.0	335	135	–	ns
		10	165	45	–	
		15	125	40	–	
Reset Pulse Width	t_{WH}	5.0	400	80	–	ns
		10	175	40	–	
		15	130	35	–	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.2	MHz
		10	–	6.0	2.0	
		15	–	10	3.0	
J-K Setup Time	t_{su}	5.0	500	120	–	ns
		10	200	50	–	
		15	150	30	–	
P/S Control Setup Time	t_{su}	5.0	500	25	–	ns
		10	200	10	–	
		15	150	7.5	–	
Parallel Input Setup Time	t_{su}	5.0	500	90	–	ns
		10	200	20	–	
		15	150	15	–	

* The formula given is for the typical characteristics only.

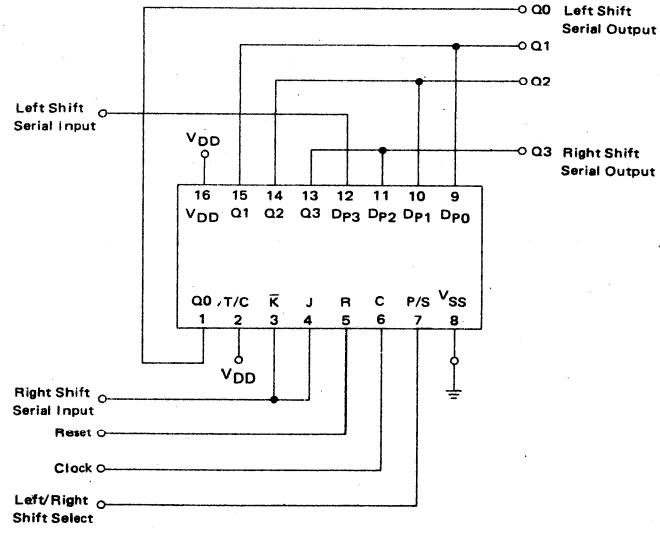
FIGURE 1 – TIMING DIAGRAM



LOGIC DIAGRAM



APPLICATION DIAGRAM
Shift Left/Shift Right Register



MOTOROLA

MC14038B

FOR COMPLETE DATA
SEE MC14032B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

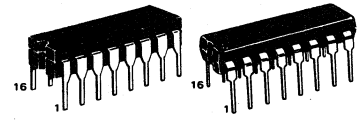
TRIPLE SERIAL ADDERS

Positive Logic – MC14032B
Negative Logic – MC14038B

TRIPLE SERIAL ADDERS

The MC14032B and MC14038B triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032B, and on the negative-going clock transition for the MC14038B. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

- Static Operation from dc to 5.0 MHz
- Buffered Outputs
- Single-Phase Clocking
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4032B and CD4038B.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

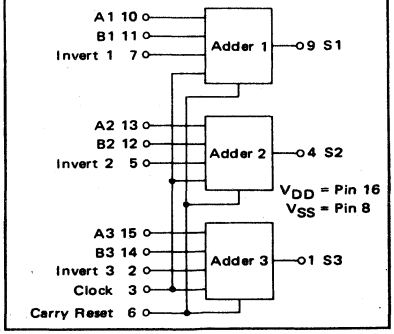
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

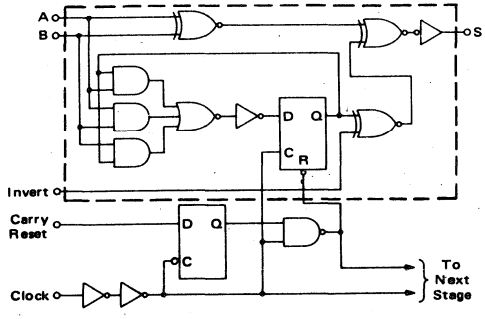
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM

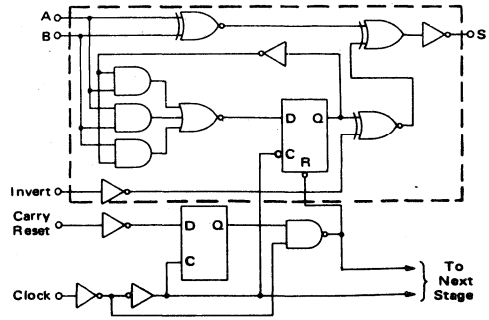


LOGIC DIAGRAMS
(ONE SECTION AND COMMON INPUTS SHOWN)

MC14032B



MC14038B



MOTOROLA

MC14040B

12-BIT BINARY COUNTER

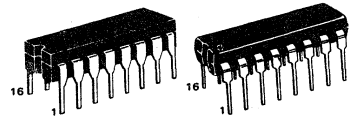
The MC14040B 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Common Reset Line
- 13 MHz Typical Counting Rate @ V_{DD} = 15 V
- Pin-for-Pin Replacement for CD4040B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

12-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

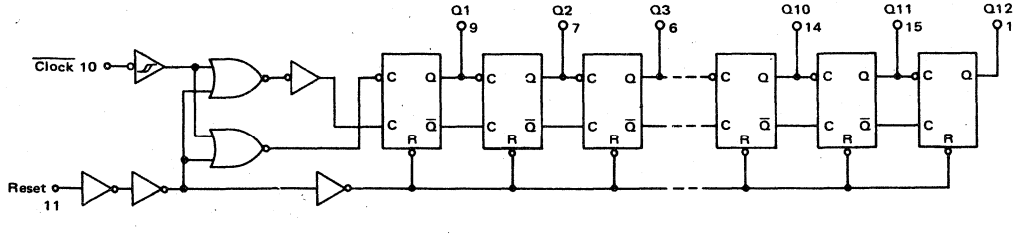
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
↓	0	No Change
↑	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



Q4 = Pin 5 Q7 = Pin 4
Q5 = Pin 3 Q8 = Pin 13
Q6 = Pin 2 Q9 = Pin 12

V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.42 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.85 µA/kHz) f + I_{DD}							
		15	I_T = (1.43 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns		10	–	170	340	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 95 ns		15	–	120	240	
Clock to Q12						ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 2415 ns		5.0	–	2.5	5.0	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 867 ns		10	–	0.9	1.8	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 475 nd		15	–	0.5	1.4	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 485 ns		5.0	–	570	1620	
t_{PHL} = (0.66 ns/pF) C_L + 182 ns		10	–	215	600	
t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	450	
Clock Pulse Width	t_{WH}	5.0	385	140	–	ns
		10	150	55	–	
		15	115	38	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.5	1.5	MHz
		10	–	9.0	3.5	
		15	–	13	4.5	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			ns
		10				
		15				
Reset Pulse Width	t_{WH}	5.0	960	320	–	ns
		10	360	120	–	
		15	270	80	–	

* The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

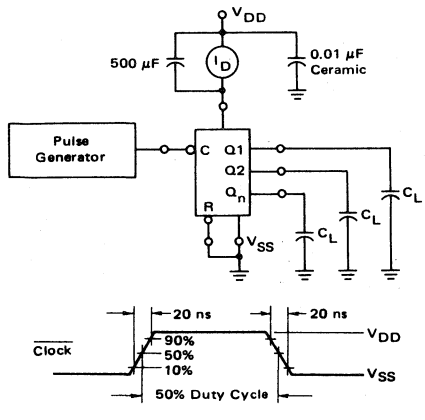


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

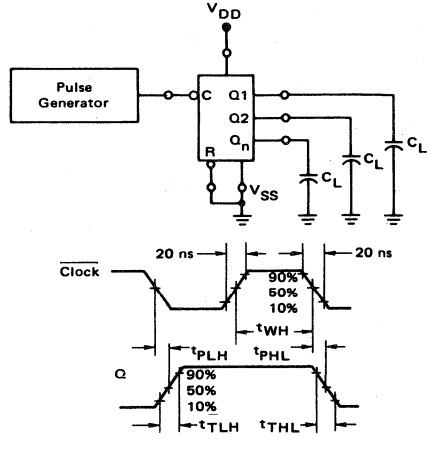
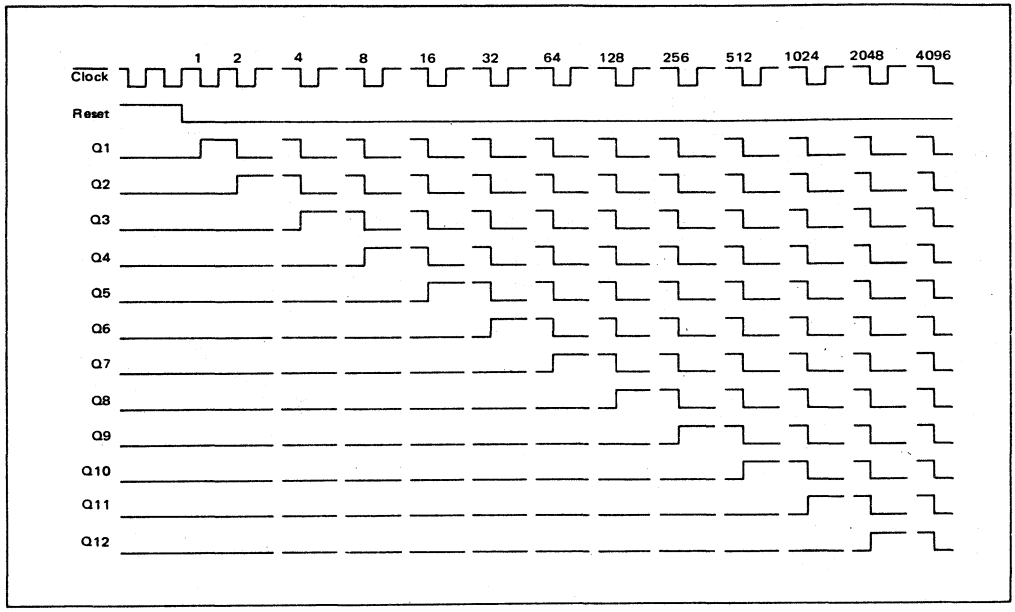


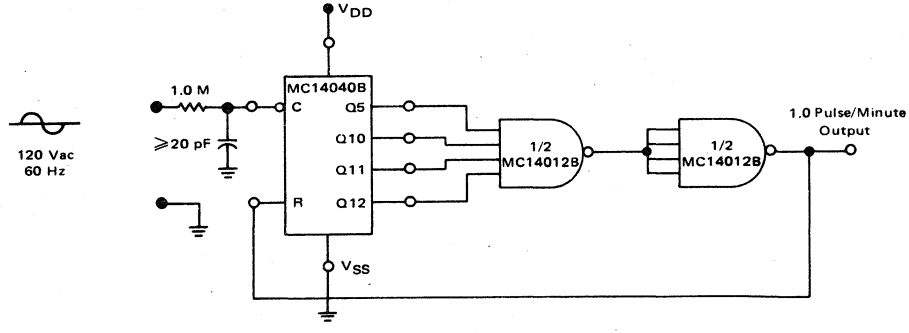
FIGURE 3 – TIMING DIAGRAM



APPLICATIONS INFORMATION

TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14012B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14042B

CMOS SSI

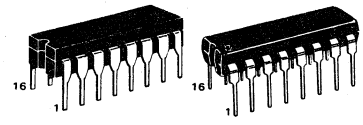
(LOW-POWER COMPLEMENTARY MOS)

QUAD LATCH

QUAD LATCH

The MC14042B quad latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe date through the latches can be reversed using the polarity input. Information present at the data input is transferred to ourputs Q and $\bar{Q}$ during the clock level which is determined by the polarity input. When the polarity input is in the logic "0" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level.

- Buffered Data Inputs
- Common Clock
- Positive or Negative Edge Clocked
- Q and $\bar{Q}$ Outputs
- Double Diode Input Protection
- No Limit on Clock Rise or Fall Times
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

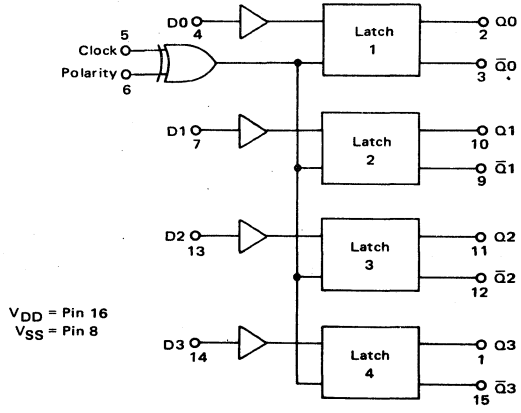
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

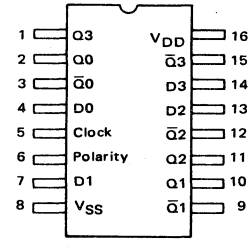
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

PIN ASSIGNMENT



TRUTH TABLE

CLOCK	POLARITY	Q
0	0	Data
⌐	0	Latch
1	1	Data
⌙	1	Latch

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# D Inputs "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Input Voltage C,P Inputs "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.75	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.25	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.0 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.0 µA/kHz) f + I_{DD}							
		15	I_T = (3.0 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time, D to Q, Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Propagation Delay Time, Clock to Q, Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		25	–	60	120	
Clock Pulse Width	t_{WH}					ns
		5.0	300	150	–	
		10	100	50	–	
		15	80	40	–	
Clock Rise Time	t_{TLH}					–
		5.0	No Limit			
		10				
		15				
Hold Time	t_h					ns
		5.0	100	50	–	
		10	50	25	–	
		15	40	20	–	
Setup Time	t_{su}					ns
		5.0	50	0	–	
		10	30	0	–	
		15	25	0	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – AC AND POWER DISSIPATION TEST CIRCUIT AND TIMING DIAGRAM
(Data to Output)

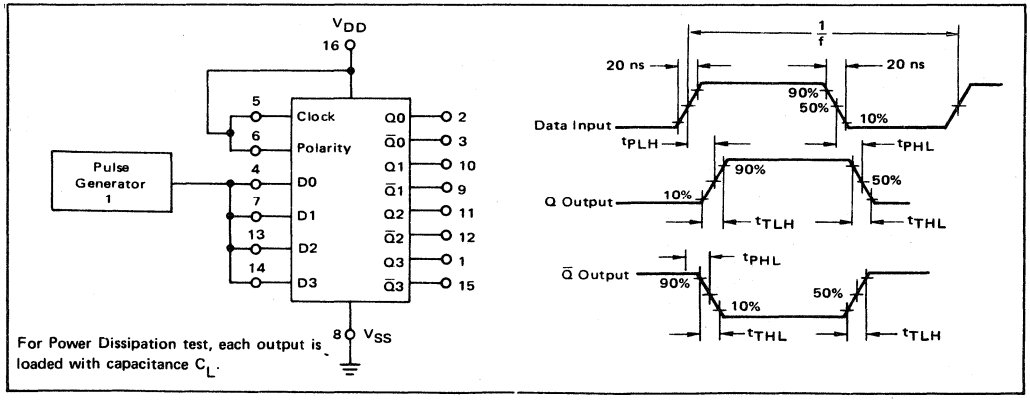
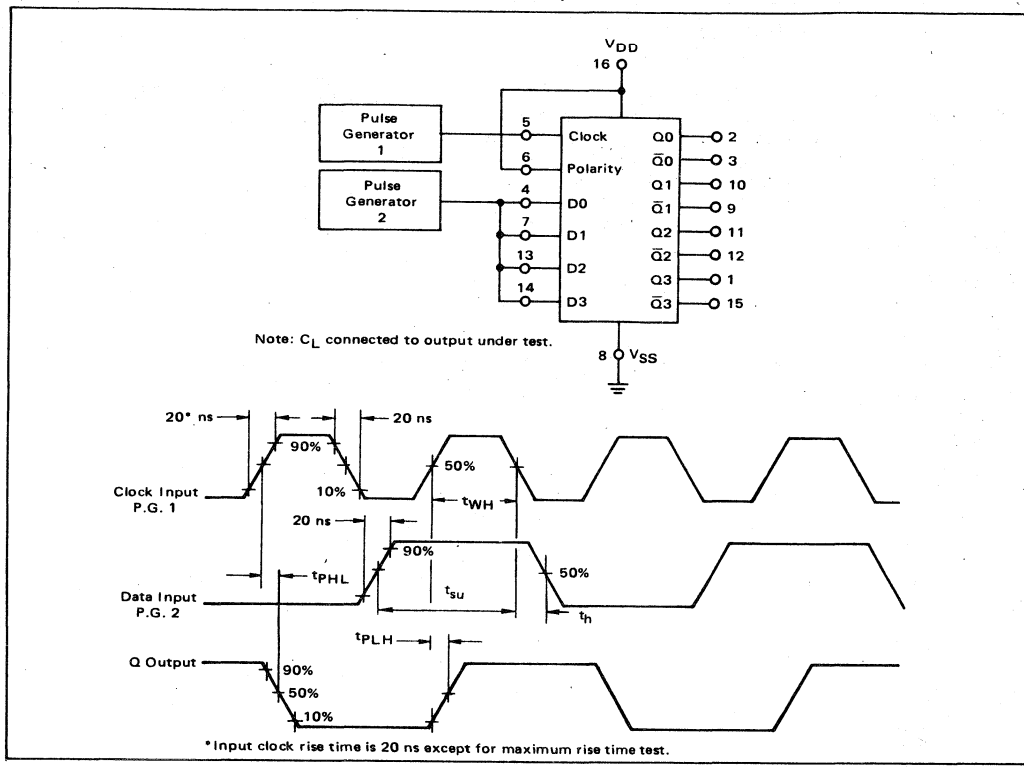


FIGURE 2 – AC TEST CIRCUIT AND TIMING DIAGRAM
(Clock to Output)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

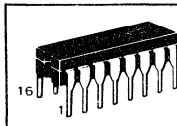
MC14043B
QUAD "NOR" R-S LATCH

MC14044B
QUAD "NAND" R-S LATCH

CMOS MSI
QUAD R-S LATCHES

The MC14043B and MC14044B quad R-S latches are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three-state buffers having a common enable input. The outputs are enabled with a logical "1" or high on the enable input; a logical "0" or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

- Quiescent Current = 4.0 nA/pkg typical @ 10 Vdc
- Double Diode Input Protection
- Three-State Outputs with Common Enable
- Outputs Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load, or Two HTL Loads Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc



L SUFFIX
CERAMIC PACKAGE
CASE 620

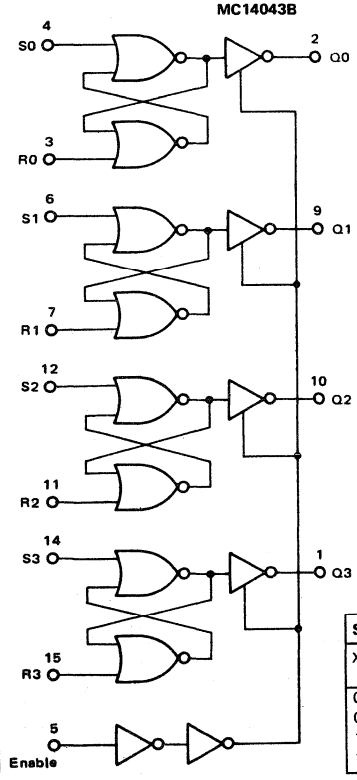


P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MC14043B



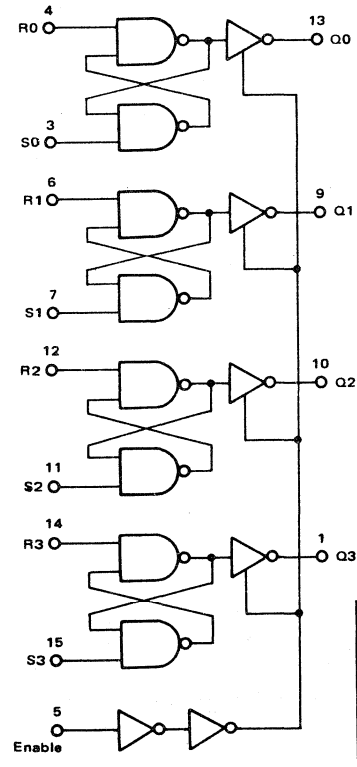
V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	No Change
0	1	1	0
1	0	1	1
1	1	1	1

X = Don't Care

MC14044B



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	No Change

X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all outputs switching)	I_T	5.0	I_T = (0.58 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.15 µA/kHz) f + I_{DD}							
		15	I_T = (1.73 µA/kHz) f + I_{DD}							
Three-State Output Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	µAdc
Three-State Output Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.0001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF.

$$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

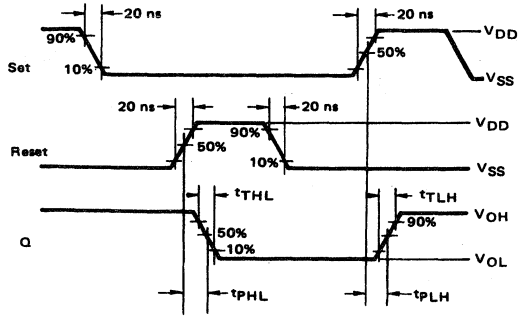
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 32.5 ns		5.0	–	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 32.5 ns		5.0	–	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.90 ns/pF) C_L + 130 ns		5.0	–	175	350	
t_{PLH} = (0.36 ns/pF) C_L + 57 ns		10	–	75	175	
t_{PLH} = (0.26 ns/pF) C_L + 47 ns		15	–	60	120	
t_{PHL} = (0.90 ns/pF) C_L + 130 ns	t_{PHL}	5.0	–	175	350	ns
t_{PHL} = (0.90 ns/pF) C_L + 57 ns		10	–	75	175	
t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	–	60	120	
Set Pulse Width	t_{WH}	5.0	200	80	–	ns
		10	100	40	–	
		15	70	30	–	
Reset Pulse Width	t_{WH}	5.0	200	80	–	ns
		10	100	40	–	
		15	70	30	–	
Three-State Enable/Disable Delay	t_{PLZ}, t_{PHZ}	5.0	–	150	300	ns
		10	–	80	160	
		15	–	55	110	

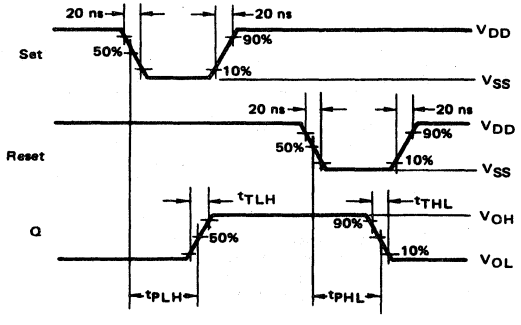
* The formulas given are for the typical characteristics only.

AC WAVEFORMS

MC14043B



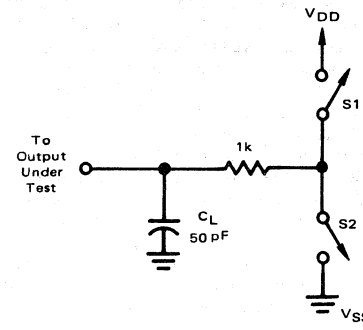
MC14044B

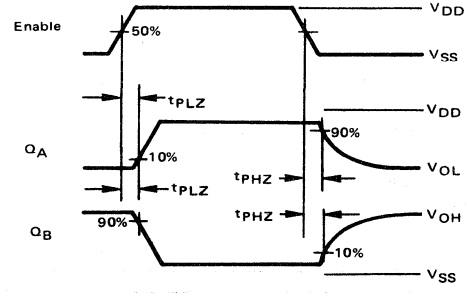


THREE-STATE ENABLE/DISABLE DELAYS

Set, Reset, and Switch Conditions for 3-State Tests.

TEST	S	R	MC14043B S1	MC14043B S2	MC14043B Q	MC14044B S1	MC14044B S2	MC14044B Q
t_{PLZ}	V_{DD}	V_{SS}	Open	Closed	A	Closed	Open	B
t_{PLZ}	V_{SS}	V_{DD}	Closed	Open	B	Open	Closed	A
t_{PHZ}	V_{DD}	V_{SS}	Open	Closed	A	Closed	Open	B
t_{PHZ}	V_{SS}	V_{DD}	Closed	Open	B	Open	Closed	A





MOTOROLA

MC14046B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

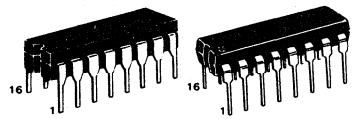
PHASE-LOCKED LOOP

PHASE-LOCKED LOOP

The MC14046B phase-locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs. PCA_{in} and PCB_{in}. Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{out}$, and maintains 90° phase shift at the center frequency between PCA_{in} and PCB_{in} signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals $PC2_{out}$ and PCP_{out}, and maintains a 0° phase shift between PCA_{in} and PCB_{in} signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins $C1_A$, $C1_B$, R1, and R2. The source-follower output SF_{out} with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

- VCO Frequency = 1.4 MHz Typical @ V_{DD} = 10 Vdc
- VCO Frequency Drift with Temperature = 0.04%/°C Typical @ V_{DD} = 10 Vdc
- VCO Linearity = 1% Typical
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Dynamic Power Dissipation — 70 μW Typical @ f_0 = 10 kHz, V_{DD} = 5.0 Vdc, R1 = 1.0 MΩ, R2 = ∞, R_{SF} = ∞
- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 Vdc
- Pin-for-Pin Replacement for CD4046B



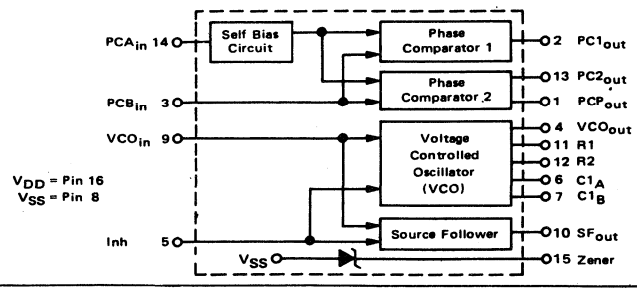
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Pins 6, 7, 10, 11, 12, and 15 if unused must be left open.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
(Inh = "1" and PCA = "1")		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
(Inh = "1" and PCA = "1")		15	–	80	–	0.015	80	–	600	
Total Supply Current † (Inh = "0", f_o = 10 kHz, C_L = 50 pF, R1 = 1 MΩ, R2 = ∞, R_{SF} = ∞, and 50% Duty Cycle)	I_T	5.0	I_T = (1.46 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.91 µA/kHz) f + I_{DD}							
		15	I_T = (4.37 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To Calculate Total Current in General:

$$I_T \approx 2.2 \times V_{DD}\left(\frac{VCO_{in} - 1.65}{R1} + \frac{V_{DD} - 1.35}{R2}\right)^{3/4} + 1.6 \times \left(\frac{VCO_{in} - 1.65}{R_{SF}}\right)^{3/4} + 1 \times 10^{-3}(C_L + 9)\, V_{DD}\, f +$$
$$1 \times 10^{-1}\, V_{DD}^2 \left(\frac{100 - \%\ \text{Duty Cycle of PCA}_{in}}{100}\right) + I_Q$$

where: I_T in µA, C_L in pF, VCO_{in}, V_{DD} in Vdc, f in KHz, and R1, R2, R_{SF} in MΩ, C_L on VCO_{out}.

ELECTRICAL CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

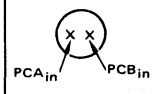
Characteristic	Symbol	V_{DD} Vdc	Minimum AL Device	Minimum CL/CP Device	Typical All Types	Maximum AL Device	Maximum CL/CP Device	Units
Output Rise Time	t_{TLH}							ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_{THL}							ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
PHASE COMPARATORS 1 and 2								
Input Resistance – PCA_{in}	R_{in}	5.0	1.0	1.0	2.0	–	–	MΩ
		10	0.2	0.2	0.4	–	–	
		15	0.1	0.1	0.2	–	–	
– PCB_{in}	R_{in}	15	150	15	1500	–	–	MΩ
Minimum Input Sensitivity	V_{in}	5.0	–	–	200	300	400	mV p-p
AC Coupled – PCA_{in}		10	–	–	400	600	800	
C series = 1000 pF, f = 50 kHz		15	–	–	700	1050	1400	
DC Coupled – PCA_{in}, PCB_{in}	–	5 to 15	See Noise Immunity					
VOLTAGE CONTROLLED OSCILLATOR (VCO)								
Maximum Frequency	f_{max}	5.0	0.50	0.35	0.70	–	–	MHz
(VCO_{in} = V_{DD}, C1 = 50 pF,		10	1.0	0.7	1.4	–	–	
R1 = 5 kΩ, and R2 = ∞)		15	1.4	1.0	1.9	–	–	
Temperature – Frequency Stability	–	5.0	–	–	0.12	–	–	%/°C
(R2 = ∞)		10	–	–	0.04	–	–	
		15	–	–	0.015	–	–	
Linearity (R2 = ∞)	–							%
(VCO_{in} = 2.50 V ± 0.30 V, R1 ≥ 10 kΩ)		5.0	–	–	1	–	–	
(VCO_{in} = 5.00 V ± 2.50 V, R1 ≥ 400 kΩ)		10	–	–	1	–	–	
(VCO_{in} = 7.50 V ± 5.00 V, R1 ≥ 1000 kΩ)		15	–	–	1	–	–	
Output Duty Cycle	–	5 to 15	–	–	50	–	–	%
Input Resistance – VCO_{in}	R_{in}	15	150	15	1500	–	–	MΩ
SOURCE-FOLLOWER								
Offset Voltage	–	5.0	–	–	1.65	2.2	2.5	Vdc
(VCO_{in} minus SF_{out}, R_{SF} > 50 kΩ)		10	–	–	1.65	2.2	2.5	
		15	–	–	1.65	2.2	2.5	
Linearity	–							%
(VCO_{in} = 2.50 V ± 0.30 V, R_{SF} > 50 kΩ)		5.0	–	–	0.1	–	–	
(VCO_{in} = 5.00 V ± 2.50 V, R_{SF} > 50 kΩ)		10	–	–	0.6	–	–	
(VCO_{in} = 7.50 V ± 5.00 V, R_{SF} > 50 kΩ)		15	–	–	0.8	–	–	
ZENER DIODE								
Zener Voltage (I_Z = 50 μA)	V_Z	–	6.7	6.3	7.0	7.3	7.7	Vdc
Dynamic Resistance (I_Z = 1 mA)	R_Z	–	–	–	100	–	–	Ω

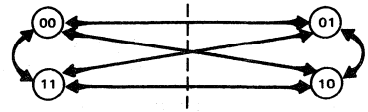
*The formula given is for the typical characteristics only.

FIGURE 1 – PHASE COMPARATORS STATE DIAGRAMS

PHASE COMPARATOR 1

Input State

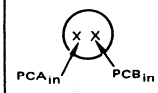


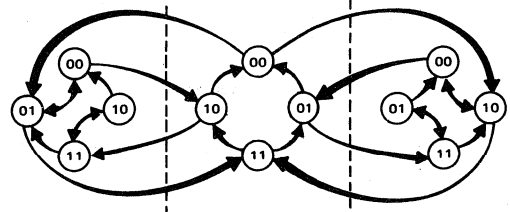


PC1$_{out}$	0	1

PHASE COMPARATOR 2

Input State





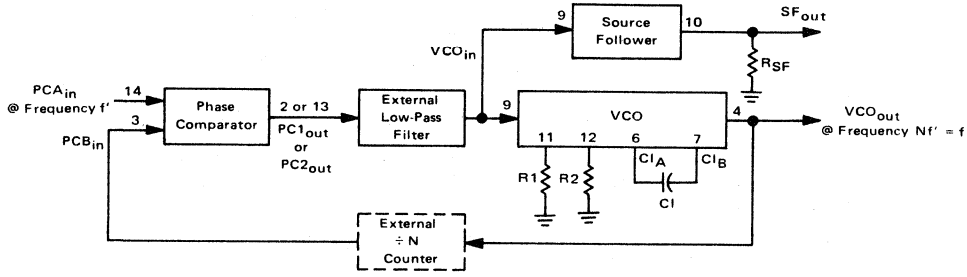
PC2$_{out}$	0	3-State Output Disconnected	1
PCP$_{out}$ (Lock Indicator)	0	1	0

Refer to Waveforms in Figure 3.

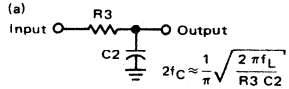
FIGURE 2 – DESIGN INFORMATION

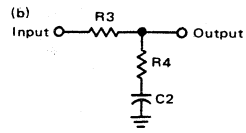
Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA$_{in}$.	VCO in PLL system adjusts to center frequency (f_0).	VCO in PLL system adjusts to minimum frequency (f_{min}).
Phase angle between PCA$_{in}$ and PCB$_{in}$.	90° at center frequency (f_0), approaching 0° and 180° at ends of lock range ($2f_L$).	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range ($2f_L$).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock. $2f_L$ = full VCO frequency range = $f_{max} - f_{min}$.	
Capture frequency range ($2f_C$).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (see Figure 3). $f_C \leq f_L$	$f_C = f_L$
Center frequency (f_0).	The frequency of VCO$_{out}$, when VCO$_{in}$ = 1/2 V_{DD}	
VCO output frequency (f). Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is less than ±20%.	$f_{min} = \frac{1}{R_2(C_1 + 32\ pF)}$ (V_{CO} input = V_{SS}) $f_{max} = \frac{1}{R_1(C_1 + 32\ pF)} + f_{min}$ (V_{CO} input = V_{DD}) Where: $10K \leq R_1 \leq 1M$ $10K \leq R_2 \leq 1M$ $100pF \leq C_1 \leq .01\ \mu F$	

FIGURE 3 – GENERAL PHASE-LOCKED LOOP CONNECTIONS AND WAVEFORMS



Typical Low-Pass Filters





Typically:

$$R_4\ C_2 = \frac{6N}{f_{max}} - \frac{N}{2\pi\Delta f}$$

$$(R_3 + 3{,}000\Omega)\ C_2 = \frac{100N\Delta F}{f_{max}^2} - R_4\ C_2$$

$$\Delta f = f_{max} - f_{min}$$

Note: for further information, see:

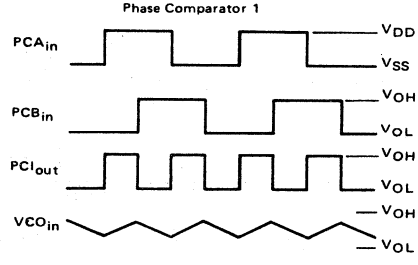
(1) F. Gardner, "Phase-Lock Techniques", John Wiley and Son, New York, 1966.

(2) G. S. Moschytz, "Miniature RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

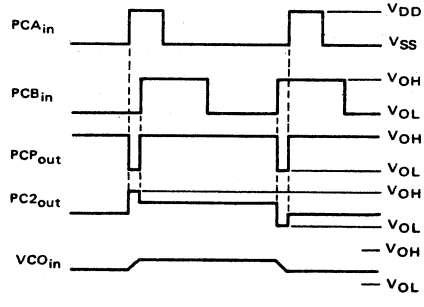
(3) Garth Nash, "Phase-Lock Loop Design Fundamentals", AN-535, Motorola Inc.

Waveforms

Phase Comparator 1



Phase Comparator 2



MOTOROLA

MC14049UB
MC14050B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

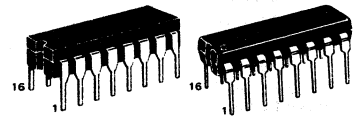
HEX BUFFERS

Inverting – MC14049UB
Noninverting – MC14050B

HEX BUFFERS

The MC14049UB hex inverter/buffer and MC14050B noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{CC}. The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage for logic-level conversions. Two TTL/DTL Loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (V_{CC} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA). Note that pin 16 is not connected internally on these devices; consequently connections to this terminal will not affect circuit operation.

- High Source and Sink Currents
- High-to-Low Level Converter
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Meets JEDEC UB Specifications–MC14049UB
  Meets JEDEC B Specification–MC14050B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

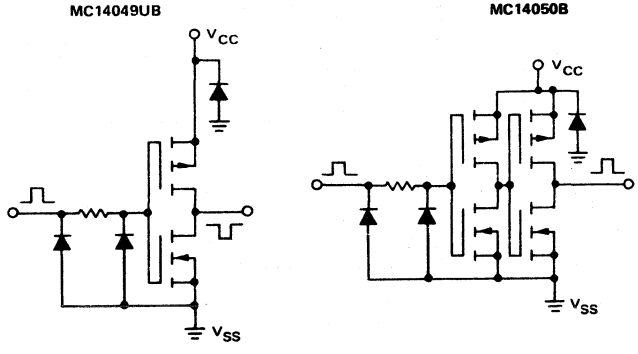
MC14XXXUB
MC14XXXB

Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

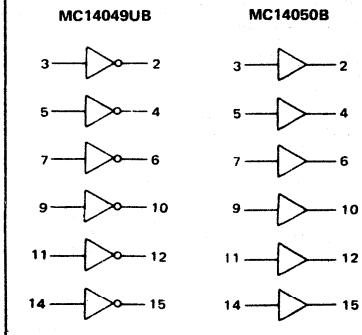
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to +18	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	45	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAMS



NC = Pin 13, 16
V_{SS} = Pin 8
V_{CC} = Pin 1

NC = Pin 13, 16
V_{SS} = Pin 8
V_{CC} = Pin 1

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage #MC14049UB	"0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)			5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)			10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)			15	–	2.5	–	6.75	2.5	–	2.5	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 Vdc)			5.0	4.0	–	4.0	2.75	–	4.0	–	
(V_O = 1.0 Vdc)			10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 Vdc)			15	12.5	–	12.5	8.25	–	12.5	–	
Input Voltage #MC14050B	"0" Level	V_{IL}									Vdc
(V_O = 0.5 Vdc)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 1.0 Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 1.5 Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									Vdc
(V_O = 4.5 Vdc)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 9.0 Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 13.5 Vdc)			15	11	–	11	8.25	–	11	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-1.6	–	-1.25	-2.5	–	-0.9	–	
(V_{OH} = 9.5 Vdc)			10	-1.6	–	-1.3	-2.5	–	-0.9	–	
(V_{OH} = 13.5 Vdc)			15	-4.7	–	-3.75	-10	–	-2.7	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	3.75	–	3.2	6.0	–	2.2	–	mAdc
(V_{OL} = 0.5 Vdc)			10	10	–	8.0	16	–	5.6	–	
(V_{OL} = 1.5 Vdc)			15	30	–	24	40	–	17.0	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-1.5	–	-1.25	-2.5	–	-1.0	–	
(V_{OH} = 9.5 Vdc)			10	-1.5	–	-1.25	-2.5	–	-1.0	–	
(V_{OH} = 13.5 Vdc)			15	-4.5	–	-3.75	-10	–	-3.0	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	3.6	–	3.2	6.0	–	2.6	–	mAdc
(V_{OL} = 0.5 Vdc)			10	9.6	–	8.0	16	–	6.6	–	
(V_{OL} = 1.5 Vdc)			15	28	–	24	40	–	19	–	
Input Current (AL Device)		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)		I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	10	20	–	–	pF
Quiescent Current (AL Device)		I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
(Per Package)			10	–	2.0	–	0.004	2.0	–	60	
			15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)		I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
(Per Package)			10	–	8.0	–	0.004	8.0	–	60	
			15	–	16	–	0.006	16	–	120	
Total Supply Current**†		I_T	5.0	$I_T = (1.8\ \mu A/kHz)f + I_{DD}$							μAdc
(Dynamic plus Quiescent, Per Package)			10	$I_T = (3.5\ \mu A/kHz)f + I_{DD}$							
(C_L 50 pF on all outputs, all buffers switching)			15	$I_T = (5.3\ \mu A/kHz)f + I_{DD}$							

*T_{low} = 55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

†To Calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3}(C_L - 50)\ V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

#Noise immunity specified for worst-case input combination
B Suffix Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
UB Suffix Noise Margin for both "1" and "0" level =
0.5 Vdc min @ V_{DD} = 5.0 Vdc
1.0 Vdc min @ V_{DD} = 10 Vdc
1.0 Vdc min @ V_{DD} = 15 Vdc

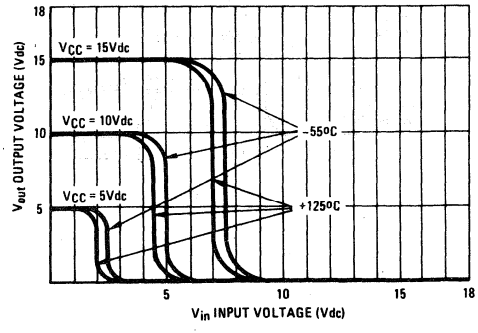
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
MC14049UB						
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.8 ns/pF) C_L + 60 ns		5.0	–	100	160	
t_{TLH} = (0.3 ns/pF) C_L + 35 ns		10	–	50	100	
t_{TLH} = (0.27 ns/pF) C_L + 26.5 ns		15	–	40	60	
Output Fall Time	t_{THL}					ns
t_{THL} = (0.3 ns/pF) C_L + 25 ns		5.0	–	40	60	
t_{THL} = (0.12 ns/pF) C_L + 14 ns		10	–	20	40	
t_{THL} = (0.1 ns/pF) C_L + 10 ns		15	–	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.38 ns/pF) C_L + 61 ns		5.0	–	80	120	
t_{PLH} = (0.20 ns/pF) C_L + 30 ns		10	–	40	65	
t_{PLH} = (0.11 ns/pF) C_L + 24.5 ns		15	–	30	50	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.38 ns/pF) C_L + 11 ns		5.0	–	30	60	
t_{PHL} = (0.12 ns/pF) C_L + 9 ns		10	–	15	30	
t_{PHL} = (0.11 ns/pF) C_L + 4.5 ns		15	–	10	20	
MC14050B						
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.7 ns/pF) C_L + 65 ns		5.0	–	100	160	
t_{TLH} = (0.25 ns/pF) C_L + 37.5 ns		10	–	50	80	
t_{TLH} = (0.2 ns/pF) C_L + 30 ns		15	–	40	60	
Output Fall Time	t_{THL}					ns
t_{THL} = (0.2 ns/pF) C_L + 30 ns		5.0	–	40	60	
t_{THL} = (0.06 ns/pF) C_L +17 ns		10	–	20	40	
t_{THL} = (0.04 ns/pF) C_L + 13 ns		15	–	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.33 ns/pF) C_L + 63.5 ns		5.0	–	80	140	
t_{PLH} = (0.19 ns/pF) C_L + 30.5 ns		10	–	40	80	
t_{PLH} = (0.06 ns/pF) C_L + 27 ns		15	–	30	60	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.2 ns/pF) C_L + 30 ns		5.0	–	40	80	
t_{PHL} = (0.1 ns/pF) C_L + 15 ns		10	–	20	40	
t_{PHL} = (0.05 ns/pF) C_L + 12.5 ns		15	–	15	30	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

MC14049UB



MC14050B

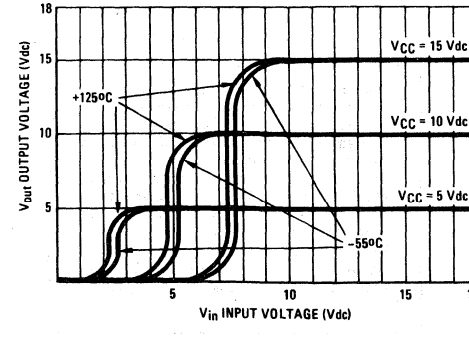


FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

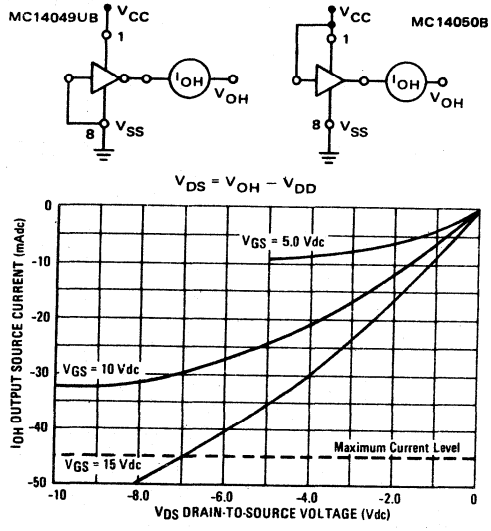


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS

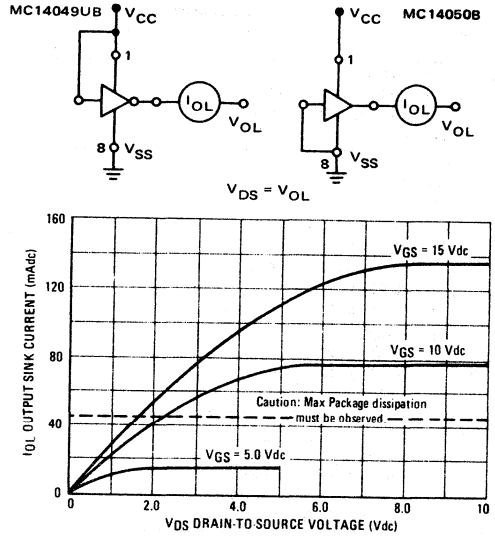
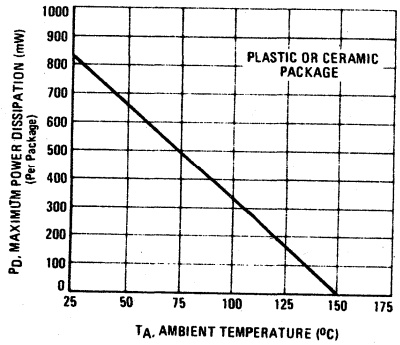


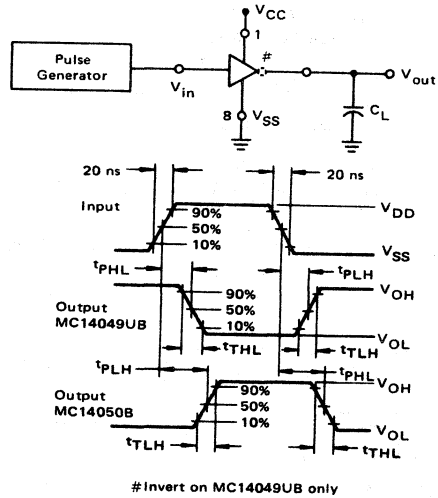
FIGURE 4 – AMBIENT TEMPERATURE POWER DERATING



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



#Invert on MC14049UB only

MOTOROLA

MC14051B
MC14052B
MC14053B

ANALOG MULTIPLEXERS/DEMULTIPLEXERS

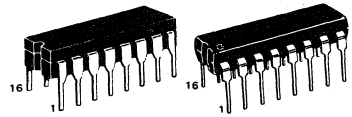
The MC14051B, MC14052B, and MC14053B, analog multiplexers are digitally controlled analog switches. The MC14051B effectively implements an 8PST electronic switch, the MC14052B a 4PDT or 2P4T, and the MC14053B a DP3T or 3P2T. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- High On/Off Output Voltage Ratio – 65 dB typical
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches – 80 dB typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 65 MHz
- Linearized Transfer Characteristics, $\triangle R_{ON} < 60\ \Omega$ for $V_{in} = V_{DD}$ to V_{EE} @ 15 Vdc
- Low Noise – 12 $nV/\sqrt{Cycle}$, $f \geq 1$ kHz typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/ DEMULTIPLEXERS



CASE 620
L SUFFIX
CERAMIC PACKAGE

CASE 648
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION

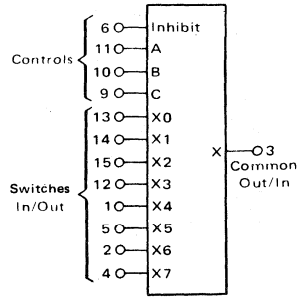
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{EE}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
Through Current	I	25	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

MC14051B

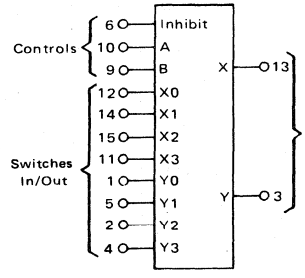
8-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

MC14052B

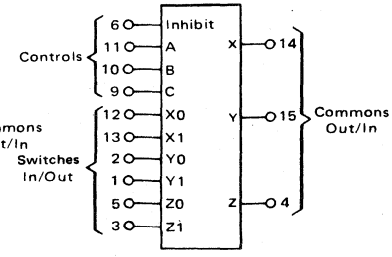
Dual 4-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

MC14053B

Triple 2-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

Note: Control Inputs referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be $\leq V_{SS}$.

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD}-V_{EE} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or V_{SS}			10	–	0.05	–	0	0.05	–	0.05	
V_{SS} = V_{EE}			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage#	"0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	11.25	–	11.0	8.25	–	11.0	–	
Input Current (Control, Inhibit)		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance		C_{in}									pF
(V_{in} = 0)											
Control, Inhibit			–	–	–	–	5.0	–	–	–	
Switch Inputs			–	–	–	–	10	–	–	–	
Output Capacitance	MC14051B	C_{out}	10	–	–	–	60	–	–	–	pF
	MC14052B		10	–	–	–	32	–	–	–	
	MC14053B		10	–	–	–	17	–	–	–	
Feedthrough Capacitance	MC14051B	C_{in-out}	10	–	–	–	0.18	–	–	–	pF
	MC14052B		10	–	–	–	0.12	–	–	–	
	MC14053B		10	–	–	–	0.10	–	–	–	
Quiescent Current (AL Device)		I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)			10	–	10	–	0.010	10	–	300	
			15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)		I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)			10	–	40	–	0.010	40	–	300	
			15	–	80	–	0.015	80	–	600	
Total Supply Current**†		I_T	5.0	I_T = (0.07 μA/kHz) f + I_Q							μAdc
(Dynamic plus Quiescent,			10	I_T = (0.20 μA/kHz) f + I_Q							
Per Package)			15	I_T = (0.36 μA/kHz) f + I_Q							
ON Resistance (AL Device)		R_{ON}	5.0	–	880	–	250	1050	–	1200	Ω
			10	–	400	–	120	500	–	550	
			15	–	220	–	80	280	–	320	
ON Resistance (CL/CP Device)		R_{ON}	5.0	–	880	–	250	1050	–	1200	Ω
			10	–	450	–	120	500	–	520	
			15	–	250	–	80	280	–	300	
Δ ON Resistance Between Any		ΔR_{ON}	5.0	–	–	–	25	–	–	–	Ω
Two Channels			10	–	–	–	10	–	–	–	
			15	–	–	–	5.0	–	–	–	
OFF Channel Leakage Current		–									nAdc
Any Channel			15	–	100	–	±0.01	100	–	1000	
(AL Device) All Channels OFF:											
	MC14051B		15	–	100	–	±0.08	100	–	1000	
	MC14052B		15	–	100	–	±0.04	100	–	1000	
	MC14053B		15	–	100	–	±0.02	100	–	1000	
OFF Channel Leakage Current		–									nAdc
Any Channel			15	–	1000	–	±0.01	1000	–	3000	
(CL/CP Device)											
All Channels OFF:	MC10451B		15	–	1000	–	±0.08	1000	–	3000	
	MC10452B		15	–	1000	–	±0.04	1000	–	3000	
	MC10453B		15	–	1000	–	±0.02	1000	–	3000	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity is defined as the control input voltage coincident with the specified change, ΔV_{out}, at an output in the OFF state.
**The formulas given are for the typical characteristics only at 25°C.
†Total Supply Current, I_T, is the current drawn at device terminals V_{DD} and V_{SS} for total current through the device. The channel component, $(V_{in}-V_{out})/R_{ON}$, should not be included.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}-V_{EE} Vdc	Typ All Types	Max	Unit
Propagation Delay Times	t_{PLH}, t_{PHL}				ns
Switch Input to Switch Output (R_L = 10 kΩ)					
MC14051					
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns		5.0	35	90	
t_{PLH}, t_{PHL} - (0.08 ns/pF) C_L + 11 ns		10	15	40	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns		15	12	30	
MC14052					
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 21.5 ns		5.0	30	75	ns
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 8.0 ns		10	12	30	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 7.0 ns		15	10	25	
MC14053					
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 16.5 ns		5.0	25	65	ns
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 4.0 ns		10	8.0	20	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 3.0 ns		15	6.0	15	
Inhibit to Output (R_L = 10 kΩ):	t_{PHZ}, t_{PLZ},				ns
Output "1" or "0" to High Impedance, or	t_{PZH}, t_{PZL}				
High Impedance to "1" or "0" Level					
MC14051B		5.0	350	700	
		10	170	340	
		15	140	280	
MC14052B		5.0	300	600	ns
		10	155	310	
		15	125	250	
MC14053B		5.0	275	550	ns
		10	140	280	
		15	110	220	
Control Input to Output (R_L = 10 kΩ)	t_{PLH}, t_{PHL}				ns
MC14051B		5.0	360	720	
		10	160	320	
		15	120	240	
MC14052B		5.0	325	650	ns
		10	130	260	
		15	90	180	
MC14053B		5.0	300	600	ns
		10	120	240	
		15	80	160	
Sine Wave Distortion (R_L = 1 kΩ, f = 1 kHz)	–	10	0.04	–	%
Bandwidth	BW				MHz
(R_L = 1 kΩ, V_{in} = 1/2 (V_{DD} - V_{SS}) p-p,					
20 Log 10 $\frac{V_{Out}}{V_{in}$ = -3 dB) MC14051B		10	20	–	
MC14052B		10	30	–	
MC14053B		10	55	–	
Feedthrough Attenuation, Input to Output	–				MHz
(R_L = 1 kΩ, 20 Log 10 $\frac{V_{out}}{V_{in}$ = -50 dB) MC14051B		10	4.5	–	
MC14052B		10	30	–	
MC14053B		10	55	–	
Channel Separation	–	10	3.0	–	MHz
(R_L = 1 kΩ, V_{in} = 1/2 (V_{DD} - V_{SS}) p-p,					
20 Log 10 $\frac{V_{out(B)}}{V_{in(A)}$ = -50 dB)					
Feedthrough Control, Input to Output	–	10	30	–	mV
(R_1 = 1 kΩ, R_L = 10 kΩ Control/Inhibit					
t_{TLH} = t_{THL} = 20 ns)					
Maximum Control Frequency	–	10	10	–	MHz
(R_L = 1 kΩ, V_{out} = 1/2 V_{in})					

* The formulas given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC

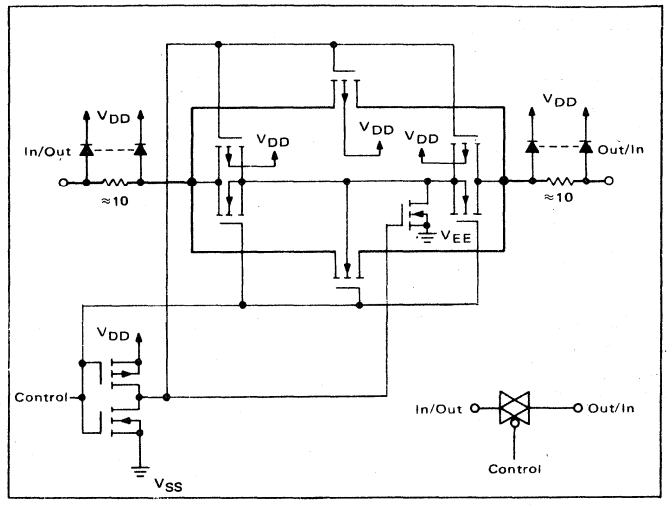
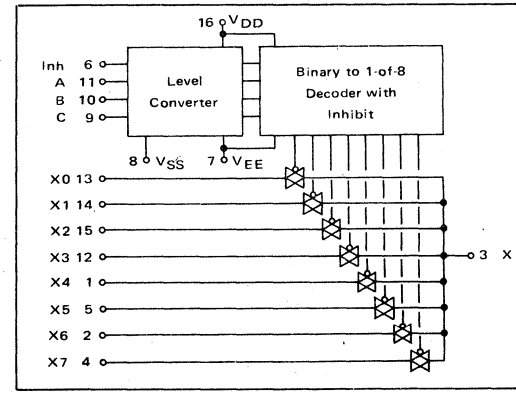


FIGURE 2 – MC14051B FUNCTIONAL DIAGRAM



TRUTH TABLE

Control Inputs				ON Switches					
	Select								
Inhibit	C*	B	A	MC14051B	MC14052B		MC14053B		
0	0	0	0	X0	Y0	X0	Z0	Y0	X0
0	0	0	1	X1	Y1	X1	Z0	Y0	X1
0	0	1	0	X2	Y2	X2	Z0	Y1	X0
0	0	1	1	X3	Y3	X3	Z0	Y1	X1
0	1	0	0	X4			Z1	Y0	X0
0	1	0	1	X5			Z1	Y0	X1
0	1	1	0	X6			Z1	Y1	X0
0	1	1	1	X7			Z1	Y1	X1
1	x	x	x	None	None		None		

*Not applicable for MC14052
x = Don't Care

FIGURE 3 – MC14052B FUNCTIONAL DIAGRAM

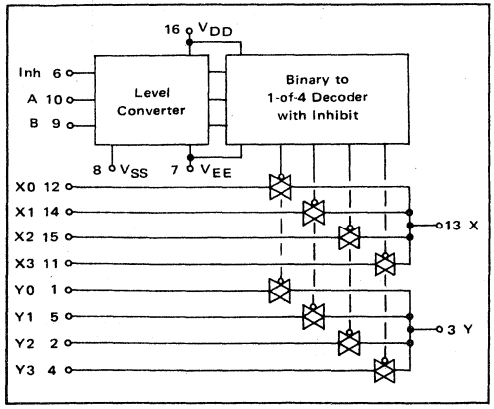
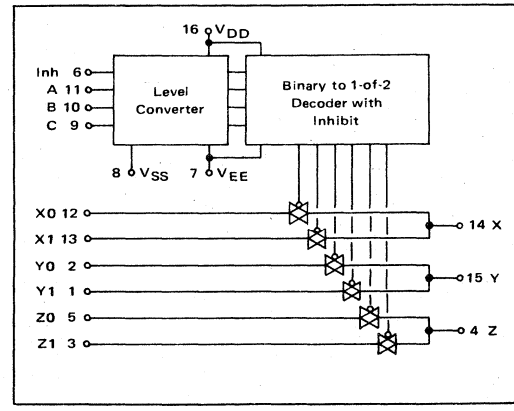


FIGURE 4 – MC14053B FUNCTIONAL DIAGRAM



TEST CIRCUITS

FIGURE 5 – INPUT VOLTAGE

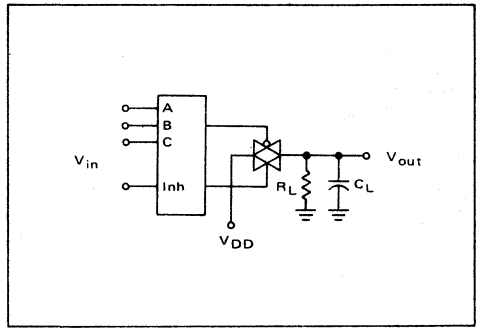


FIGURE 6 – PROPAGATION DELAY TIMES, CONTROL AND INHIBIT TO OUTPUT

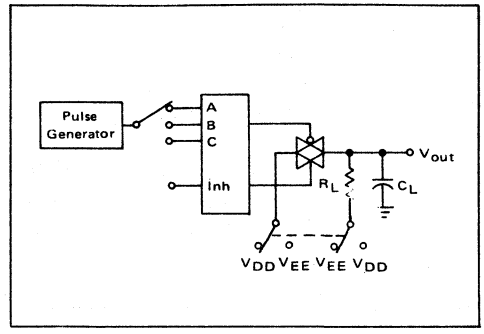


FIGURE 7 – BANDWIDTH AND FEEDTHROUGH ATTENUATION

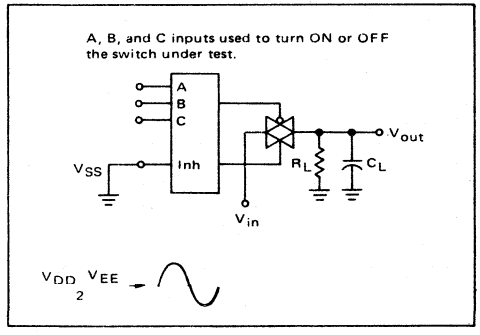


FIGURE 8 – CROSSTALK BETWEEN ANY TWO SWITCHES

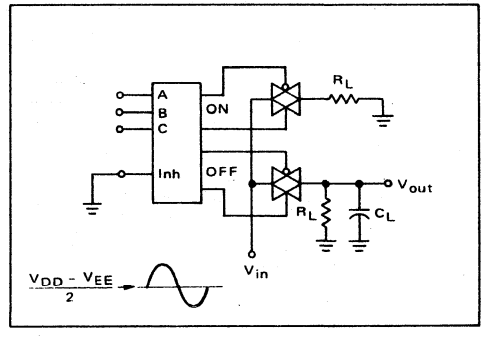


FIGURE 9 – FEEDTHROUGH, CONTROL TO SIGNAL OUTPUT

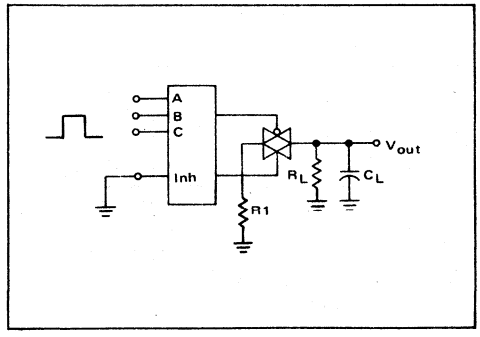


FIGURE 10 – MAXIMUM CONTROL FREQUENCY

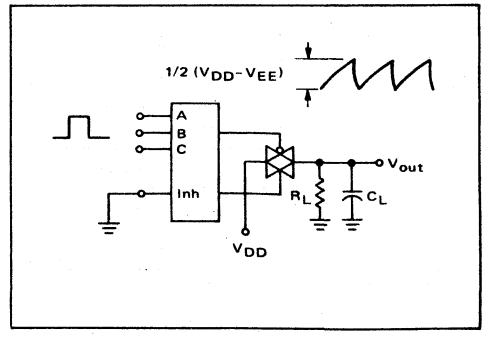
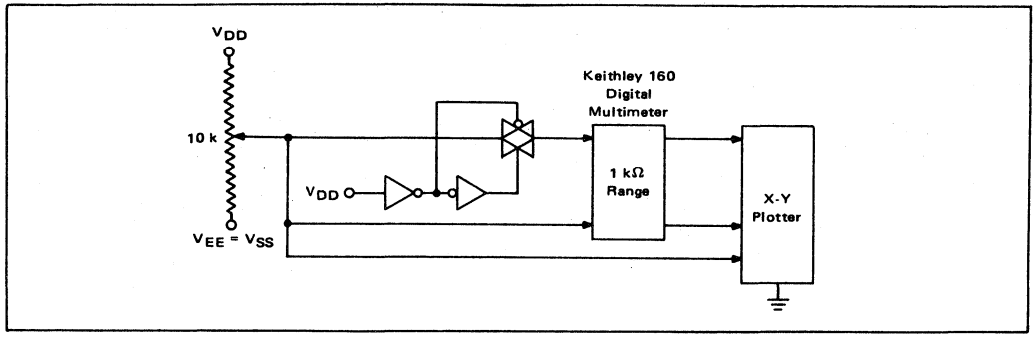


FIGURE 11 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 12 – V_{DD} = 7.5 V, V_{EE} = -7.5 V

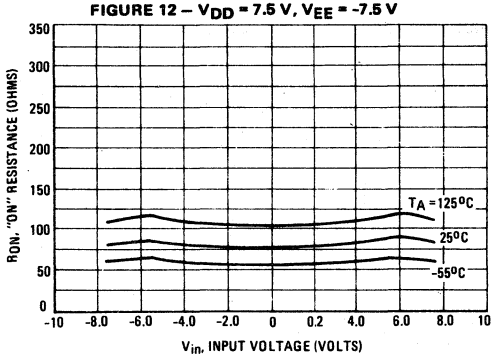


FIGURE 13 – V_{DD} = 5.0 V, V_{EE} = -5.0 V

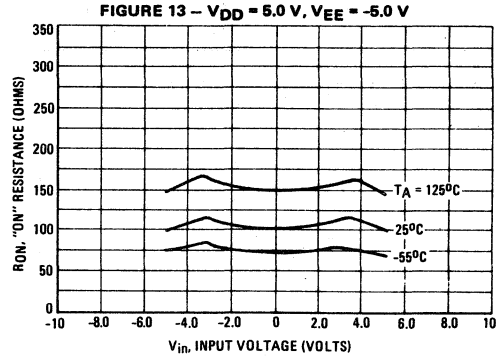


FIGURE 14 – V_{DD} = 2.5 V, V_{EE} = -2.5 V

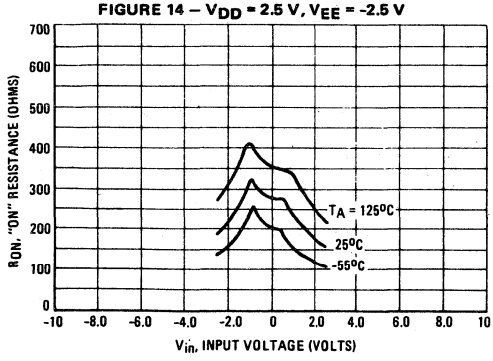
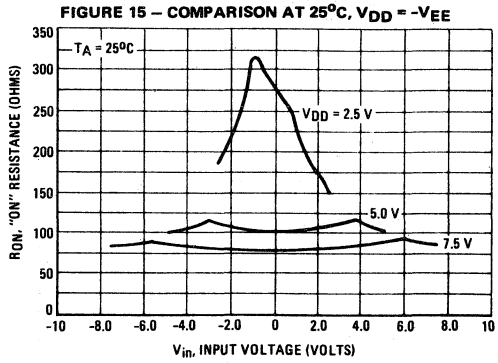


FIGURE 15 – COMPARISON AT 25°C, V_{DD} = -V_{EE}



MOTOROLA

MC14066B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

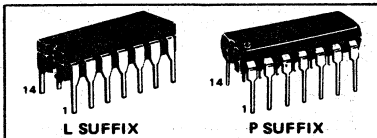
QUAD ANALOG SWITCH QUAD MULTIPLEXER

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- High On/Off Output Voltage Ratio — 65 dB typical
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches —50 dB typical @ 8 MHz
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 65 MHz @ 10 Vdc
- Linearized Transfer Characteristics, $\Delta R_{ON} < 60\ \Omega$ for $V_{in} = V_{DD}$ to V_{SS} (at 15V)
- Low Noise — 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4016, CD4066, MC14016



L SUFFIX
CERAMIC PACKAGE
CASE 632

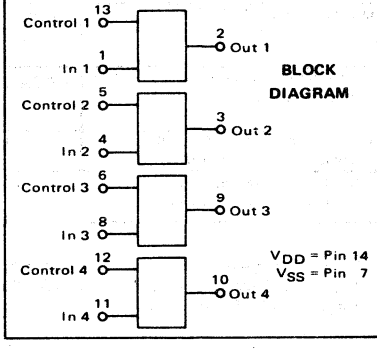
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

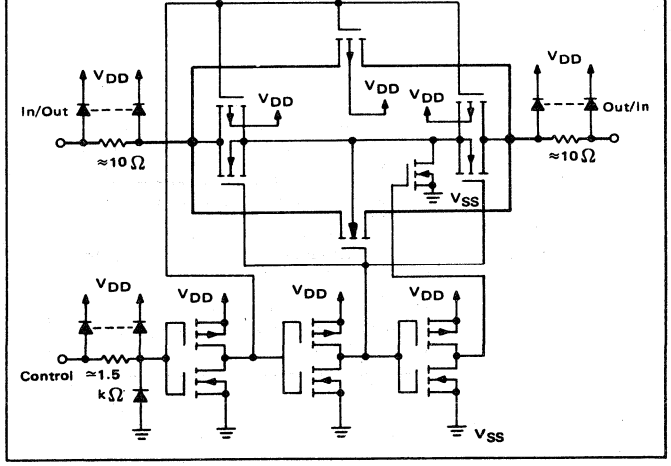
MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

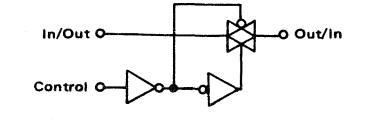
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
Through Current	I	25	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)



LOGIC DIAGRAM AND TRUTH TABLE
(1/4 OF DEVICE SHOWN)



Control	Switch
0	OFF
1	ON

Logic Diagram Restrictions
$V_{SS} \le V_{in} \le V_{DD}$
$V_{SS} \le V_{out} \le V_{DD}$

$V_{control}$	V_{in} to V_{out} Resistance
V_{SS}	$>10^9$ Ohms typ
V_{DD}	3×10^2 Ohms typ

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Voltage (Control) "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.75	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.25	–	11.25	8.25	–	11.25	–	
Input Current (AL Device) Control	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device) Control	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}									pF
Control Input			–	–	–	5.0	7.5	–	–	
Switch Inputs		10	–	–	–	8.0	15	–	–	
Output Capacitance	C_{out}	10	–	–	–	8.0	–	–	–	pF
Feedthrough Capacitance	C_{in-out}	10	–	–	–	0.5	–	–	–	pF
Quiescent Current (AL Device)	I_Q	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_Q	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
ON Resistance (AL Device)	R_{ON}	5.0	–	800	–	250	1050	–	1200	Ω
		10	–	400	–	120	500	–	520	
		15	–	220	–	80	280	–	300	
ON Resistance (CL/CP Device)	R_{ON}	5.0	–	880	–	250	1050	–	1300	Ω
		10	–	450	–	120	500	–	550	
		15	–	250	–	80	280	–	320	
ΔON Resistance Between Any Two of Four Switches	ΔR_{ON}	5.0	–	–	–	25	–	–	–	Ω
		10	–	–	–	10	–	–	–	
		15	–	–	–	5.0	–	–	–	
Input/Output Leakage Current Switch OFF (AL Device)	–	15	–	±100	–	±0.01	±100	–	±1000	nAdc
Input/Output Leakage Current Switch OFF (CL/CP Device)	–	15	–	±300	–	±0.01	±300	–	±1000	nAdc

*The formulas given are for the typical characteristics only.
T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Propagation Delay Times V_{SS} = 0 Vdc						
Input to Output (R_L = 10 kΩ)	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 15.5 ns		5.0	–	20	40	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 6.0 ns		10	–	10	20	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 4.0 ns		15	–	7.0	15	
Control to Output (R_L = 1 kΩ)						
Output "1" to High Impedance	t_{PHZ}	5.0	–	40	80	ns
		10	–	35	70	
		15	–	30	60	
Output "0" to High Impedance	t_{PLZ}	5.0	–	40	80	ns
		10	–	35	70	
		15	–	30	60	
High Impedance to Output "1"	t_{PZH}	5.0	–	60	120	ns
		10	–	20	40	
		15	–	15	30	
High Impedance to Output "0"	t_{PZL}	5.0	–	60	120	ns
		10	–	20	40	
		15	–	15	30	
Sine Wave Distortion V_{SS} = −5 Vdc (V_{in} = 1.77 Vdc, RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	–	5.0	–	0.1	–	%
Frequency Response (Switch ON) V_{SS} = −5 Vdc (R_L = 1 kΩ, 20 Log_{10} $\frac{V_{out}}{V_{in}}$ = −3 dB)	–	5.0	–	65	–	MHz
Feedthrough Attenuation (Switch OFF) V_{SS} = −5 Vdc (R_L = 1 kΩ, 20 Log_{10} $\frac{V_{out}}{V_{in}}$ = −50 dB)	–	5.0	–	1.0	–	MHz
Crosstalk Between Any Two Switches V_{SS} = −5 Vdc (R_L = 1 kΩ, 20 Log_{10} $\frac{V_{out(B)}}{V_{in(A)}}$ = −50 dB, (Switch A ON, Switch B OFF)	–	5.0	–	8.0	–	MHz
Crosstalk, Control Input to Signal Output V_{SS} = −5 Vdc	–	5.0	–	300	–	mV
Maximum Control Input Frequency V_{SS} = 0 Vdc	–	5.0	–	6.0	–	MHz
(20 Log_{10} $\frac{V_{out}}{V_{in}}$ = −6 dB)		10	–	8.0	–	
		15	–	8.5	–	

*The formulas given are for the typical characteristics only.

TEST CIRCUITS

FIGURE 1 – INPUT VOLTAGE

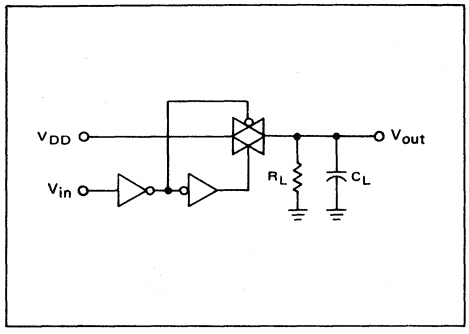


FIGURE 2 – PROPAGATION DELAY TIME, CONTROL TO OUTPUT

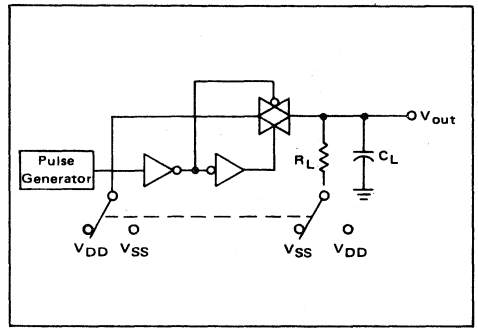


FIGURE 3 – BANDWIDTH AND FEEDTHROUGH ATTENUATION

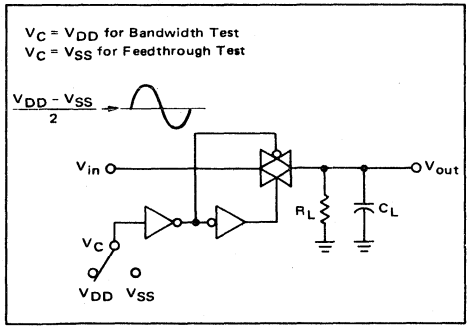


FIGURE 4 – CROSSTALK BETWEEN ANY TWO SWITCHES

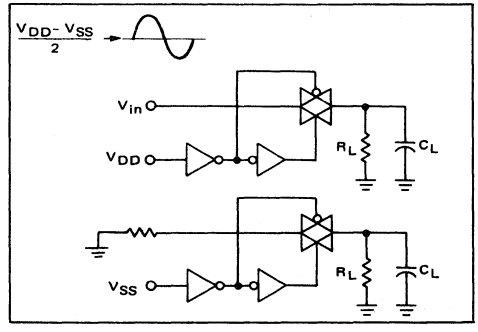


FIGURE 5 – CROSSTALK, CONTROL TO OUTPUT

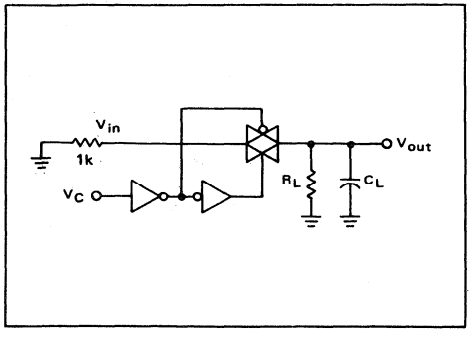


FIGURE 6 – MAXIMUM CONTROL FREQUENCY

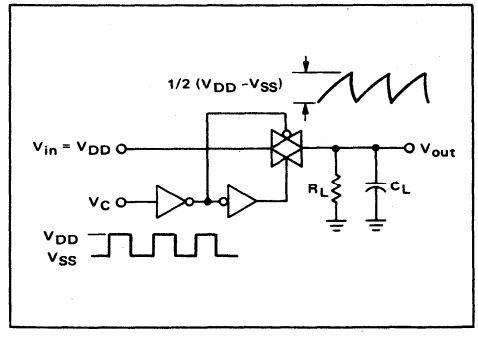
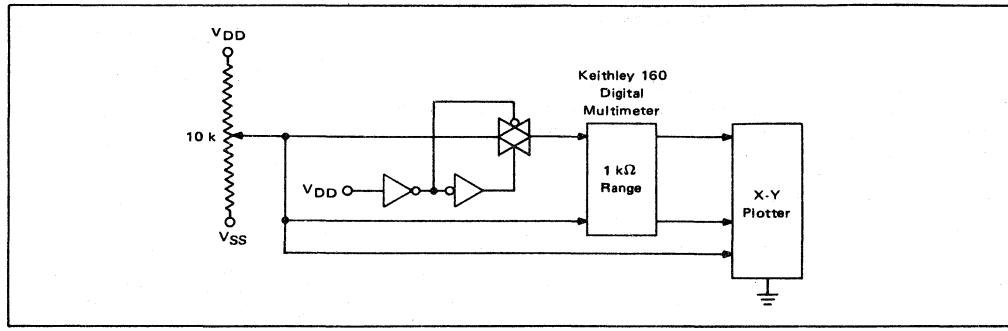


FIGURE 7 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 8 – V_{DD} = 7.5 V, V_{SS} = -7.5 V

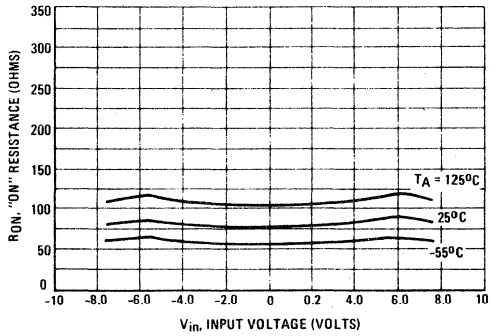


FIGURE 9 – V_{DD} = 5.0 V, V_{SS} = -5.0 V

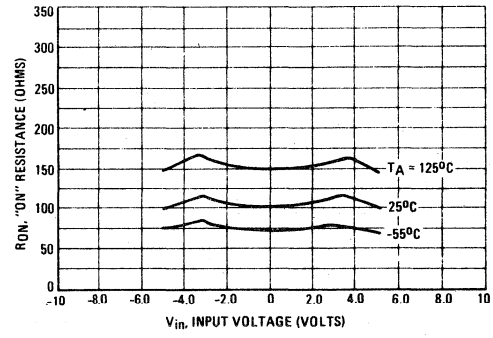


FIGURE 10 – V_{DD} = 2.5 V, V_{SS} = -2.5 V

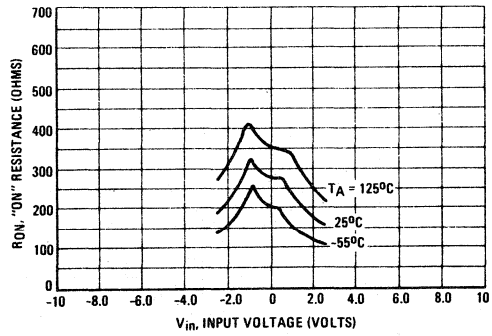
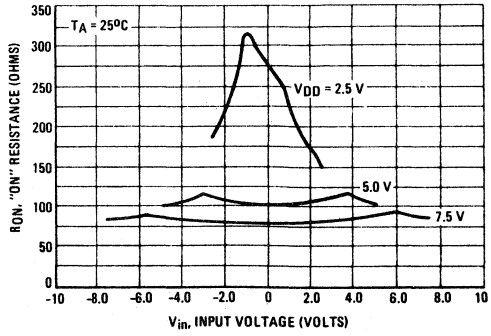


FIGURE 11 – COMPARISON AT 25°C, V_{DD} = -V_{SS}



MOTOROLA

MC14068B

8 – INPUT "NAND" GATE

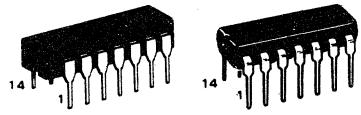
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4068B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

8-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

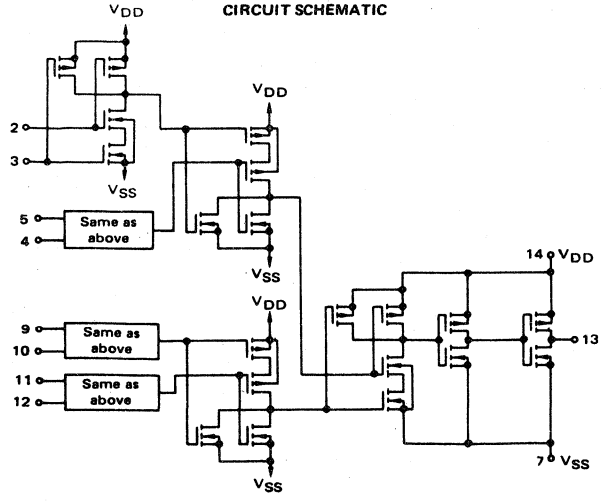
MC14XXXB — Suffix — Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

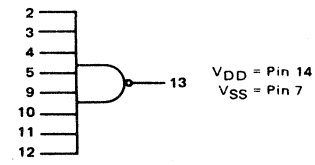
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14069UB

HEX INVERTER

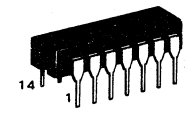
The MC14069UB hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications

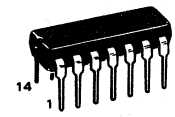
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

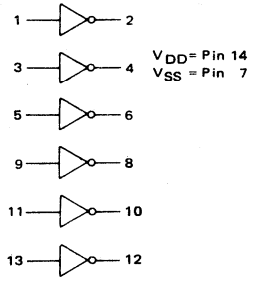
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

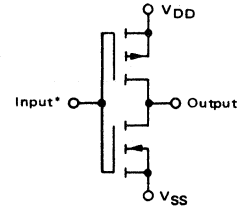
ORDERING INFORMATION

MC14XXXUB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

LOGIC DIAGRAM



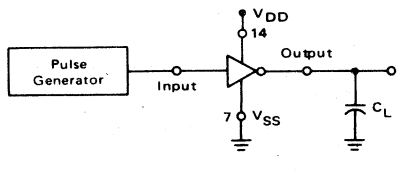
CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)

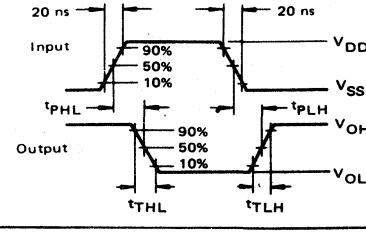


*Double diode protection on all inputs not shown.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5 Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0 Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)	I_T	5.0	$I_T = (0.3\ \mu A/kHz)\ f + I_{DD}/6$							µAdc
		10	$I_T = (0.6\ \mu A/kHz)\ f + I_{DD}/6$							
		15	$I_T = (0.9\ \mu A/kHz)\ f + I_{DD}/6$							
Output Rise and Fall Times** (C_L = 50 pF)	t_{TLH}, t_{THL}									ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	–	–	100	200	–	–	
t_{TLH}, t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	–	–	50	100	–	–	
t_{TLH}, t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	–	–	40	80	–	–	
Propagation Delay Times** (C_L = 50 pF)	t_{PLH}, t_{PHL}									ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 20 ns		5.0	–	–	–	65	125	–	–	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 22 ns		10	–	–	–	40	75	–	–	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 17 ns		15	–	–	–	30	55	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device

†To calculate total supply current at loads other than 50 pf:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3}(C_L - 50)V_{DD}f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
0.5 Vdc min @ V_{DD} = 5.0 Vdc
1.0 Vdc min @ V_{DD} = 10 Vdc
1.0 Vdc min @ V_{DD} = 15 Vdc

MOTOROLA

MC14070B

QUAD EXCLUSIVE "OR" GATE

MC14077B

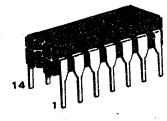
QUAD EXCLUSIVE "NOR" GATE

CMOS SSI

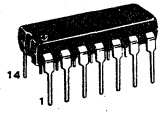
QUAD EXCLUSIVE "OR" AND "NOR" GATES

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- MC14070B — Replacement for CD4030B, CD4070B, and MC14507 Types
- MC14077B — Replacement for CD4077B Type



CASE 632
L SUFFIX
CERAMIC PACKAGE



CASE 646
P SUFFIX
PLASTIC PACKAGE

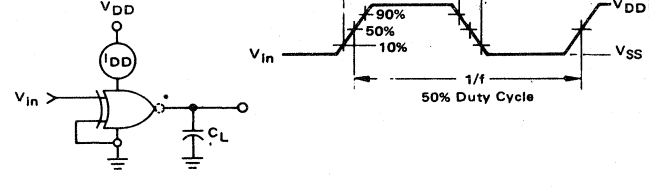
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

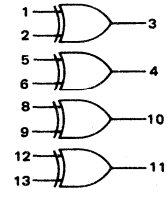
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

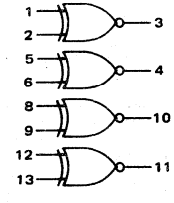


*Inverted output on MC14077B only.

MC14070B
Quad Exclusive OR Gate

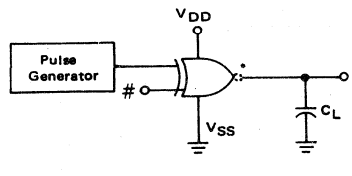


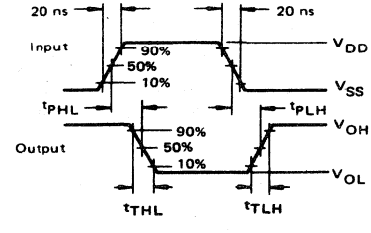
MC14077B
Quad Exclusive NOR Gate



V_{DD} = Pin 14
V_{SS} = Pin 7
(Both Devices)

FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





*Inverted output on MC14077B only.
#Connect unused input to V_{DD} for MC14070B, to V_{SS} for MC14077B.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.6 µA/kHz) f + I_{DD}							
		15	I_T = (0.9 µA/kHz) f + I_{DD}							
Output Rise and Fall Times** (C_L = 50 pF)	t_{TLH}, t_{THL}									ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	–	–	100	200	–	–	
t_{TLH}, t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	–	–	50	100	–	–	
t_{TLH}, t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	–	–	40	80	–	–	
Propagation Delay Times** (C_L = 50 pF)	t_{PLH}, t_{PHL}									ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns		5.0	–	–	–	175	350	–	–	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns		10	–	–	–	75	150	–	–	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		15	–	–	–	50	100	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14071
MC14071B

QUAD 2-INPUT "OR" GATE

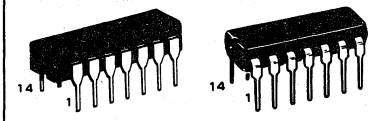
The MC14071 and MC14071B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14071B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4071A and CD4071B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

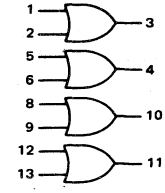
Delete for Non-B Device

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics of the B-Series device.

LOGIC DIAGRAM

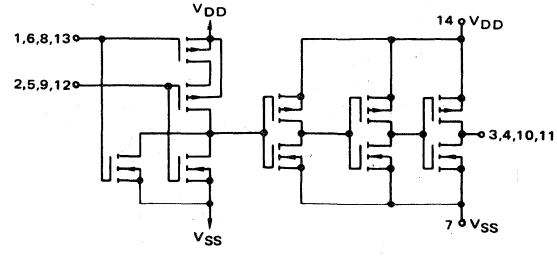


V_{DD} = Pin 14
V_{SS} = Pin 7

MC14071

CIRCUIT SCHEMATICS
(1/4 of Device Shown)

MC14071B



NOTE:
MC14071 (Non B) is not recommended for new designs. Use MC14071B.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14072B

DUAL 4 INPUT "OR" GATE

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4072B

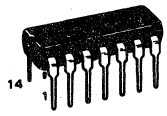
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

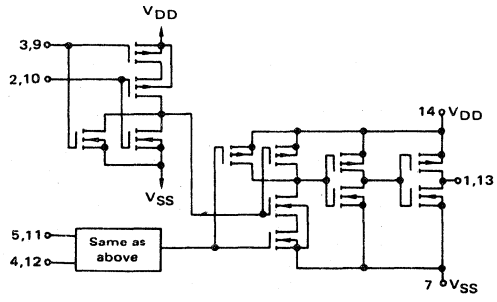
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

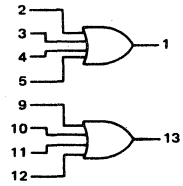
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATICS
(1/2 of Device Shown)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14073B

TRIPLE 3–INPUT "AND" GATE

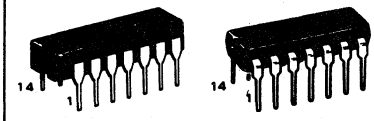
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4073B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "AND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS})

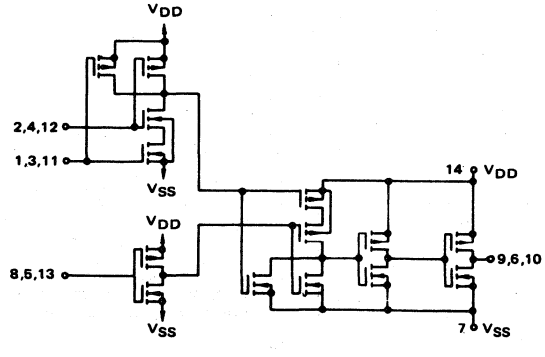
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ORDERING INFORMATION

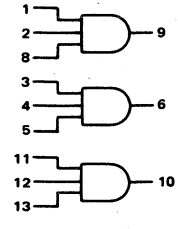
MC14XXXB — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATICS
(1/3 of Device Shown)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14075B

TRIPLE 3—INPUT "OR" GATE

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4075B

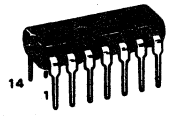
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

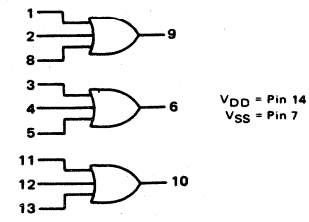
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

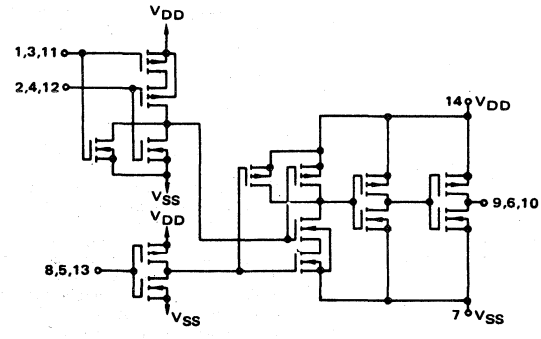
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

LOGIC DIAGRAM



CIRCUIT SCHEMATICS
(1/3 of Device Shown)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14076B

4-BIT D-TYPE REGISTER with THREE-STATE OUTPUTS

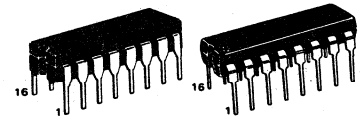
The MC14076B 4-Bit Register consists of four D-type flip-flops operating synchronously from a common clock. OR gated output-disable inputs force the outputs into a high-impedance state for use in bus organized systems. OR gated data-disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master reset is provided to clear all four flip-flops simultaneously independent of the clock or disable inputs.

- Three-State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- For Bus Buffer Registers
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD D-TYPE REGISTER with THREE STATE OUTPUTS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

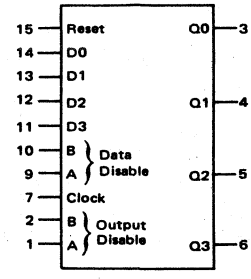
FUNCTION TABLE

INPUTS					OUTPUT
		Data Disable		Data	
Reset	Clock	A	B	D	Q
1	X	X	X	X	0
0	0	X	X	X	Q_n
0	⌐	1	X	X	Q_n
0	⌐	X	1	X	Q_n
0	⌐	0	0	0	0
0	⌐	0	0	1	1

When either output disable A or B (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

X = Don't Care.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.50 µA/kHz) f + I_{DD}							
		15	I_T = (2.25 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

FIGURE 1 – TIMING DIAGRAM

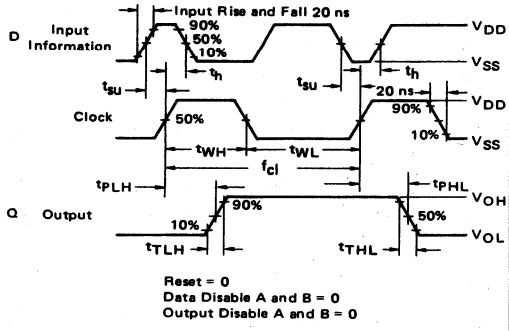
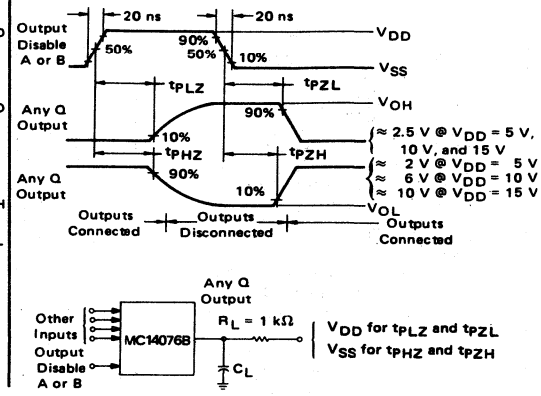
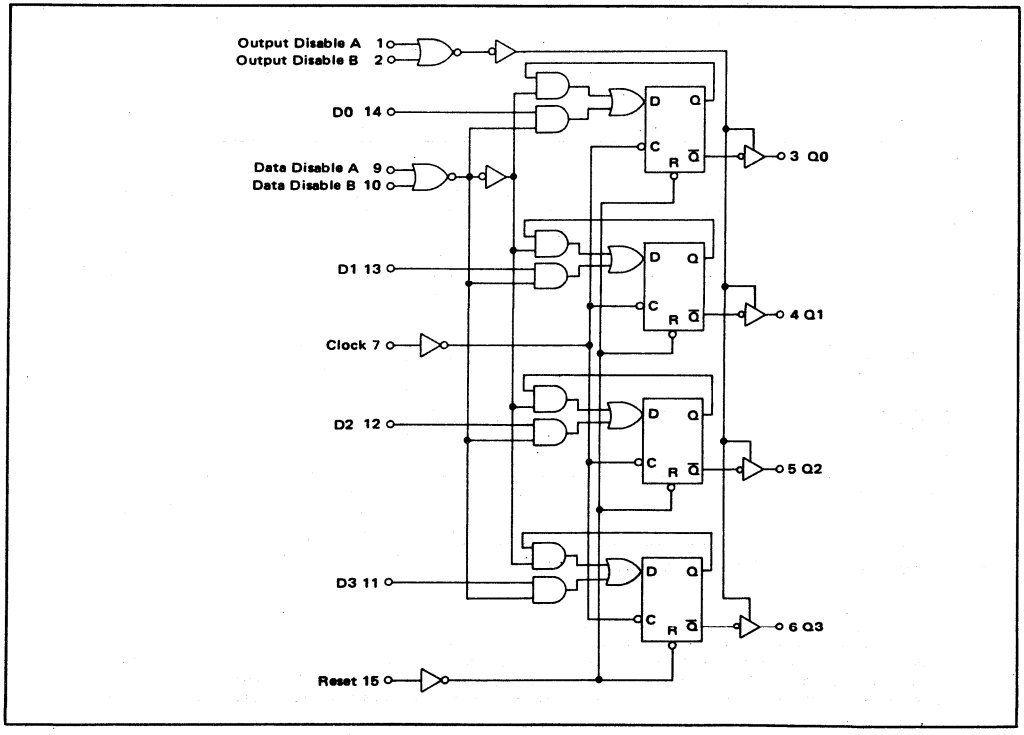


FIGURE 2 – THREE-STATE PROPAGATION DELAY WAVESHAPE AND CIRCUIT



FUNCTIONAL BLOCK DIAGRAM



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time, All B-Series Gates	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time, All B-Series Gates	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	
3-State Propagation Delay, Output "1" or "0" to High Impedance	t_{PHZ}, t_{PLZ}	5.0	–	150	300	ns
		10	–	60	120	
		15	–	45	90	
3-State Propagation Delay, High Impedance to "1" or "0" Level	t_{PZH}, t_{PZL}	5.0	–	200	400	ns
		10	–	80	160	
		15	–	60	120	
Clock Pulse Width	t_{WH}	5.0	260	130	–	ns
		10	110	55	–	
		15	80	40	–	
Reset Pulse Width	t_{WH}	5.0	370	185	–	ns
		10	150	75	–	
		15	110	55	–	
Data Setup Time	t_{su}	5.0	30	15	–	ns
		10	10	5	–	
		15	4	2	–	
Data Hold Time	t_h	5.0	130	65	–	ns
		10	60	30	–	
		15	50	25	–	
Data Disable Setup Time	t_{su}	5.0	220	110	–	ns
		10	80	40	–	
		15	50	25	–	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
Clock Pulse Frequency	f_{cl}	5.0	–	3.6	1.8	MHz
		10	–	9.0	4.5	
		15	–	12	6.0	

*The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14077B

QUAD EXCLUSIVE "NOR" GATE

FOR COMPLETE DATA
SEE MC14070B

CMOS SSI

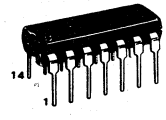
QUAD EXCLUSIVE "OR" AND "NOR" GATES

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- **MC14070B** – Replacement for CD4030B, CD4070B, and MC14507 Types
- MC14077B – Replacement for CD4077B Type



CASE 632
L SUFFIX
CERAMIC PACKAGE



CASE 646
P SUFFIX
PLASTIC PACKAGE

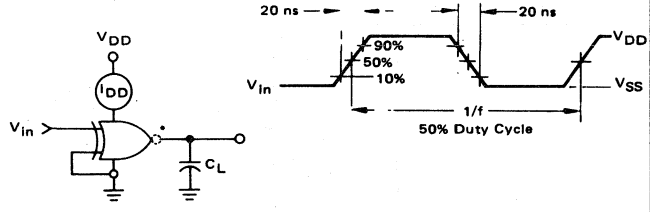
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

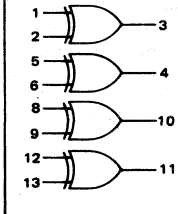
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

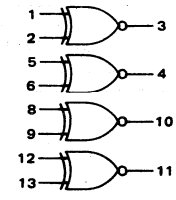


*Inverted output on MC14077B only.

MC14070B
Quad Exclusive OR Gate

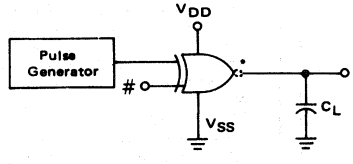


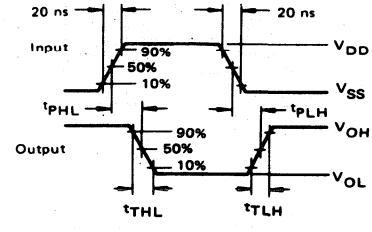
MC14077B
Quad Exclusive NOR Gate



V_{DD} = Pin 14
V_{SS} = Pin 7
(Both Devices)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





*Inverted output on MC14077B only.
#Connect unused input to V_{DD} for MC14070B, to V_{SS} for MC14077B.

MOTOROLA

MC14078B

8 – INPUT "NOR" GATE

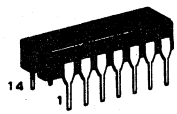
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4078B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

8-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

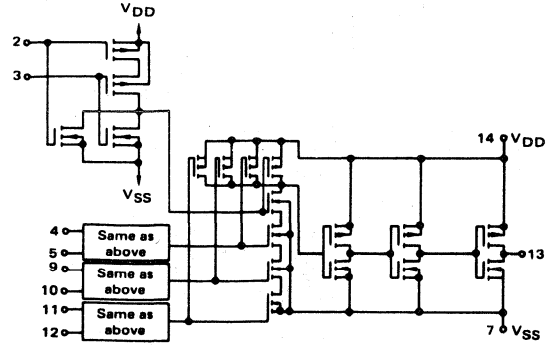
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

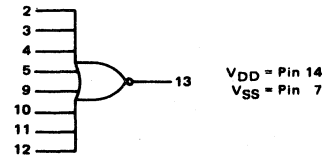
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



N.C. pins 1, 6, and 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14081
MC14081B

QUAD 2-INPUT "AND" GATE

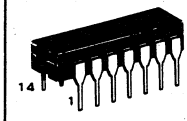
The MC14081 and MC14081B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14081B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4081A and CD4081B

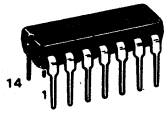
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "AND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

Delete for Non-B Device

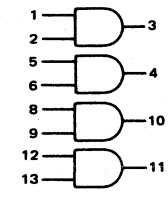
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics of the B-Series device.

LOGIC DIAGRAM

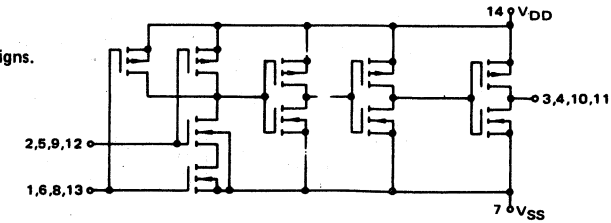


V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATICS
(1/4 of Device Shown)

MC14081

MC14081B



NOTE:
MC14081 (Non-B) is not recommended for new designs.
Use MC14081B.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14082B

DUAL 4-INPUT "AND" GATE

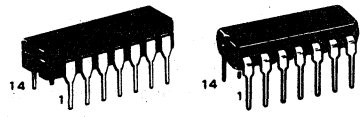
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4082B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "AND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS})

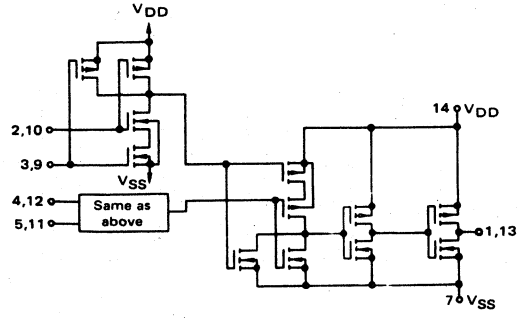
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ORDERING INFORMATION

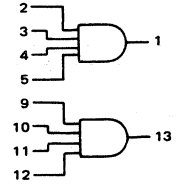
MC14XXXB — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATICS
(1/2 of Device Shown)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14093B

Advance Information

QUAD 2-INPUT "NAND" SCHMITT TRIGGER

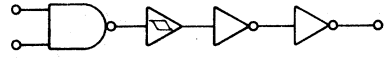
The MC14093B Schmitt trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14093B may be used in place of the MC14011B quad 2-input NAND gate for enhanced noise immunity or to "square up" slowly changing waveforms.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Compatible with CD4093
- Can be Used to Replace MC14011B

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

EQUIVALENT CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)



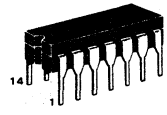
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This is advance information and specifications are subject to change without notice.

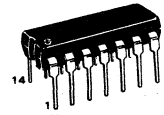
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND"
SCHMITT TRIGGER



L SUFFIX
CERAMIC PACKAGE
CASE 632

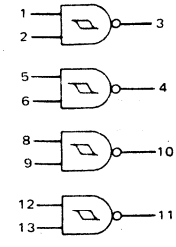


P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	–	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	–	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	–	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	–	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	–	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	–	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.2\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (2.4\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.6\ \mu A/kHz)\ f + I_{DD}$							
Hysteresis Voltage (Pins 2, 5, 9, 12, held high)	V_H‡	5.0	0.20	0.42	0.17	0.26	0.39	0.13	0.39	Vdc
		10	0.29	0.65	0.25	0.38	0.60	0.20	0.60	
		15	0.39	1.00	0.33	0.50	0.90	0.27	0.90	
Threshold Voltage (Pins 2, 5, 9, 12, held high) Positive-Going	V_{T+}	5.0	1.90	4.15	1.80	2.70	4.05	1.70	4.05	Vdc
		10	3.05	6.75	2.95	4.43	6.65	2.85	6.65	
		15	4.12	9.15	4.02	6.03	9.05	3.92	9.05	
Negative-Going	V_{T-}	5.0	1.63	3.76	1.63	2.44	3.66	1.53	3.66	Vdc
		10	2.70	6.18	2.70	4.05	6.08	2.60	6.08	
		15	3.59	8.40	3.69	5.53	8.30	3.70	8.30	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50)\ V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

‡$V_H = V_{T+} - V_{T-}$ (But maximum variation of V_H is specified as less than $V_{T+\ max} - V_{T-\ min}$).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0	–	125	250	ns
		10	–	50	100	
		15	–	40	80	

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVE FORMS

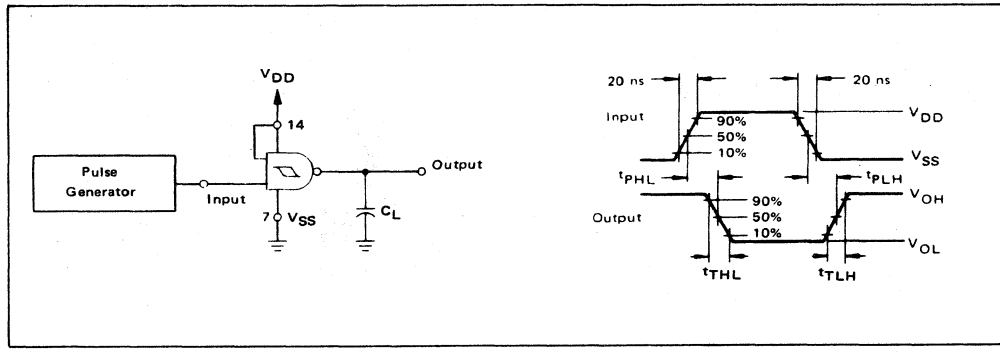


FIGURE 2 – TYPICAL SCHMITT TRIGGER APPLICATIONS

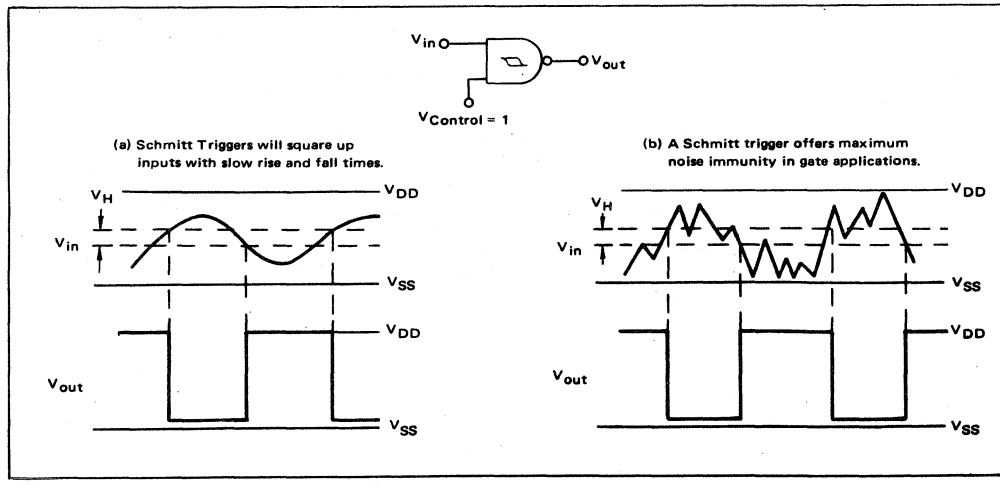
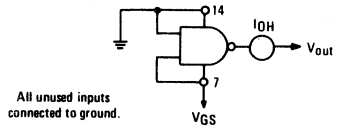


FIGURE 3 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT



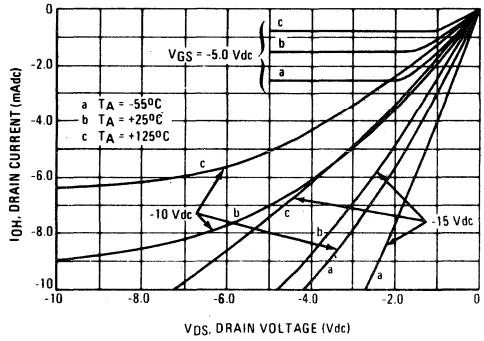
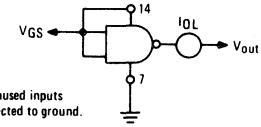


FIGURE 4 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



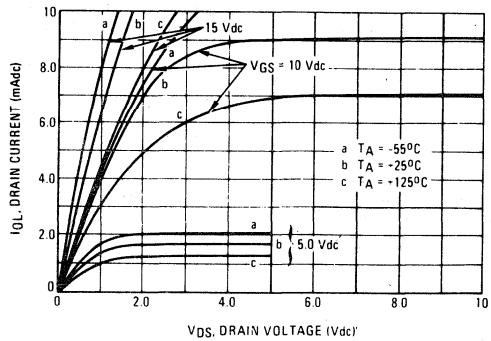
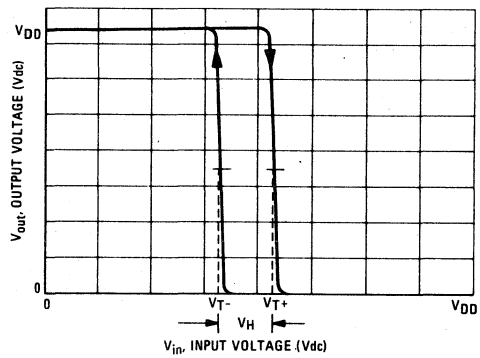


FIGURE 5 – TYPICAL TRANSFER CHARACTERISTICS



MOTOROLA

MC14094B

8-STAGE SHIFT/STORE REGISTER WITH THREE-STATE OUTPUTS

The MC14094B combines an 8-stage shift register with a data latch for each stage and a three-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q_S output data is for use in high-speed cascaded systems. The Q'_S output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

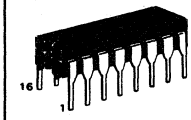
Outputs of the eight data latches are controlled by three-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

- Three-State Outputs
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTTL Loads Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Three-State Bus Compatible
- Pin-for-Pin Compatible with CD4094B

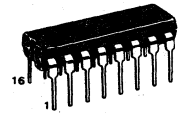
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-STAGE SHIFT/STORE REGISTER



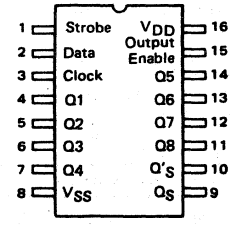
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Clock	Output Enable	Strobe	Data	Parallel Outputs Q1	Parallel Outputs Q_N	Serial Outputs Q_S*	Serial Outputs Q'_S
↑	0	X	X	3S	3S	Q7	No Chg.
↓	0	X	X	3S	3S	No Chg.	Q7
↑	1	0	X	No Chg.	No Chg.	Q7	No Chg.
↑	1	1	0	0	Q_N-1	Q7	No Chg.
↑	1	1	1	1	Q_N-1	Q7	No Chg.
↓	1	1	1	No Chg.	No Chg.	No Chg.	Q7

3S = Three-State
X = Don't Care
*At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (4.1\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (14\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (140\ \mu A/kHz)\ f + I_{DD}$							
3-State Output Leakage Current	I_{TL}	18	–	±0.4	–	±0.0001	±0.4	–	±12	µAdc

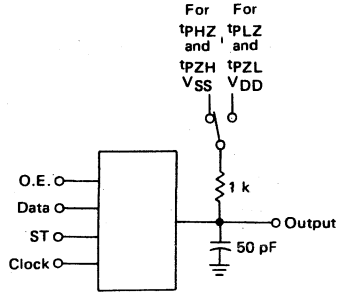
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

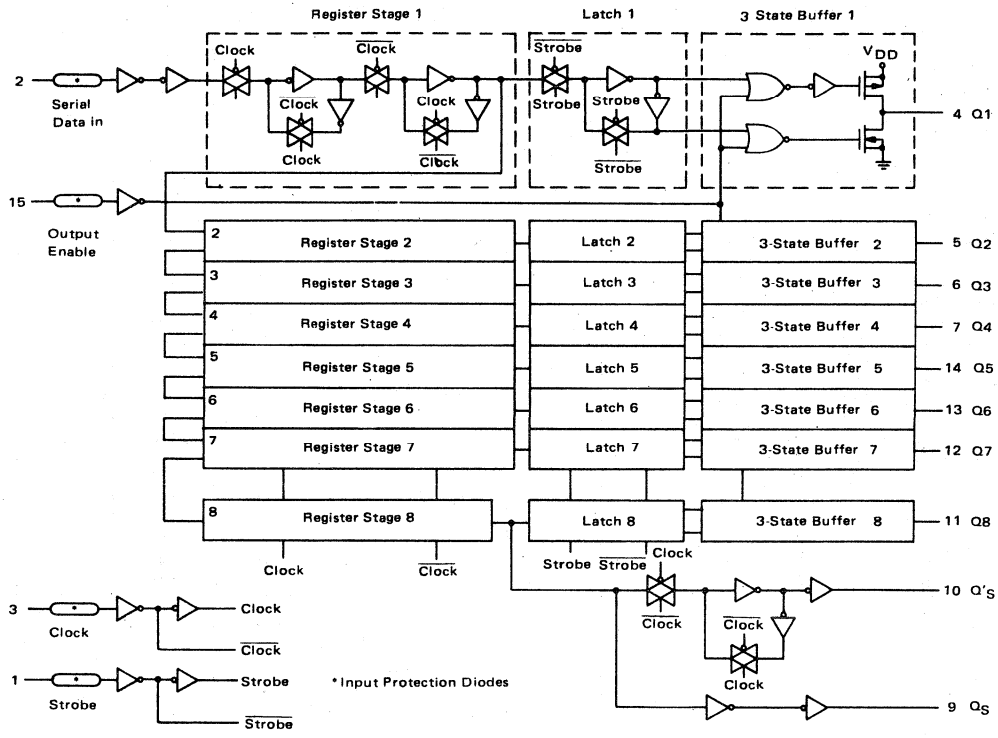
Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Serial out QS						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 305 ns		5.0	–	350	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 82 ns		15	–	95	190	
Clock to Serial out Q'S						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 350 ns		5.0	–	230	460	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 149 ns		10	–	110	220	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 62 ns		15	–	75	150	
Clock to Parallel out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 375 ns		5.0	–	420	840	
t_{PLH}, t_{PHL} = (0.35 ns/pF) C_L + 177 ns		10	–	195	390	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 122 ns		15	–	135	270	
Strobe to Parallel out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 245 ns		5.0	–	290	580	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 127 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	–	100	200	
Output Enable to Output						
t_{PHZ}, t_{PZL} = (0.90 ns/pF) C_L + 95 ns		5.0	–	140	280	
t_{PHZ}, t_{PZL} = (0.36 ns/pF) C_L + 57 ns		10	–	75	150	
t_{PHZ}, t_{PZL} = (0.26 ns/pF) C_L + 42 ns		15	–	55	110	
t_{PLZ}, t_{PZH} = (0.90 ns/pF) C_L + 180 ns		5.0	–	225	450	
t_{PLZ}, t_{PZH} = (0.36 ns/pF) C_L + 77 ns		10	–	95	190	
t_{PLZ}, t_{PZH} = (0.26 ns/pF) C_L + 57 ns		15	–	70	140	
Setup Time	t_{su}					ns
Data in to Clock		5.0	125	60	–	
		10	55	30	–	
		15	35	20	–	
Clock Pulse Width, High	t_{WH}	5.0	200	100	–	ns
		10	100	50	–	
		15	83	40	–	
Clock Rise Time	$t_{r(cl)}$	5	15	–	–	μs
		10	5.0	–	–	
		15	5.0	–	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.25	MHz
		10	–	5.0	2.5	
		15	–	6.0	3.0	
Strobe Pulse Width	t_{WL}	5.0	200	100	–	ns
		10	80	40	–	
		15	70	35	–	

*The formula given is for the typical characteristics only.

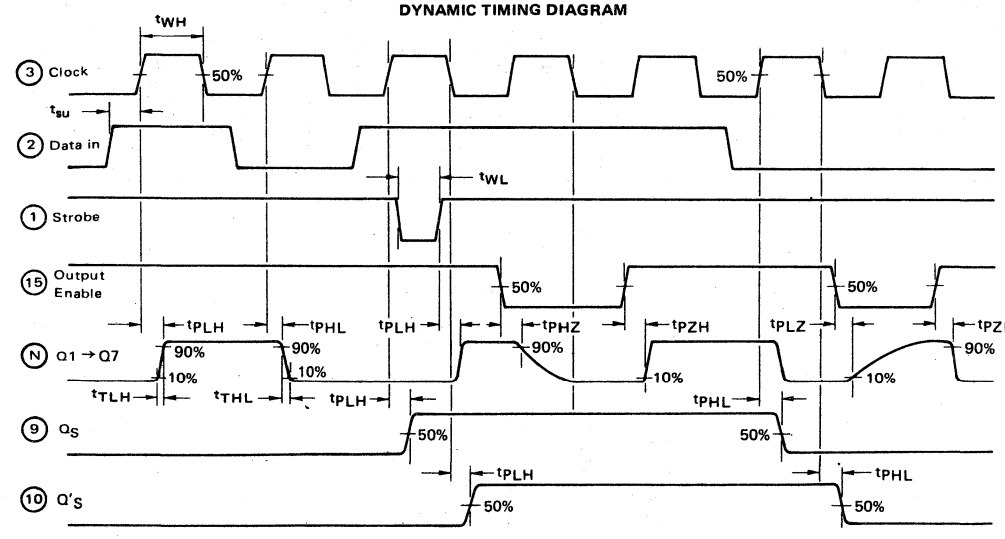
3-STATE TEST CIRCUIT



BLOCK DIAGRAM



DYNAMIC TIMING DIAGRAM



MOTOROLA

MC14099B
MC14599B

8-BIT ADDRESSABLE LATCHES

The MC14099B and MC14599B are 8-bit addressable latches. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. Chip enable must be high for writing into MC14599B. For the MC14599B the data pin is a bidirectional data port and for the MC14099B the input is a unidirectional write only port. The Write/$\overline{\text{Read}}$ line controls this port in the MC14599B.

The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/$\overline{\text{Read}}$ or Chip Enable.

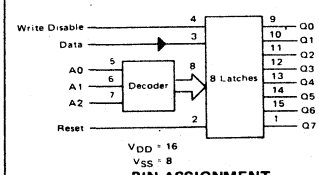
A Master Reset capability is available on both parts.

- Serial Data Input
- Parallel Output
- Low Input Capacitance – 5.0 pF typical
- Master Reset
- Noise Immunity – 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B
- Pin for pin compatible with Fairchild 4724.

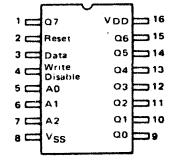
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

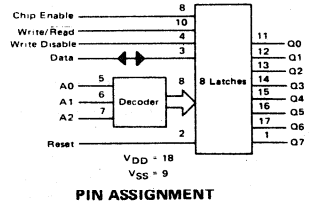
MC14099B



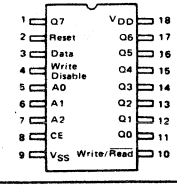
PIN ASSIGNMENT



MC14599B



PIN ASSIGNMENT

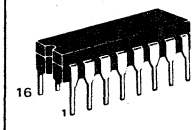


CMOS MSI

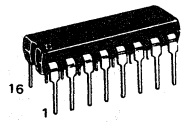
(LOW-POWER COMPLEMENTARY MOS)

8-BIT ADDRESSABLE LATCH

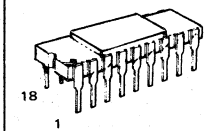
MC14599B WITH BIDIRECTIONAL PORT



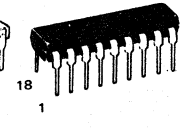
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 680



P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Input Capacitance MC14599B—Data (pin 3) (V_{in} = 0)	C_{in}	–	–	–	–	15.0	22.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.5 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.0 μA/kHz) f + I_{DD}							
		15	I_T = (4.5 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$$

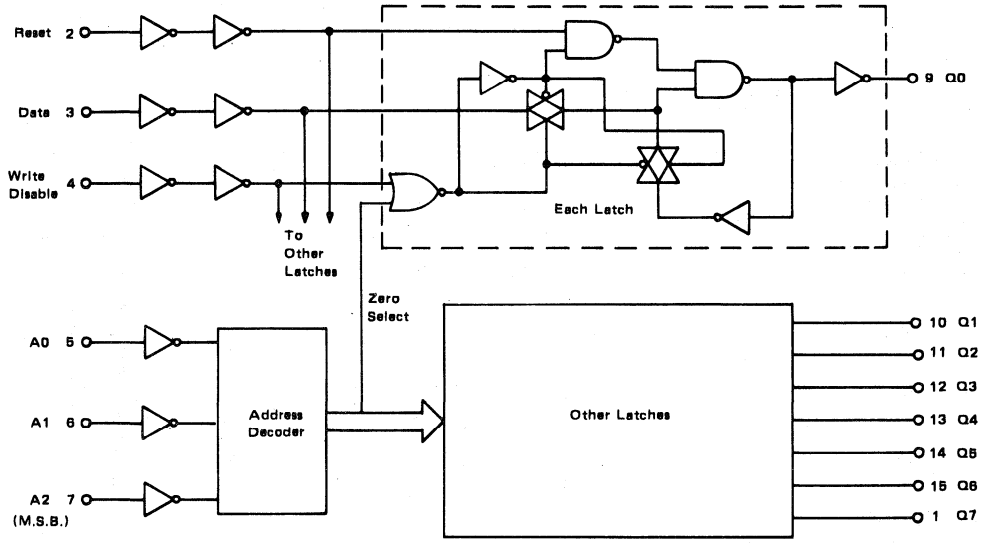
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L +32 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L +20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L +20 ns		15	–	40	80	
Propagation Delay Time	t_{PHL},					ns
Data to Output	t_{PLH}	5.0	–	200	400	
		10	–	75	150	
		15	–	50	100	
Write Disable to Output		5.0	–	200	400	ns
		10	–	80	160	
		15	–	60	120	
Reset to Output		5.0	–	175	350	ns
		10	–	80	160	
		15	–	65	130	
Address, CE to Output		5.0	–	225	450	ns
		10	–	100	200	
		15	–	75	150	
Propagation Delay Time, MC14599B only	t_{PHL},					ns
Chip Enable, Write/Read to Data	t_{PLH}	5.0	–	200	400	
		10	–	80	160	
		15	–	65	130	
Address to Data		5.0	–	200	400	ns
		10	–	90	180	
		15	–	75	150	
Minimum Pulse Widths	t_{WH},					ns
Data	t_{WL}	5.0	200	100	–	
		10	100	50	–	
		15	80	40	–	
Address		5.0	400	200	–	ns
		10	200	100	–	
		15	125	65	–	
Reset		5.0	150	75	–	ns
		10	75	40	–	
		15	50	25	–	
Write Disable		5.0	320	160	–	ns
		10	160	80	–	
		15	120	60	–	
Set Up Time	t_{su}					ns
Data		5.0	100	50	–	
		10	50	25	–	
		15	35	20	–	
Hold Time	t_h					ns
Data		5.0	150	75	–	
		10	75	40	–	
		15	50	25	–	

MC14099B
FUNCTION DIAGRAM

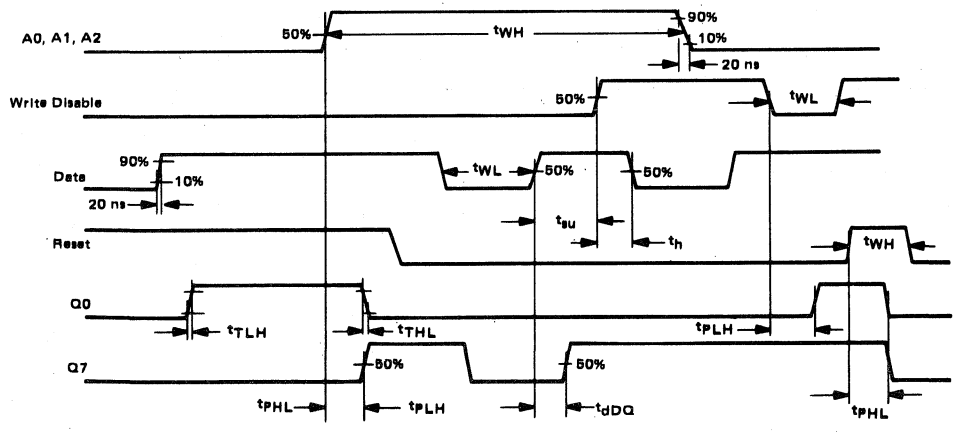


TRUTH TABLE

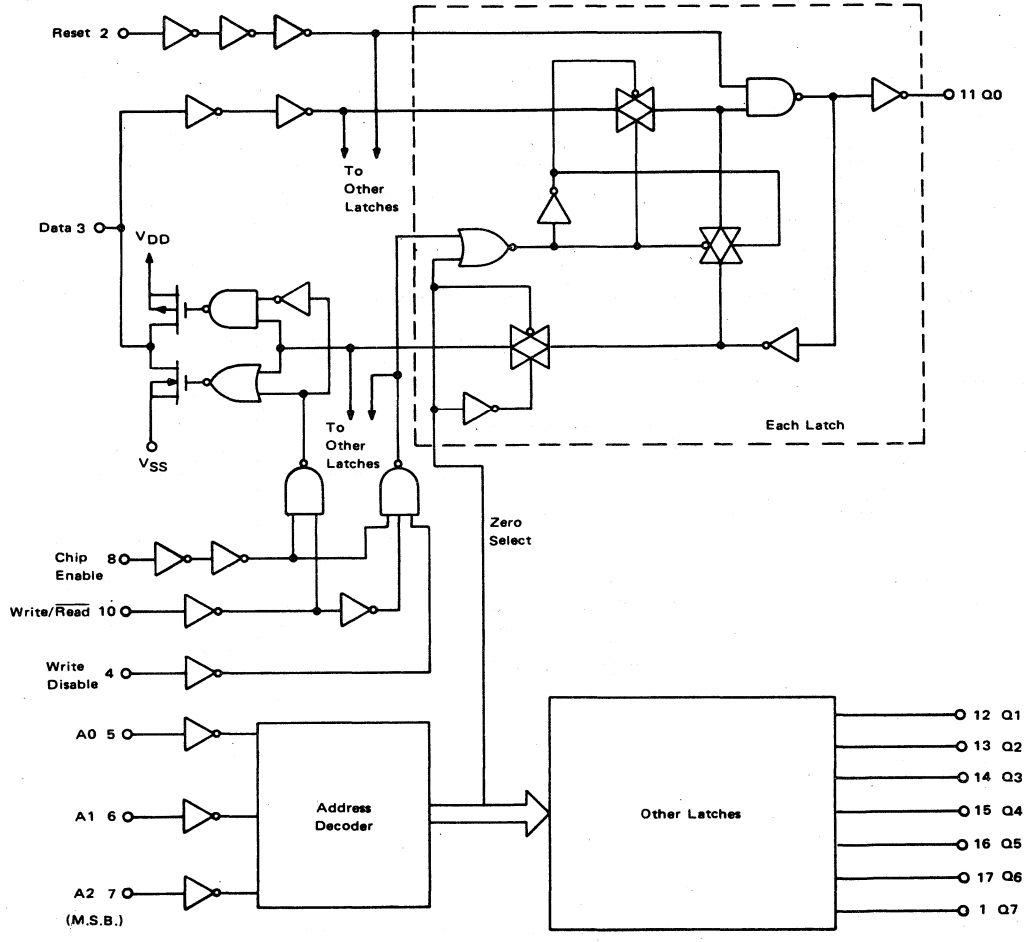
Write Disable	Reset	Addressed Latch	Unaddressed Latch
0	0	Data	Q_n*
0	1	Data	Reset†
1	0	Q_n*	Q_n*
1	1	Reset	Reset

* Q_n is previous state of latch.
† Reset to zero state.

TIMING DIAGRAM



MC14599B
FUNCTION DIAGRAM

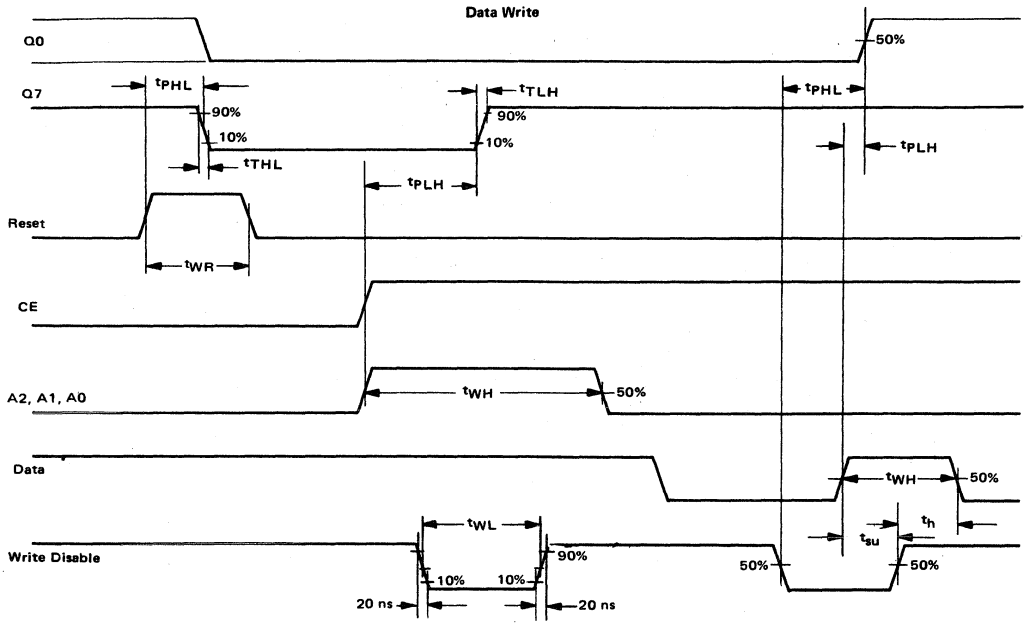


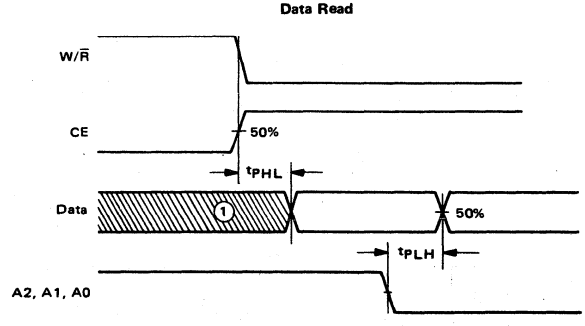
TRUTH TABLE

Chip Enable	Write/$\overline{\text{Read}}$	Write Disable	Reset	Addressed Latch	Other Latches	Data Pin
0	X	X	0	*	*	Z
1	1	0	0	Data	*	Input
1	1	1	0	*	*	Z
1	0	X	0	*	*	Q_n
X	X	X	1	0	0	Z/0

X = Don't care.
* = No change in state of latch.
Z = High impedance.
Q_n = State of addressed latch.

MC14599B
TIMING DIAGRAMS





NOTE: 1. Invalid Data Output
2. Reset in LOW State

MOTOROLA

MC14160B
DECADE COUNTER
with Asynchronous Clear

MC14161B
4-BIT BINARY COUNTER
with Asynchronous Clear

MC14162B
DECADE COUNTER
with Synchronous Clear

MC14163B
4-BIT BINARY COUNTER
with Synchronous Clear

CMOS MSI

SYNCHRONOUS PROGRAMMABLE 4-BIT COUNTERS

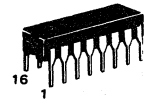
The MC14160B – MC14163B are synchronous programmable counters constructed with complementary MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These counters are functionally equivalent to the 74160–74163 TTL counters.

Two are synchronous programmable decade counters with asynchronous and synchronous clear inputs respectively (MC14160B, MC14162B. The other two are synchronous programmable 4-bit binary counters with the asynchronous and synchronous clear respectively (MC14161B, MC14163B).

- Internal Look-Ahead for Fast Counting
- Carry Output for N-Bit Cascading
- Synchronously Programmable
- Synchronous Counting
- Load Control Line
- Synchronous or Asynchronous Clear
- Positive Edge Clocked



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

ORDERING INFORMATION

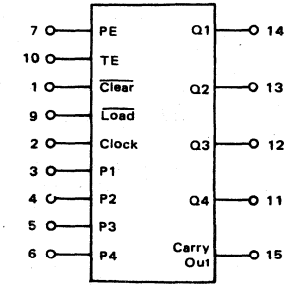
MC14xxxB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.56 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.1 µA/kHz) f + I_{DD}							
		15	I_T = (1.9 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

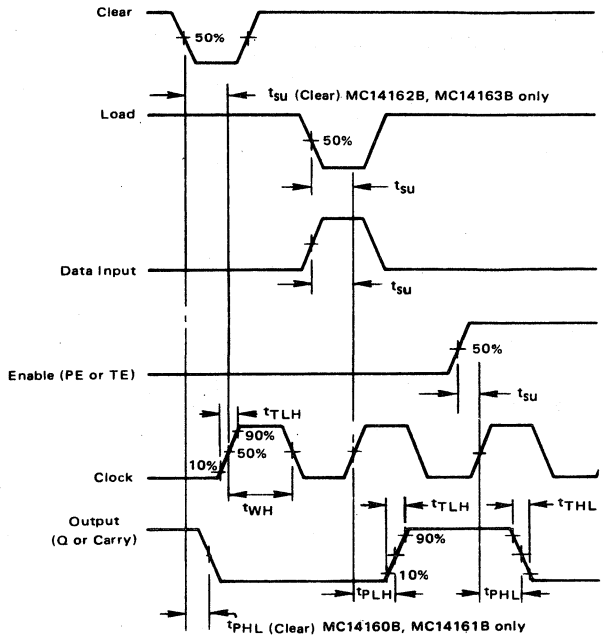
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{TLH} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 305 ns		5.0	–	350	700	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	–	100	200	
Clock to Carry Out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 395 ns		5.0	–	440	880	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 167 ns		10	–	185	370	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 112 ns		15	–	125	250	
TE to Carry Out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 255 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 112 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 77 ns		15	–	90	180	
Clear to Q (MC14160B, MC14161B only)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 110 ns		5.0	–	350	700	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 37 ns		10	–	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 22 ns		15	–	100	200	
Minimum Setup Time						
Data to Clock	t_{su}	5.0	320	160	–	ns
		10	130	65	–	
		15	90	45	–	
Load to Clock		5.0	600	300	–	
		10	260	130	–	
		15	180	90	–	
Enable to Clock (PE or TE)		5.0	420	210	–	
		10	170	85	–	
		15	120	60	–	
Clear to Clock (MC14162B, MC14163B only)		5.0	310	155	–	
		10	110	55	–	
		15	70	35	–	
Clock Pulse Width, High	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	70	35	–	
Clock Rise Time	t_{TLH}	5	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
Clock Pulse Frequency	f_{cl}	5.0	–	2.0	1.0	MHz
		10	–	5.0	2.5	
		15	–	8.0	4.0	

*The formula given is for the typical characteristics only.

SWITCHING WAVEFORMS

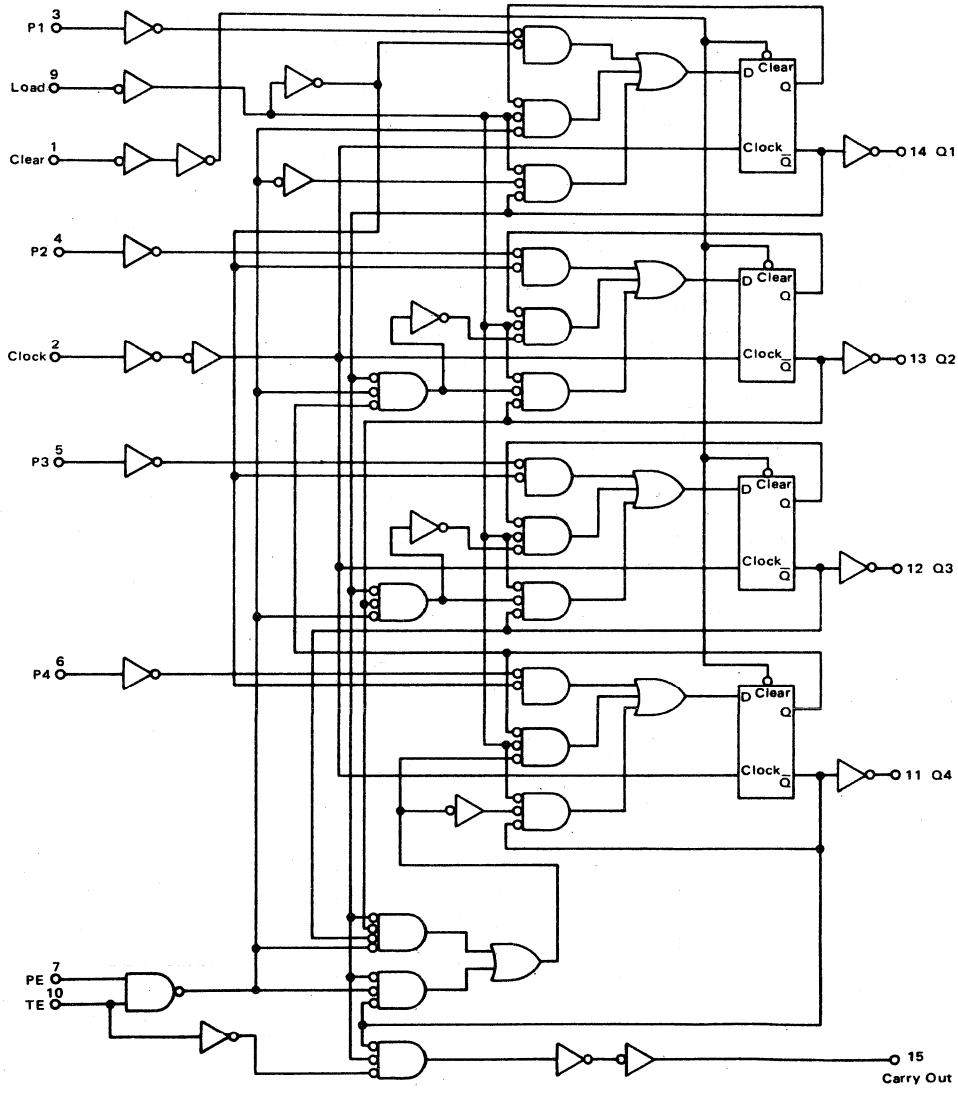


FUNCTIONAL DESCRIPTION

These counters are fully programmable; that is the outputs may be preset to either level. As presetting is synchronous, settling up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the MC14160B, MC14161B is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs. The clear function for the MC14162B and MC14163B is synchronous and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily; decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (PE, TE) must be high to count, and enable input TE fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages.

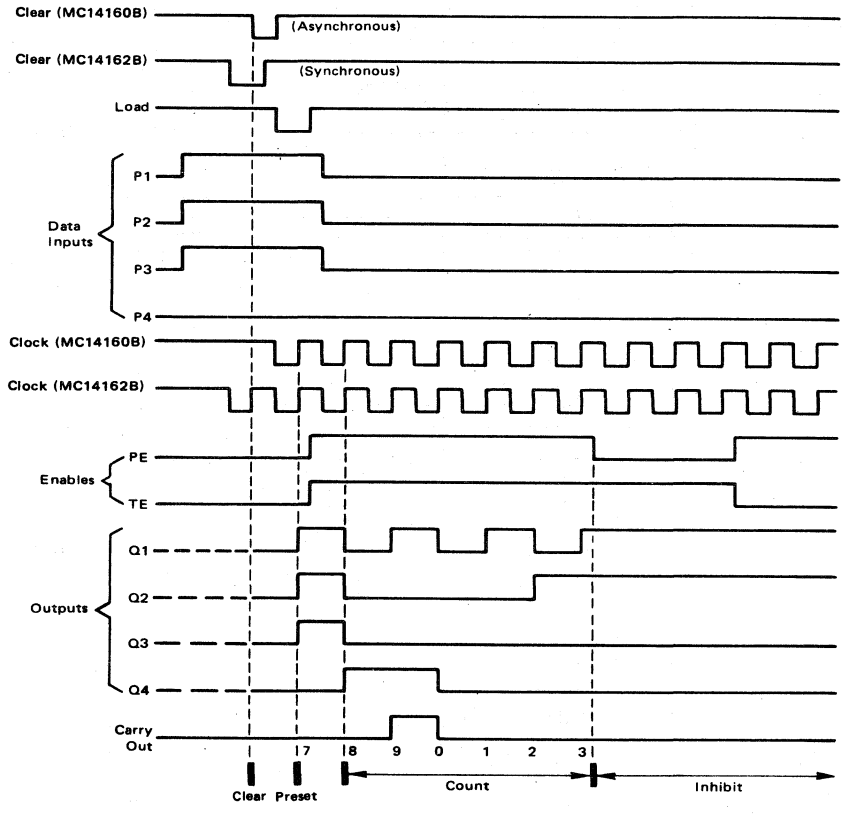
MC14160B, MC14162B LOGIC DIAGRAM
(Clear is synchronous for MC14162B)



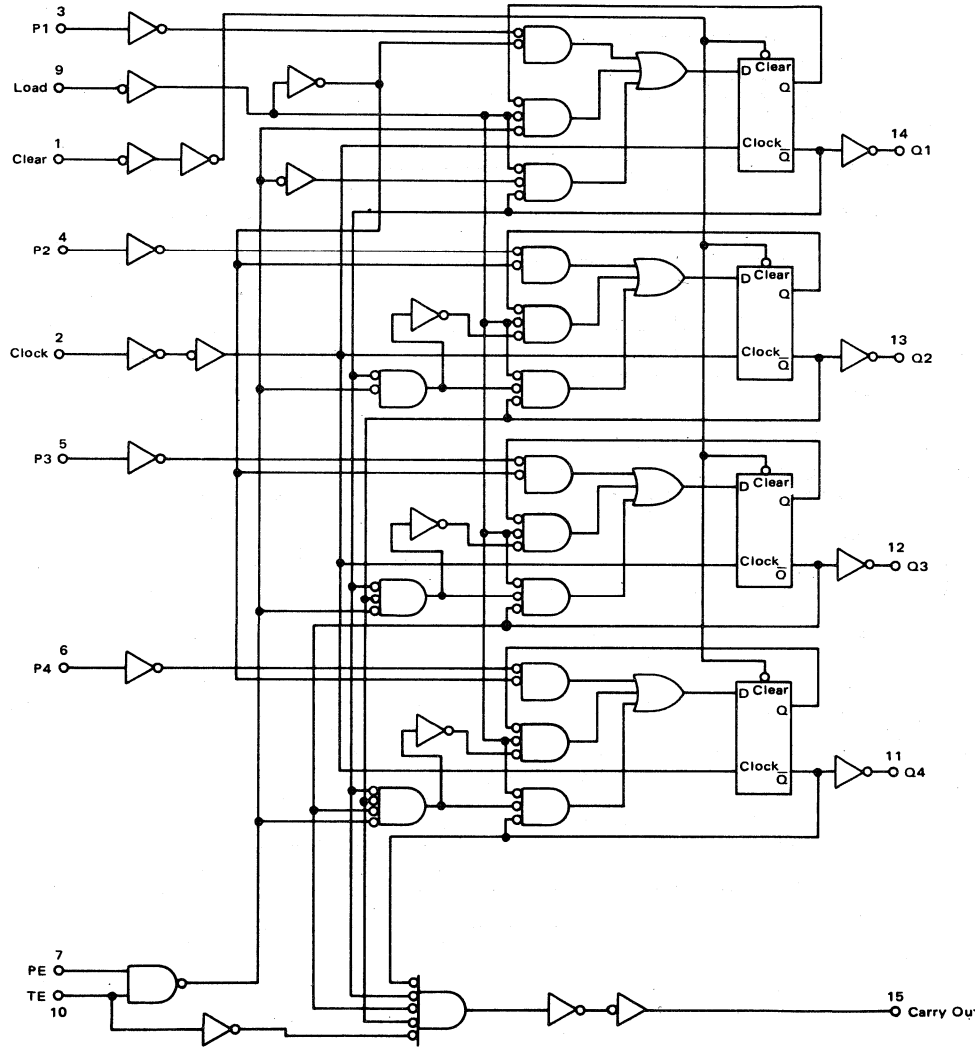
MC14160B, MC14162B TIMING DIAGRAM

Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit



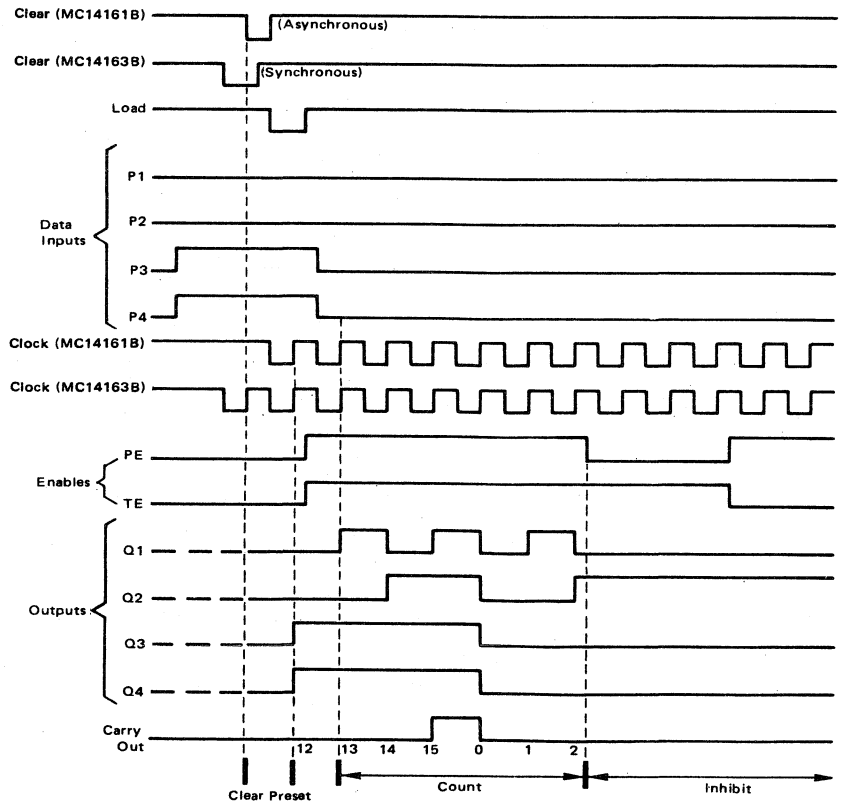
MC14161B, MC14163B LOGIC DIAGRAM
(Clear is Synchronous for MC14163B)



MC14161B, MC14163B TIMING DIAGRAM

Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two,
4. Inhibit



MOTOROLA

MC14174B

CMOS MSI

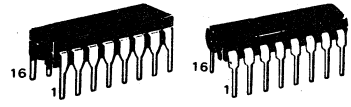
(LOW-POWER COMPLEMENTARY MOS)

HEX TYPE D FLIP-FLOP

HEX TYPE D FLIP-FLOP

The MC14174B hex type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data on the D inputs which meets the setup time requirements is transferred to the Q outputs on the positive edge of the clock pulse. All six flip-flops share common clock and reset inputs. The reset is active low, and independent of the clock.

- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Output Compatible with Two HTL Loads, Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74174



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

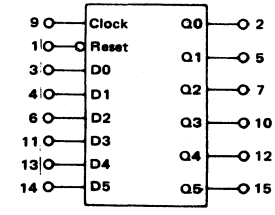
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE
(Postive Logic)

INPUTS			OUTPUT	
Clock	Data	$\overline{\text{Reset}}$	Q	
⎍	0	1	0	
⎍	1	1	1	
⎎	X	1	Q	No Change
X	X	0	0	

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.1\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (2.3\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.7\ \mu A/kHz)\ f + I_{DD}$							

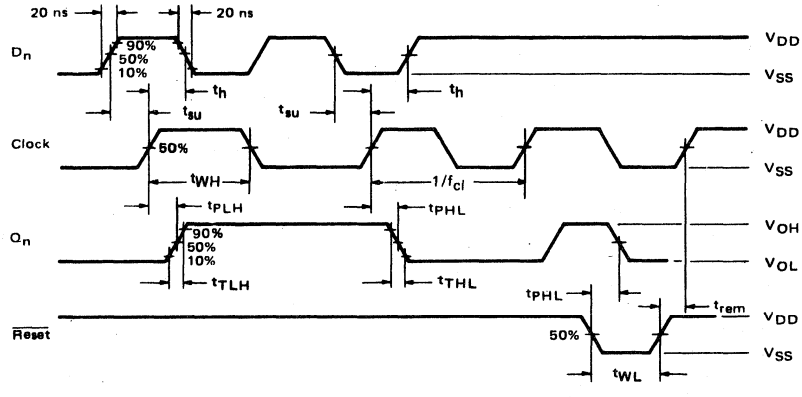
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

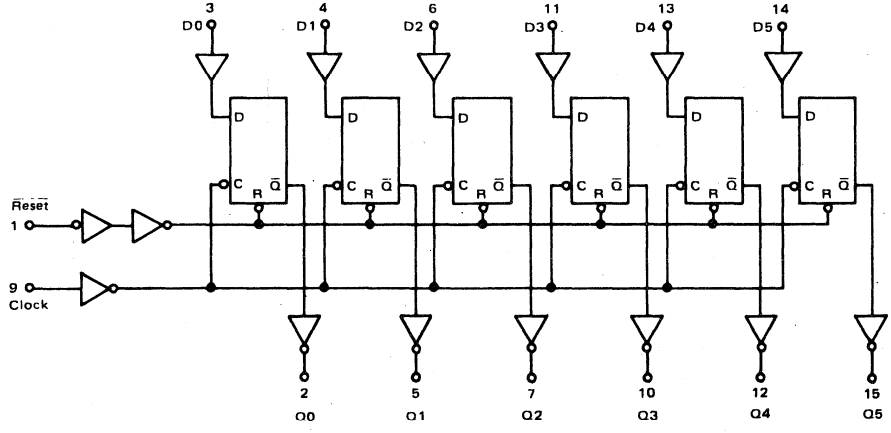
Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time – Clock to Q	t_{PLH},					ns
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 165 ns	t_{PHL}	5.0	–	210	400	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 64 ns		10	–	85	160	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 52 ns		15	–	65	120	
Propagation Delay Time – $\overline{\text{Reset}}$ to Q	t_{PHL}					ns
t_{PHL} = (0.9 ns/pF) C_L + 205 ns		5.0	–	250	500	
t_{PHL} = (0.36 ns/pF) C_L + 79 ns		10	–	100	200	
t_{PHL} = (0.26 ns/pF) C_L + 62 ns		15	–	75	150	
Clock Pulse Width	t_{WH}	5.0	150	75	–	ns
		10	90	45	–	
		15	70	35	–	
$\overline{\text{Reset}}$ Pulse Width	t_{WL}	5.0	200	100	–	ns
		10	100	50	–	
		15	80	40	–	
Clock Pulse Frequency	f_{cl}	5.0	–	7.0	2.0	MHz
		10	–	12.0	5.0	
		15	–	15.5	6.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
Data Setup Time	t_{su}	5.0	40	20	–	ns
		10	20	10	–	
		15	15	0	–	
Data Hold Time	t_h	5.0	80	40	–	ns
		10	40	20	–	
		15	30	15	–	
$\overline{\text{Reset}}$ Removal Time**	t_{rem}	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	

*The formulas given are for the typical characteristics only.
**The reset signal must be high prior to a positive-going transition of the clock.

TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



MOTOROLA

MC14175B

CMOS SSI

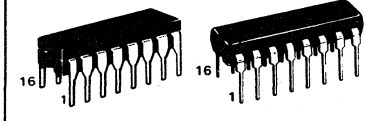
(LOW-POWER COMPLEMENTARY MOS)

QUAD TYPE D FLIP-FLOP

QUAD TYPE D FLIP-FLOP

The MC14175B quad type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each of the four flip-flops is positive-edge triggered by a common clock input (C). An active-low reset input ($\overline{R}$) asynchronously resets all flip-flops. Each flip-flop has independent Data (D) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Complementary Outputs
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Output Compatible with Two HTL Loads, Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74175



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

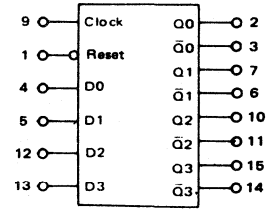
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE
(Postive Logic)

INPUTS			OUTPUTS		
Clock	Data	$\overline{Reset}$	Q	$\overline{Q}$	
⌐	0	1	0	1	
⌐	1	1	1	0	
¬	X	1	Q	$\overline{Q}$	No Change
X	X	0	0	1	

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.7\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (3.4\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (5.0\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

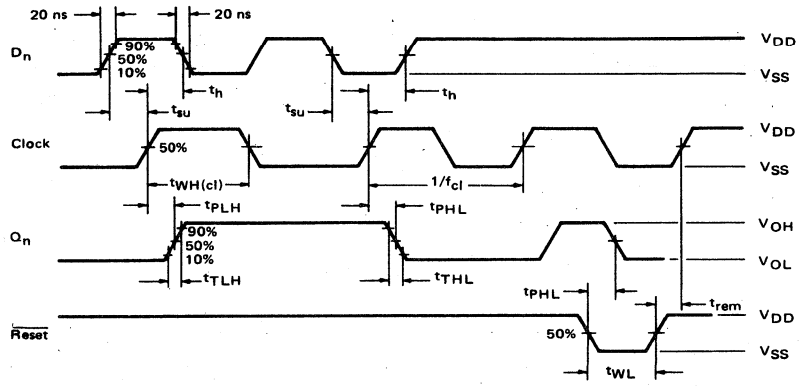
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF)C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time – Clock to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 175 ns		5.0	–	220	400	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 72 ns		10	–	90	160	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 57 ns		15	–	70	120	
Propagation Delay Time – $\overline{\text{Reset}}$ to Q	t_{PHL}					ns
t_{PHL} = (0.9 ns/pF) C_L + 280 ns		5.0	–	325	500	
t_{PHL} = (0.36 ns/pF) C_L + 112 ns		10	–	130	200	
t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	–	100	150	
Clock Pulse Width	t_{WH}	5.0	250	110	–	ns
		10	100	45	–	
		15	75	35	–	
$\overline{\text{Reset}}$ Pulse Width	t_{WL}	5.0	200	100	–	ns
		10	80	40	–	
		15	60	30	–	
Clock Pulse Frequency	f_{cl}	5.0	–	4.5	2.0	MHz
		10	–	11	5.0	
		15	–	14	6.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
Data Setup Time	t_{su}	5.0	120	60	–	ns
		10	50	25	–	
		15	40	20	–	
Data Hold Time	t_h	5.0	80	40	–	ns
		10	40	20	–	
		15	30	15	–	
$\overline{\text{Reset}}$ Removal Time**	t_{rem}	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	

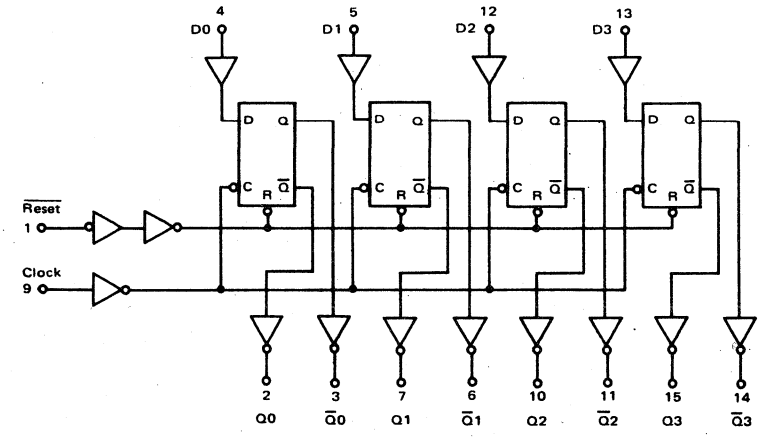
*The formulas given are for the typical characteristics only.

**The reset signal must be high prior to a positive-going transition of the clock.

TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



MOTOROLA

MC14194B

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

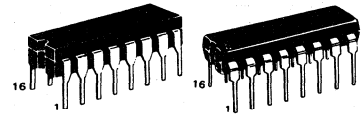
The MC14194B is a 4-bit static shift register capable of operating in the parallel load, serial shift left, serial shift right, or hold mode. The asynchronous $\overline{\text{Reset}}$ input, when at a low level, overrides all other inputs, resets all stages, and forces all outputs low. When $\overline{\text{Reset}}$ is at a logic 1 level, the two mode control inputs, S0 and S1, control the operating mode as shown in the truth table. Both serial and parallel operation are triggered on the positive-going transition of the Clock input. The Parallel Data, Data Shift, and mode control inputs must be stable for the specified setup and hold times before and after the positive-going Clock transition.

- Quiescent Current = 5.0 nA typ/pkg @ 5 Vdc
- Typical Shift Frequency = 9.0 MHz @ 10 Vdc
- Synchronous Right/Left Serial Operation
- Synchronous Parallel Load
- Asynchronous Hold (Do Nothing) Mode
- Functional Pin for Pin Equivalent of 74194

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

TRUTH TABLE

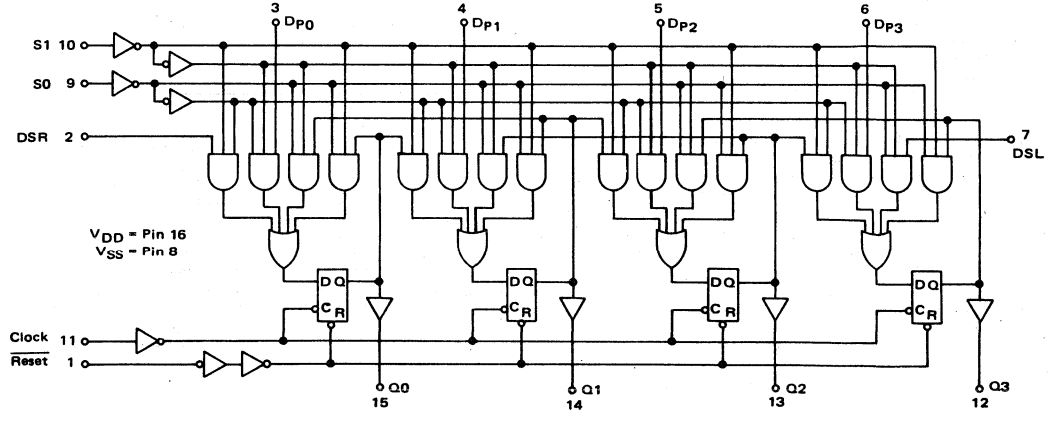
OPERATING MODE	INPUTS ($\overline{\text{Reset}}$ = 1)					OUTPUTS (@ t_{n+1})			
	S1	S0	DSR	DSL	D_{P0-3}	Q0	Q1	Q2	Q3
Hold	0	0	X	X	X	Q0	Q1	Q2	Q3
Shift Left	1	0	X	0	X	Q1	Q2	Q3	0
	1	0	X	1	X	Q1	Q2	Q3	1
Shift Right	0	1	0	X	X	0	Q0	Q1	Q2
	0	1	1	X	X	1	Q0	Q1	Q2
Parallel	1	1	X	X	0	0	0	0	0
	1	1	X	X	1	1	1	1	1

X = Don't Care
t_{n+1} = State after the next positive-going transition of the clock.

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	12.0	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.95\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (1.9\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (2.9\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

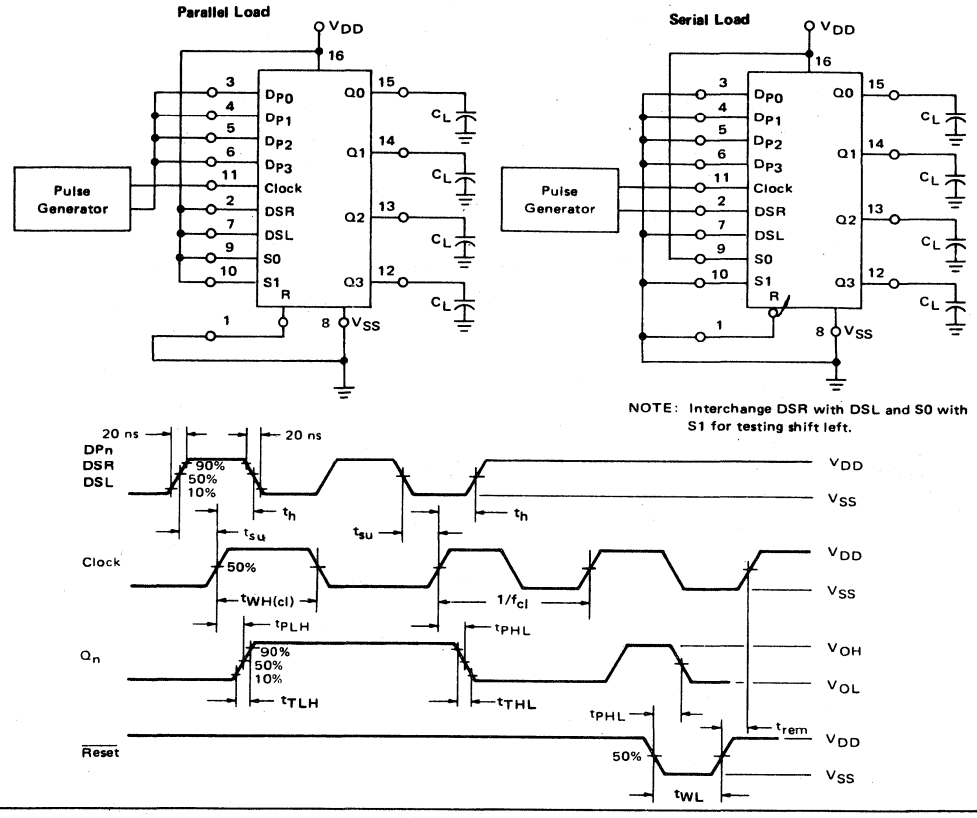
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},t_{PHL}					ns
Clock to Q						
t_{PLH},t_{PHL} = (0.9 ns/pF) C_L + 230 ns		5.0	–	275	550	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 92 ns		10	–	110	220	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 72 ns		15	–	85	170	
$\overline{Reset}$ to Q	t_{PHL}					ns
t_{PHL} = (0.9 ns/pF) C_L + 305 ns		5.0	–	350	700	
t_{PHL} = (0.36 ns/pF) C_L + 122 ns		10	–	140	280	
t_{PHL} = (0.26 ns/pF) C_L + 97 ns		15	–	110	220	
Clock Pulse Width	t_{WH}	5.0	280	140	–	ns
		10	110	55	–	
		15	85	40	–	
$\overline{Reset}$ Pulse Width	t_{WH}	5.0	180	90	–	ns
		10	70	35	–	
		15	50	26	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.6	1.8	MHz
(Shift Right or Left Mode)		10	–	9.0	4.5	
		15	–	12	6.0	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0			15	μs
		10			5	
		15			4	
Setup Time	t_{su}					ns
Data to Clock		5.0	10	-8.0	–	
		10	20	0	–	
		15	40	9.0	–	
Mode Control (S) to Clock		5.0	200	100	–	ns
		10	75	36	–	
		15	55	27	–	
Hold Time	t_h					ns
Data to Clock		5.0	180	90	–	
		10	50	25	–	
		15	35	10	–	
Mode Control (S) to Clock		5.0	0	-40	–	ns
		10	0	-27	–	
		15	0	-20	–	
$\overline{Reset}$ Removal Time**	t_{rem}	5.0	300	150	–	ns
		10	110	55	–	
		15	80	40	–	

*The formulas given are for the typical characteristics only.
**The reset signal must be high prior to a positive-going transition of the clock.

FIGURE 1 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



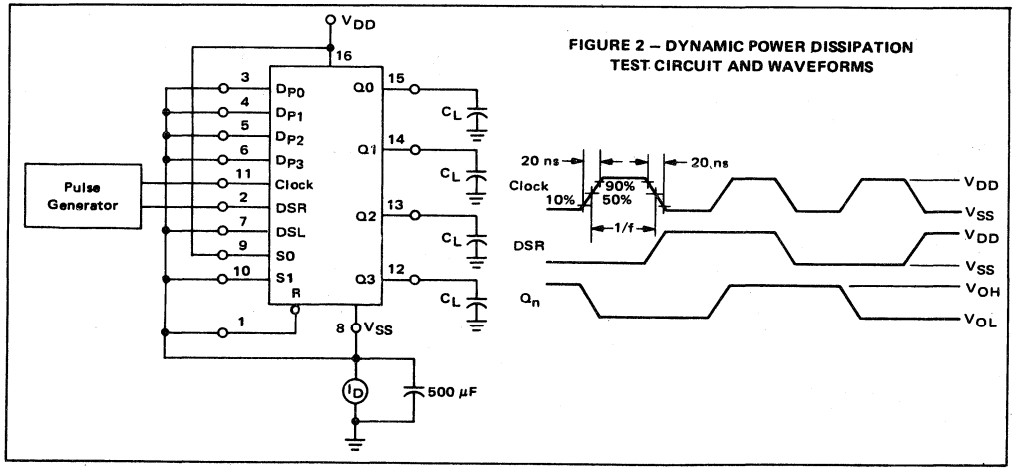


FIGURE 2 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

MOTOROLA

MC14403
MC14405

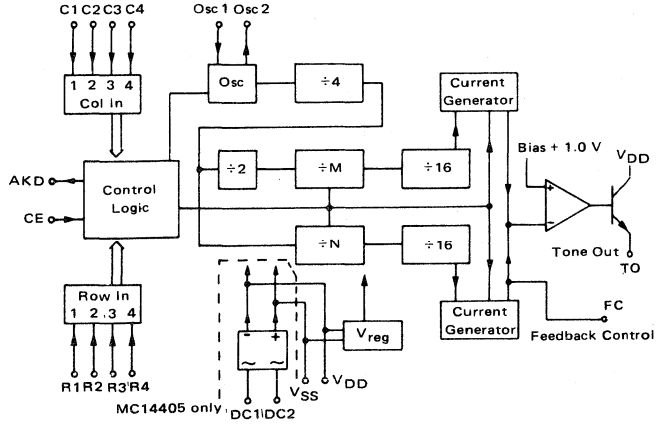
Product Preview

DUAL TONE MULTIFREQUENCY DIALER

The MC14403 and MC14405 produce audio tones according to the telephone standard 2 of 8 (DTMF) encoding. An on-chip mixer provides weighted amplitudes of high and low band signals that are generated as piecewise linear sine waves to minimize distortion. Low external parts count and use of an inexpensive 3.58 MHz crystal make these parts cost-effective in telephone instrument design, tone encoding for radio transmitters, or for use as a standard tone source for security systems and data transfer.

- 3 to 12 Volt Operation
- Uses Inexpensive 3.579545 MHz (TV Color Burst) Crystal
- Distortion Typically 2% Without Filtering
- Crystal Oscillator is Inhibited When No Key is Depressed
- Minimum Turn On and Turn Off Transients
- Amplitude Level is Selectable with External Capacitor and is Suppy Voltage Independent
- Low Standby Current
- Integrated Active Bridge Rectifier Eliminates External Diode Bridge in Telephone Applications
- Uses Standard Telephone Keyboard for Maximum Noise Immunity
- Dual Tone or Single Tone Capability
- MC14403 Similar to MK5089. Row and Column Inputs Have Pull-Up Current Sources
- MC14405 Same as MC14403 with Internal Active Bridge

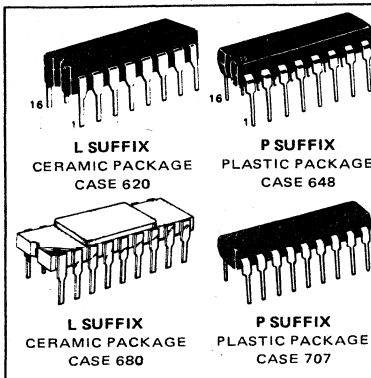
BLOCK DIAGRAM



CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

DTMF
INTEGRATED TONE DIALER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

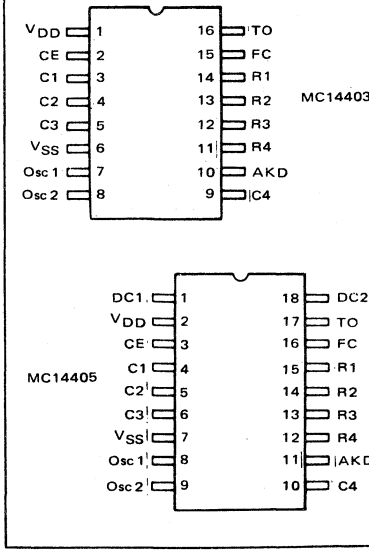
L SUFFIX
CERAMIC PACKAGE
CASE 680

P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

PIN ASSIGNMENT



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage ($V_{DD}-V_{SS}$)	V_{DD}	12	Vdc
Voltage on Any Pin	V_{in}	V_{SS} – 0.3 to V_{DD} + 0.3	Vdc
Maximum Power Dissipation	P_D	500	mW
Tone Output Current	I_{out}	20	mA
Storage Temperature Range	T_{stg}	–55 to +150	°C
Operating Temperature Range	T_A	–30 to +60	°C
MC14405 Only			
Supply Voltage Pin 1 to Pin 18	V_{DC}	12	V
Supply Current into Pin 1 or Pin 18	I_{DC}	100	mA
Voltage on Pins 1 or 18	V_{in}	V_{SS} –0.7 to V_{DD} +0.7	Vdc

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating	Unit
Supply Voltage	$V_{DD}-V_{SS}$	3.0 to 12	V
Key Sensing and $\overline{AKD}$ Operation	$V_{DD}-V_{SS}$	1.5 to 12	V

ELECTRICAL CHARACTERISTICS (T_A = 25°C Voltages Referenced to V_{SS})

Characteristic		Symbol	$V_{DD}-V_{SS}$	Min	Typ	Max	Unit
Input Voltage	Row, Column	V_{IL}	5.0	–	2.25	1.5	Vdc
			10	–	4.50	3.0	
	CE		5.0	–	–	3.0	
			10	–	–	8.0	
	Row, Column	V_{IH}	5.0	3.5	2.75	–	Vdc
			10	7.0	5.5	–	
	CE		5.0	4.0	–	–	
			10	9.0	–	–	
Output Drive Current	AKD	I_{OH}					μA
(V_O = 4.5 Vdc)			5.0	–20	–	–	
(V_O = 9.5 Vdc)			10	–80	–	–	
(V_O = 2.0 Vdc)		I_{OL}	5.0	3.0	–	–	mA
(V_O = 2.0 Vdc)			10	12	–	–	
Tone Output Before Clipping	R_L = 600 Ω	V_O	*	0.9	–	–	V_p
	R_L = 250 Ω		*	0.8	–	–	
Total Harmonic Distortion	R_L = 600 Ω	THD	*	–	2.0	–	%
Quiescent Current		I_{DD}	5.0	–	100	–	μA
(No Key Depressed)			10	–	130	–	
Total Supply Current	R_L = 1.0 kΩ	I_T	*	–	3.0	–	mA
Turn On Delay Time (Oscillator Start-Up Time)		T_D	*	–	–	10	ms
Output Voltage Active Rectifier			**DC1–DC2**				Vdc
(Output = $V_{DD}-V_{SS}$)	I_{DD} = 1 mA		3.0	–	2.9	–	
	2 mA		3.0	–	2.8	–	
	5 mA		3.0	–	2.5	–	
	1 mA		3.5	–	3.4	–	
	2 mA		3.5	–	3.3	–	
	6 mA		3.5	–	3.0	–	
	1 mA		4.0	–	3.9	–	
	5 mA		4.0	–	3.6	–	
	10 mA		4.0	–	3.3	–	
	15 mA		4.0	–	3.0	–	
	1 mA		4.5	–	4.4	–	
	10 mA		4.5	–	3.9	–	

*Independent of Supply if 3.0 Vdc < V_{DD} < 12 Vdc.

FUNCTIONAL DESCRIPTION

TONE GENERATION

The output frequencies are derived from the 3.579545 MHz crystal oscillator by integer divider ratios. The sine wave output is generated by feeding different constant currents into an integrator. At the output of this integrator, the current steps appear as variable ramps. The output amplitude is inversely proportional to the integrator capacitance between tone output and feedback input and can be adjusted by the choice of capacitor value. A 0.012 μF capacitor delivers approximately 970 mVp of composite output voltage for Key D (R4/C4).

The tone output dc component is V_{SS}, if no tone is to be generated and it is approximately V_{SS} + 1.1 V, if a tone is generated. The maximum output swing without clipping is from V_{SS} to V_{SS} + 2.2 V. An external resistor is added across the capacitor to reduce output drift. The time constant equal to the feedback capacitor times feedback resistor must be equal or larger than the longest single output period.

$R_F \geq 1/(C_F \cdot f\,Row\,1) = 120\ k\Omega$ for $C_F = 0.012\ \mu F$

KEYBOARD DEBOUNCE

The leading edge of a valid keyboard input signal will enable the oscillator. The oscillator will start up within typically 5.0 ms. If the signal bounces within these 5.0 ms, there is no effect at the tone output. After 1/16 of the period of the highest frequency to be generated following the oscillator start-up time, the keyboard signal is latched and will not be affected anymore by key bounce. It will be unlatched only during those times at which the composite tone output is within approximately 6% of its absolute minimum and, after releasing the key, continues until it is again within 6% of that minimum. In addition to debouncing the keyboard, the dc switch-on/switch-off transients are minimized.

ACTIVE BRIDGE RECTIFIER

A dc voltage of either polarity applied between DC1 and DC2 generates another dc voltage between V_{DD} and V_{SS} with V_{DD} being always positive. Because the internal bridge rectifier replaces the conventional diodes by semiconductor switches without offset voltage, but with a finite on-resistance, the voltage drop across the rectifying element is close to zero at low currents. At high currents and low dc voltages, the voltage drop across the on-resistance of the rectifying element might exceed the forward voltage drop of a diode. In those cases, the internal bridge should be paralleled with an external diode bridge in order to increase efficiency and to prevent latch-up. If the active bridge will not be used, the supply voltage should be directly applied to V_{DD} (positive) and V_{SS} (negative).

KEYBOARD LOGIC

In the quiescent state, the row and column inputs are pulled up by constant current sources. The AKD pin is normally low and goes high if any key input is activated (even an invalid combination). Thus AKD or any key down can be used for receiver muting and transmitter switching in lieu of extra common switches on the keyboard. The keyboard logic operates as follows:

a. DTMF-tone pairs will only be generated by pushing a single key.

b. Single tones can be generated by activating one row (or column) and more than one column (or row) inputs. Pushing two or more keys in a given row will generate only the common row tone and pushing two or more keys in a given column will generate only the common column tone.

c. Single tones can also be generated by activating only one row or only one column input, e.g., C1 activated.

CE (Chip Enable) is also pulled to V_{DD} with an internal current source. If CE is pulled low, the oscillator and the tone output are disabled and no tone will be generated. The AKD output is unaffected by CE.

SUPPLY VOLTAGE/CURRENT CONSIDERATIONS

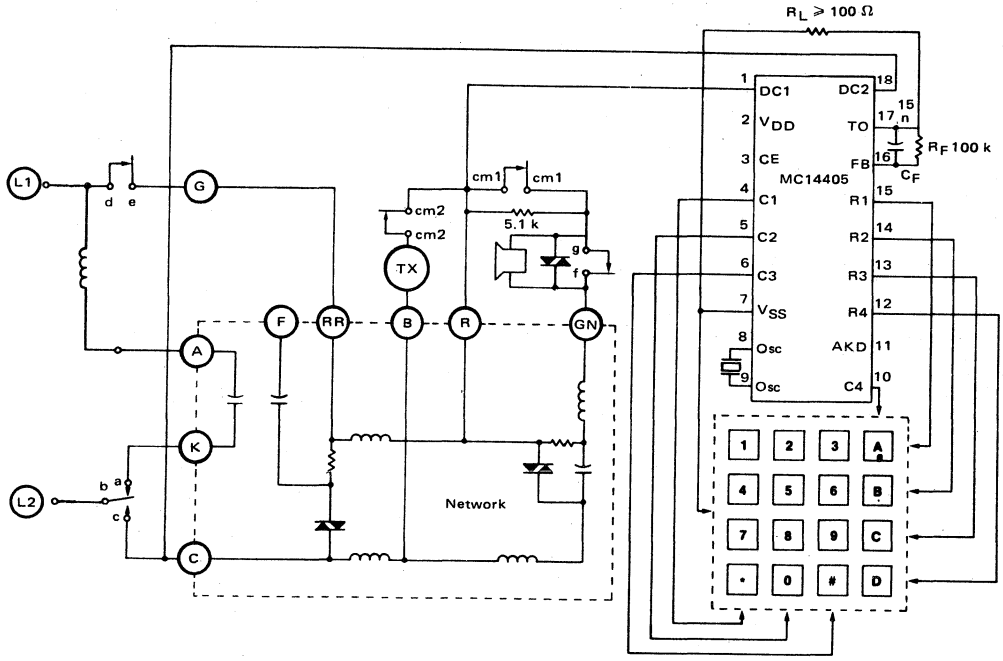
Most of the chip is operated from an internally generated 3.0 V regulated voltage that tracks the supply voltage below 3.0 V. The chip current consumption increases from 0 to 3.0 V and stays constant from 3.0 V to 12 V. The tone output ac and dc voltage is constant when the supply voltage is above 3.0 V. The chip-current consumption does not load the tone signal down by its own impedance.

FREQUENCY TABLE

Input	Nominal Hz	Actual* Hz	Deviation* %	Divider Ratio N	Relative A1/A2	Amplitude dB
R1	697	699.13	+0.3	5120	1.0	0
R2	770	766.17	−0.5	4672	1.04	0.3
R3	852	847.43	−0.5	4224	1.08	0.7
R4	941	947.97	+0.74	3776	1.12	1.0
C1	1209	1215.88	+0.57	2944	1.30	2.3
C2	1336	1331.68	−0.32	2688	1.35	2.6
C3	1477	1471.85	−0.35	2432	1.41	3.0
C4	1633	1645.01	+0.74	2176	1.46	3.3

*f_{osc} = 3,579,545 Hz, f_{actual} = Osc/N. R1 Amplitude (Volts Peak) = (4.5 ±0.4) · $10^9/C_F$ (C_F in Farads).

MC14405 APPLICATIONS SCHEMATIC



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MOTOROLA

MC14406
MC14407

Advanced Information

PULSE CODE MODULATION (PCM) CODEC

The MC14406 and MC14407 per channel PCM codecs are designed for 8000-samples-per-second, 8-bit-per-sample voice coding and decoding. These devices are full duplex and provide both Mu and A companding laws.

The transmit and receive data rates are independently selectable from 64 kHz to 3.088 MHz allowing direct interface to 24, 30, 32, and 48 channel digital frames.

Both codecs are fabricated using CMOS technology for reliable low power performance. The MC14406 is the full feature device in a 28-pin package. The MC14407 provides a 24-pin package without signaling capabilites.

- Per Channel Full Duplex Capability
- Low Power Operation – 80 mW Typ
- Power Down Input (1.0 mW Max in Power Down Mode)
- Pin Selection of A-law and Mu-law Companding (MC14407)
- Single Power Supply Operation – 10 to 16 volts
- Zero Code Suppression
- Transmit and Receive Signaling Available (MC14406)
- Independent Transmit and Receive Clocks to 3.088 MHz
- Externally Selectable Full Scale
- On-Chip Auto Zero

CMOS LSI

(LOW POWER COMPLEMENTARY MOS)

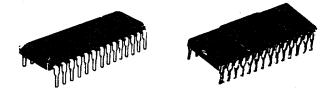
FULL DUPLEX 8-BIT COMPANDED PCM CODEC

24-PIN PACKAGE



CASE 709 – PLASTIC CASE 716 – CERAMIC

28-PIN PACKAGE

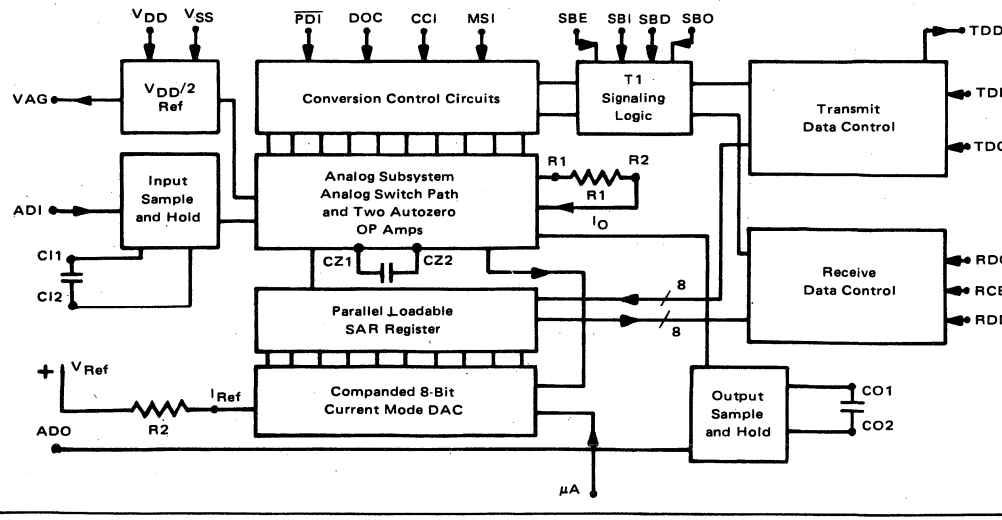


CASE 710 – PLASTIC CASE 719 – CERAMIC

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	−0.5 to +18	Vdc
Voltage, Any Pin to V_{EE}	V	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin (Excluding V_{DD})	I	10	mAdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	10	12	16	Vdc
Convert Clock Freqency	CCI	128	128	512	kHz
Transmit Data Clock Frequency	TDC	128	2048	3088	kHz
Receive Data Clock Frequency	RDC	128	2048	3088	kHz
Input Sample Capacitor	CI1, CI2	0.001	0.002	0.010	μF
Output Sample Capacitor	CO1, CO2	0.001	0.002	0.010	μF
Unit Step Size = Full Scale/4096	ADO	0.36	0.85	1.2	mV
Full Scale Voltage (V_{DD} = 15 V)	ADO	1.5	3.5	5.0	Vp
Load Bias Resistor	VAG	2.0	–	–	kΩ
Bypass Capacitor	VAG	–	0.1	–	μF
Auto Zero Capacitor	CZ1, CZ2	–	0.002	–	μF

SYSTEM PERFORMANCE A-to-D through D-to-A (R1 = 25 kΩ, R2 = 2.27 kΩ, T_A = 25°C)

Characteristic		Min	Typ	Max	Unit
Signal to Noise Ratio	+3.0 to −30 dBm	33	36	–	dB
$\frac{S+N+D}{N+D}$	−40 dBm	27	30	–	
C Message at f = 1020 Hz	−45 dBm	22	25	–	dB
Deviation from Level Linearity	+3.0 to −35 dBm	−0.5	–	+0.5	dB
	−35 to −45 dBm	−0.10	–	+1.0	dB
Idle Channel Noise (ADI = VAG)		–	0	12	dBmC
Quiet Code		–	–	–	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DIGITAL ELECTRICAL CHARACTERISTICS

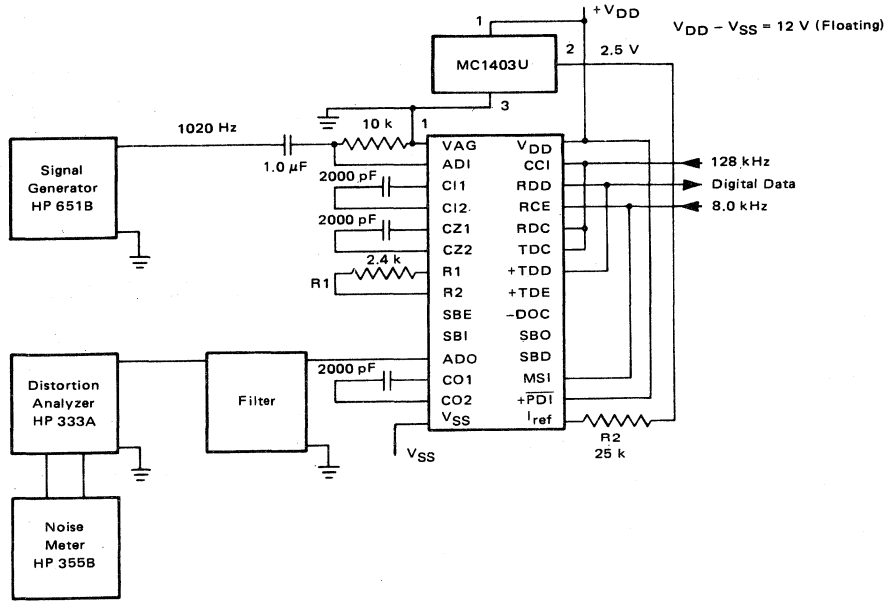
Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Operating Current (R2 = 25 k)	I	12	–	–	–	8.0	–	–	–	mA
Power-Down Current ($\overline{PDI}$ = V_{SS})	I_{PD}	12	–	–	–	30	80	–	–	μA
Input Current										
CCI, RDD, RCE, RDC, TDC, $\overline{PDI}$	I_{in}	12	–	–	–	±0.00001	±0.3	–	–	μA
DOC, SBD, MSI, SBI, SBE	I_{inS}		–	–	–	+30	–	–	–	
(Internal Pull-Down Resistors)	I_{inD}		–	–	–	-0.00001	-0.3	–	–	
TDE, Mu/A-Law	I_{inS}		–	–	–	+0.00001	+0.3	–	–	
(Internal Pull-Up Resistors)	I_{inD}		–	–	–	-30	–	–	–	
Input Voltage "0" Level	V_{IL}	12	–	–	–	5.25	3.60	–	–	V
		15	–	–	–	6.75	4.0	–	–	
"1" Level	V_{IH}	12	–	–	8.4	6.75	–	–	–	V
		15	–	–	11	8.25	–	–	–	
Input Capacitance	C_{in}	12	–	–	–	5.0	7.5	–	–	pF
Output Drive Current SBO										
V_{OH} = 11	I_{OH}	12	–	–	-2.0	-4.0	–	–	–	mA
V_{OH} = 13.5		15	–	–	-3.0	-8.8	–	–	–	
V_{OL} = 1.0	I_{OL}	12	–	–	2.0	4.0	–	–	–	mA
V_{OL} = 1.5		15	–	–	3.0	8.8	–	–	–	
Output Drive Current TDD										
V_{OH} = 11	I_{OH}	12	–	–	-4.0	-8.0	–	–	–	mA
V_{OH} = 13.5		15	–	–	-6.0	-17.6	–	–	–	
V_{OL} = 1.0	I_{OL}	12	–	–	4.0	8.0	–	–	–	mA
V_{OL} = 15		15	–	–	6.0	17.6	–	–	–	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V)

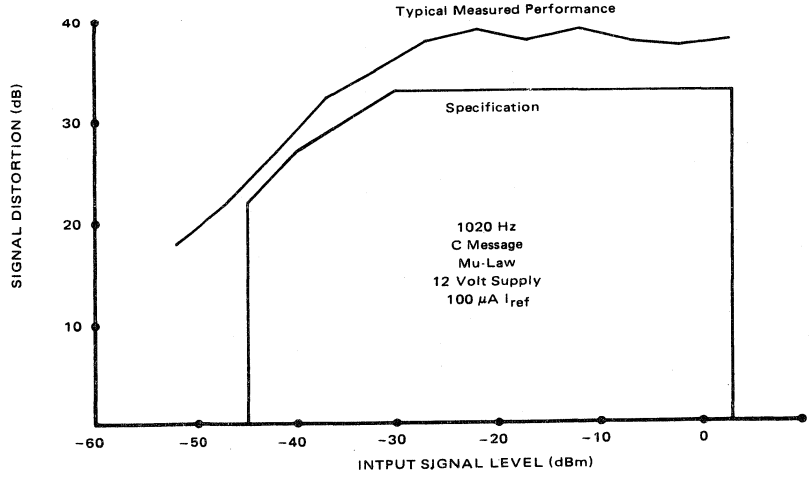
Characteristic	Pin	-40°C Min	-40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Analog Ground Voltage	VAG	–	–	6.0	6.05	6.1	–	–	V
Source Current		–	–	–	200	–	–	–	μA
Sink Current		–	–	–	5.0	–	–	–	mA
Output Impedance		–	–	–	50	–	–	–	Ω
Reference Input Current	I_{ref}	–	–	50	100	200	–	–	μA
Input Offset Voltage		–	–	–	±10	+25	–	–	mV
Offset Voltage Drift		–	–	–	30	100	–	–	μV/°C
Input Impedance dc	ADI	–	–	1.0	10	–	–	–	MΩ
AC (Ω) CI = 0.002 nF, 1 kHz		–	–	–	80	–	–	–	kΩ
Lower Common Mode Ring		–	–	–	2.0	2.5	–	–	V
Upper Common Mode Ring		–	–	9.5	10	–	–	–	V
Sample Duty Cycle	ADO	–	–	–	3/16	–	–	–	–
Neutral Duty Cycle		–	–	–	13/16	–	–	–	–
Neutral Offset (From VAG)		–	–	-25	±25	+25	–	–	mV
Neutral Offset Drift		–	–	–	30	100	–	–	μV/°C
Source Current		–	–	–	200	–	–	–	mA
Sink Current		–	–	–	5.0	–	–	–	mA
Lower Common Mode Ring		–	–	–	2.0	2.5	–	–	V
Upper Common Mode Ring		–	–	9.5	10	–	–	–	V
Output Impedance		–	–	–	100	–	–	–	Ω
Settling Time to 3.0 V R and F		–	–	–	0.3	–	–	–	μs

TEST CIRCUIT

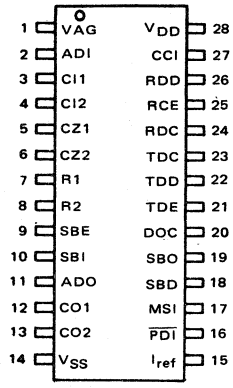
MC14406 NOISE PERFORMANCE DATA

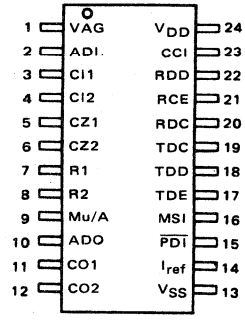


NOISE PERFORMANCE OF MC14406



PIN DESCRIPTION





VAG – Analog Ground Output (V_{DD}–V_{SS})/2. VAG is the output of the internal (V_{DD}–V_{SS})/2 voltage reference. A pull-up load resistor and bypass capacitor may be required if this output is to be used elsewhere in the system. This pin serves as the analog ground.

ADI – Analog Data Input. The band-limiting input filter between the channel unit hybrid and the codec drive pin 2. Driver source impedance should be 600 Ω or less. This is the voice input to the codec and will be sampled at 8.0 kHz.

CI1, CI2 – Input Sample Capacitor. The input sample capacitor is connected to these pins. A 2000 pF silver mica capacitor is recommended.

CZ1, CZ2 – Auto Zero Capacitor. The auto zero circuit requires a 2000 pF capacitor between these pins.

R1, R2 – Gain Resistor. The V-to-I conversion resistor is connected between these pins. Gain is established by the ratio of this resistor and the resistor at pin I_{ref}.

Mu/A – Mu-Law/A-Law Select (Internal Pull-Up). Selection of Mu-law or A-law coding is provided for logic control. An internal pull-up provides Mu-law output. An external connection to V_{SS} provides A-law operation.

SBE – Signal Bit Enable (Internal Pull-Down). SBE controls the insertion of transmit signaling bits into the transmit data register. When taken high, the next transmit word will contain the SBI pin level in the LSB position rather than the last bit of the PCM word. If kept high, the SBI data will be inserted in succeeding conversions until one conversion after it is brought low. It can be used for on-hook signaling or A and B signaling in D3 banks.

SBI – Signal Bit Input (Internal Pull-Down). SBI is the data input for transmitting signaling bits. The level of SBI will be latched on the leading edge of SBE, or by the internal latch data pulse if SBE is held high. If SBE is pulsed, the leading edge of SBE will latch SBI, and load it into the next transmit word.

ADO – Analog Data Output. ADO outputs the received PAM sample for three convert clock cycles beginning with MSI. It then returns to the output neutral voltage which may be a few millivolts different from VAG1.

CO1, CO2 – Output Sample Capacitor. The output sample capacitor is connected between these pins. A silver mica capacitor of 2000 pF is recommended.

V_{SS} – Most Negative Supply. This is the most negative supply pin, and the digital ground. All digital inputs and outputs will swing the full supply voltage.

I_{ref} – Current Reference Input. A reference current of 50 to 200 μA sets the full scale DAC current. An 80 μA input current corresponds to 1.28 mA full scale DAC current at pin R2.

$\overline{PDI}$ – Power-Down Input. $\overline{PDI}$ deactivates the codec when pulsed to V_{SS}. In the power-down mode the analog circuitry bias is turned off and the digital clock inputs are disabled. Power-down dissipation is less than 1.0 mW.

MSI – Master Sync Input (Internal Pull-Down). The MSI leading edge resets the entire chip to the initial cycle (0000). The chip continues operation on the next leading edge of data and convert clock. MSI also resets the output data multiplexer to the transmit word sign bit.

SBO – Signal Bit Output. SBO outputs the LSB of the receive data register. The LSB may be sampled externally during the first three convert clocks after MSI or used as a trigger pulse in off-hook applications.

SBD – Signal Bit Decode (Internal Pull-Up). Signal bit decode allows the control of the 1/2 LSB or LSB centering required in sample decode cycles. It is loaded by the RCE edge in each cycle. If a zero is entered, the next decode cycle adds 1/2 LSB to the 8-bit received word to center the quantization error of the 8-bit received sample when the output sample capacitor is charged. If a 1 is loaded by RCE, the 1/2 LSB is not added, and the LSB is forced to

a 1 to form a centered error 7-bit output, and the LSB is ignored and assumed to be signaling information. (For codes 1111111X or 0111111X, the LSB is disabled for SBD high.)

DOC — Decode Only Control (Internal Pull-Down). DOC is normally tied low. When high, it configures the device to skip the eight convert clocks used for A-to-D conversion. The operating cycle is then two clocks for PAM output at ADO and six clocks for charging the next output sample. The device may be used to do as many as four decode cycles in a 125 μs/period with an external transmission gate selector.

Received Data is loaded into the transmit data register at MSI when in DOC mode, so DOC can be used as a digital loop back control.

TDE — Transmit Data Enable (Internal Pull-Up). The Transmit Data Enable is a three-state control for the transmit digital output. A number of codec outputs can be interleaved into a serial stream by connecting the outputs and controlling TDE with a 1-of-N decoder. It will provide switching characteristics capable of 3.088 MHz operation.

TDD — Transmit Digital Data. The Transmit Digital Data rate is controlled by the data clock input, and is frame aligned with the Master Sync Input. If data clock is at 1.544 MHz, and convert clock is at 128 kHz, the new sign bit will be output beginning with the leading edge of convert clock 8, and the 8-bit word repeated throughout the convert cycle at the data clock rate. The data word is inverted offset binary with zero code suppression. See Conversion and Data Timing.

TDC — Transmit Data Clock. TDC sets the digital data rate of the codec. The transmit data stream will provide a continuous repetition of the current transmit data word at the TDC bit rate, beginning with MSB first and synchronized with the last MSI. The new data word is loaded and serially output at mid-cycle or on the leading edge of convert clock 8.

RDC — Receive Data Clock. RDC controls the receive data register. It clocks the receive-data register on the trailing edge under the control RCE. It is often connected to TDC.

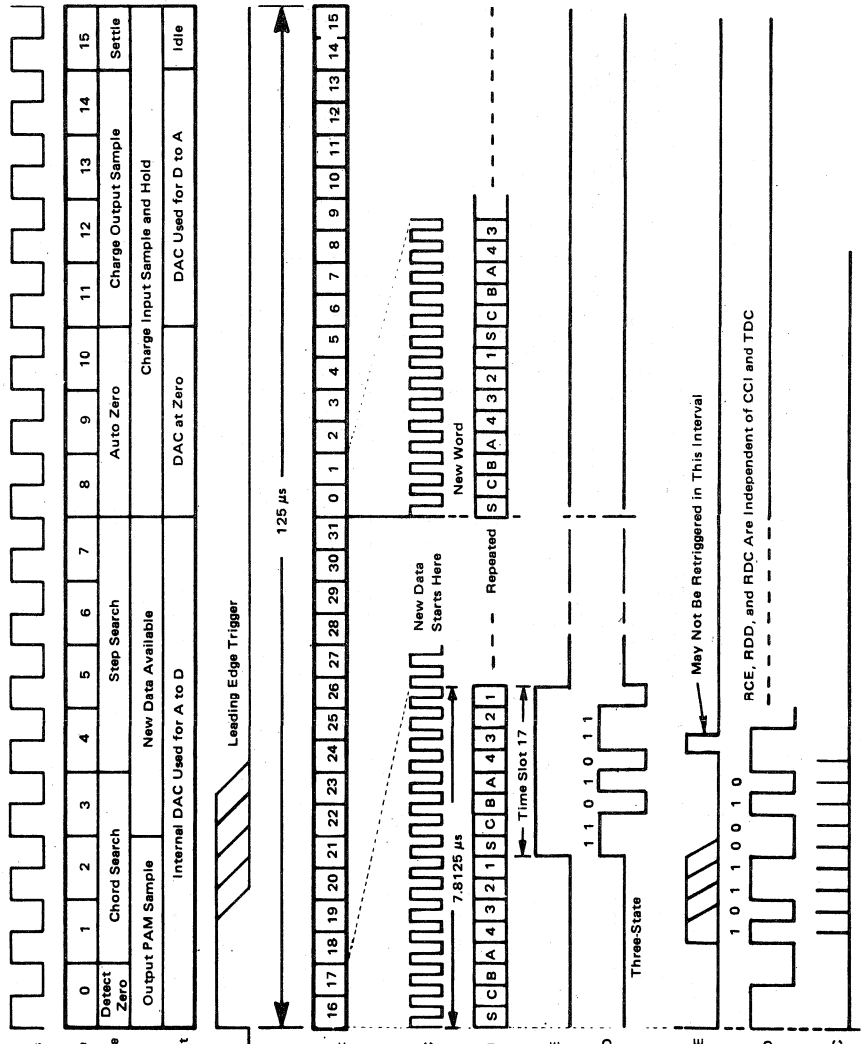
RCE — Receive Clock Enable. The rising edge of RCE triggers the receive data register to accept a new data input. After the rising edge of RCE, the data on RDD is loaded into the Receive Data Register on the next eight trailing edges of RDC. The ninth clock transfers the new 8-bit word to an internal intermediate register and frees the Receive Data Register for a new RCE.

RDD — Receive Digital Data. RDD is the input to the receive data shift register. It is controlled by RCE. The register is clocked on the trailing edge of RDC. The data format is sign bit first, inverted offset binary code.

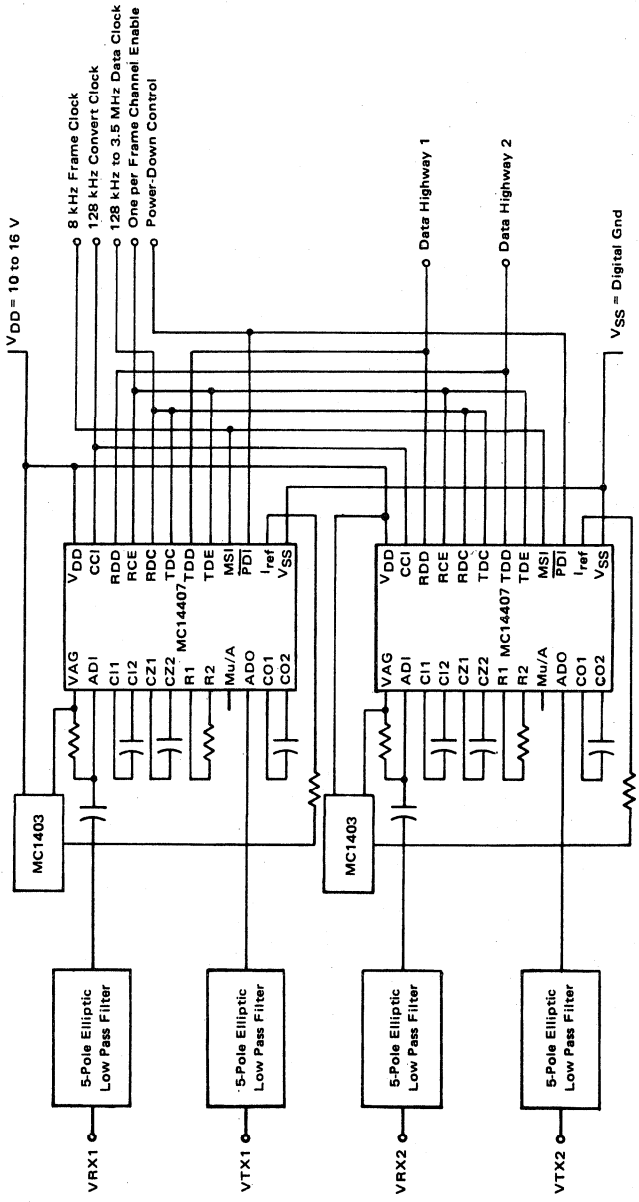
CCI — Convert Clock Input. CCI controls the conversion sequence. A 128 kHz clock will produce 64K-bits/s full duplex operation and a 256K-bits/s clock will produce 64K-bit operation for two channels. Sixteen clocks represent one chip cycle from MSI to MSI.

V_{DD} — Most Positive Supply. V_{DD} is typically 12 V with an operation range of 10 V to 16 V. All logic outputs swing the full supply voltage.

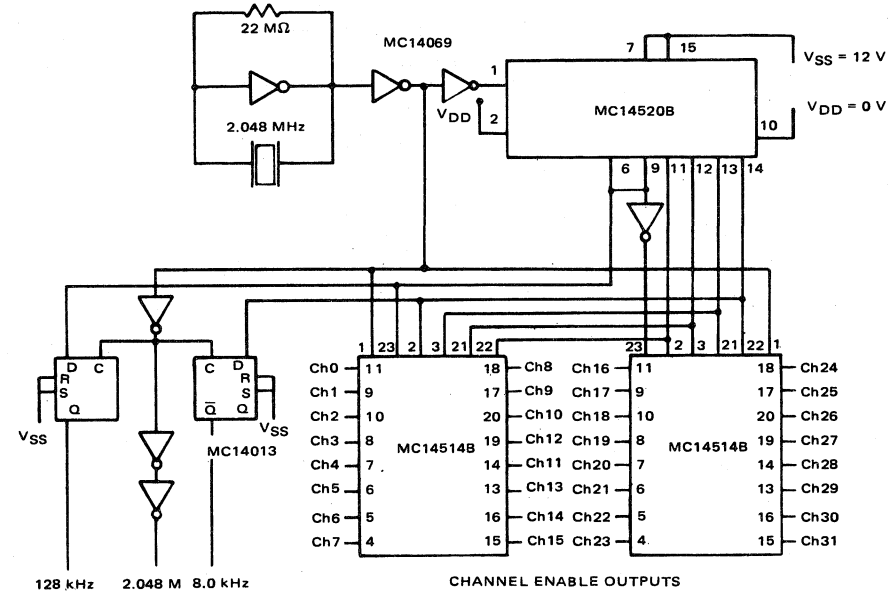
CONVERSION AND DATA TIMING FOR 64K BIT CHANNEL IN 2.048 MEGABIT FRAME

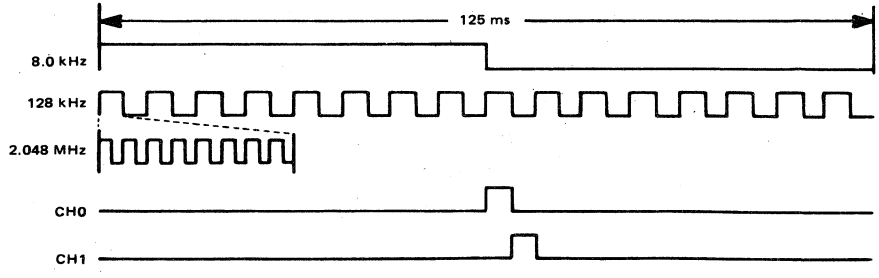


TYPICAL DIGITAL SWITCHING APPLICATION OF MC14407

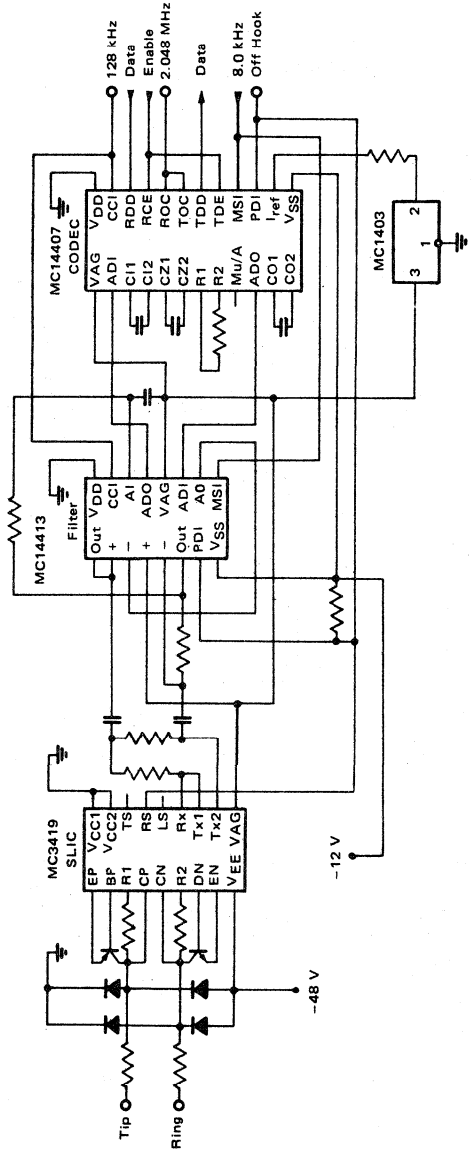


TYPICAL CMOS COMMON CLOCK GENERATOR





PROPOSED MOTOROLA 3-CHIP SUBSCRIBER CHANNEL UNIT



MOTOROLA

MC14408
MC14409

BINARY TO PHONE PULSE CONVERTER SUBSYSTEM

The MC14408 and the MC14409 are devices designed to convert a four bit binary input code to a number of serial output pulses corresponding to the value of the input code.

The devices can be used in telephone pulse dialing applications when combined with their companion device, the MC14419 (2-of-8 keypad-to-binary code converter). The devices have been partitioned to allow convenient addition of RAM memory and controls for repertoire dialing applications.

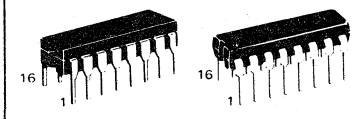
The MC14408 and MC14409 perform identical functions with the exception of the signal output at the DRO (Dial Rotating Output). In the MC14408, DRO remains high during continuous outpulsing of all digits and in the MC14409 DRO is low between each digit pulse burst.

- On-Chip Oscillator
- Diode Protection on All Inputs
- Dialing of Numbers Up to 16 Digits Long
- Memory Storage (FIFO) and Re-Dialing (single pin) of Last Telephone Number
- Hold Interrupt Control for Additional Interdigit Delays (such as a Wait for Intermediate Dial Tones)
- Selectable Dialing Rate (10 pps or 20 pps)
- Selectable Interdigit Time (300 or 800 ms @ 10 pps; 150 or 400 ms @ 20 pps)
- Selectable Make-Break Ratio (61% or 67%)
- Buffered Outputs Compatible with Discrete Transistor Driver Interface, One Low-power Schottky TTL Load or Two Low-power TTL Loads Over the Rated Temperature Range.
- Low Power Dissipation – I_{DD} (operating with oscillator) = 470 μA typ @ V_{DD} = 5.0 Vdc, f_{Osc} = 16 kHz, C_L = 50 pF

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

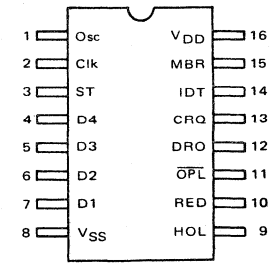
BINARY TO PHONE PULSE CONVERTER SUBSYSTEM



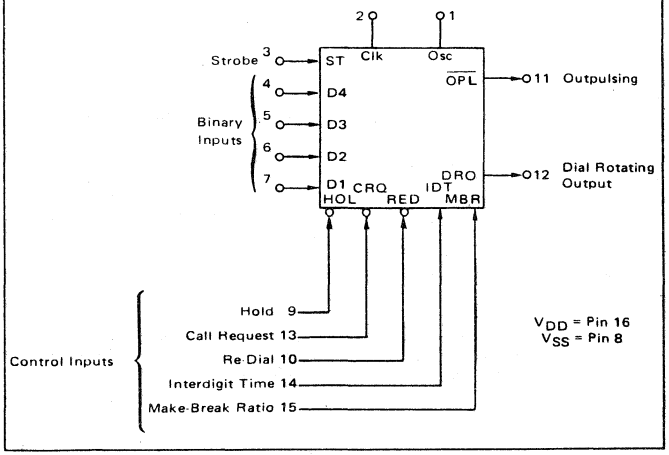
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	3.0	6.0	3.0	5.0	6.0	3.0	6.0	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Noise Immunity										
($\Delta V_{out} \leq 0.5$ Vdc)	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	Vdc
($\Delta V_{out} \leq 0.5$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.80	-1.7	–	-0.60	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.20	–	-0.16	-0.36	–	-0.12	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
Input Current	I_{in}	6.0	–	–	–	±0.00001	±0.30	–	1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	12	–	5.0	12	–	12	pF
Operating Supply Current	I_{DD}	3	–	250	–	160	200	–	200	μAdc
f_{cl} = 16 kHz (operating		5	–	700	–	470	550	–	550	
with Osc)		6	–	1250	–	740	1000	–	1000	

FIGURE 1 – TIMING DIAGRAM – DATA AND STROBE INPUTS

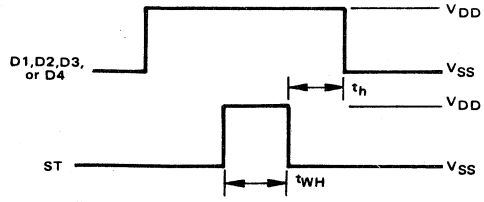
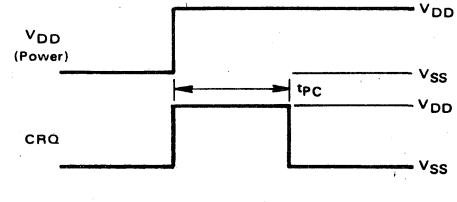


FIGURE 2 – TIMING DIAGRAM – CALL REQUEST



If power is turned off after each call, CRQ must stay high after power is applied (for a duration of t_{PC}) to ensure no spurious outpulsing. For this use the redial function is invalid.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time** t_{TLH} = (3.0 ns/pF) C_L + 30 ns	t_{TLH}	5.0	–	180	400	ns
Output Fall Time** t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	ns
Power Up to Call Request Pause	t_{PC}	3 to 6	48/f_{cl}*	–	–	ms
Call Request to First Strobe Pulse	t_{CS}	3 to 6	48/f_{cl}*	–	–	ms
Strobe to Strobe Separation Time	t_{SS}	3 to 6	48/f_{cl}*	–	–	ms
Strobe Pulse Width	t_{WH}	3 to 6	1.0	–	–	μs
Strobe to Data Hold Time	t_h	3 to 5	–	150	400	ns
Clock Frequency	f_{cl}	3 to 6	12.5	16	100	kHz
Percent Break to Make Ratio	%MB	3 to 6				%
(MBR = 0)			–	61	–	
(MBR = 1)			–	67	–	
Outpulsing Rate (f_{OPL} = *f_{cl}/1.6)	f_{OPL}	3 to 6				pps
f_{cl} = 16 kHz			–	10	–	
f_{cl} = 32 kHz			–	20	–	
Interdigit Time	t_{ID}	3 to 6				ms
t_{ID} = (5 x IDT + 3)/f_{OPL}						
IDT = 0						
f_{OPL} = 10 pps			–	300	–	
f_{OPL} = 20 pps			–	150	–	
IDT = 1						
f_{OPL} = 10 pps			–	800	–	
f_{OPL} = 20 pps			–	400	–	
Strobe to Output Time	t_{SOI}	3 to 6				ms
Initial Outpulsing Stream						
IDT = 0						
f_{OPL} = 10 pps			300	–	400	
f_{OPL} = 20 pps			150	–	200	
IDT = 1						
f_{OPL} = 10 pps			800	–	900	
f_{OPL} = 20 pps			400	–	450	
Continued Outpulsing Stream	t_{SOC}	3 to 6				ms
IDT = 0 or 1						
f_{OPL} = 10 pps			100	–	200	
f_{OPL} = 20 pps			50	–	100	
Hold to Outpulse Time	t_{HOL}	3 to 6				ms
IDT = 0 or 1						
f_{OPL} = 10 pps			100	–	200	
f_{OPL} = 20 pps			50	–	100	
Dial Rotating Overlap Time	t_{DRO}	3 to 6				ms
f_{OPL} = 10 pps			–	100	–	
f_{OPL} = 20 pps			–	50	–	

*f_{cl} in kHz

**The formula given is for the typical characteristics only.

DEVICE OPERATION

OSCILLATOR (Osc, Pin 1)

This pin is an input to the internal oscillator and feedback connection for the L-C π-network. An external clock signal, if desired can be applied to Osc.

CLOCK (Clk, Pin 2)

This pin is an output from the internal oscillator and feedback connection for the L-C π-network and provides the system clock for the MC14419 bounce eliminator circuitry.

STROBE INPUT (ST, Pin 3)

This Strobe input, when high (ST = V_{DD}), signifies that the data at the D1, D2, D3, and D4 inputs is valid, and enters the 4-bit number into the internal FIFO (First-In, First-Out) memory for subsequent outpulsing. The first strobe pulse after a call is requested (CRQ = low) clears the memory of any previous number and enters the first digit of the new number. Successive strobe pulses will store up to a maximum of 16 digits in the internal FIFO memory, which ignores all digits entered in excess of that amount until a new call is requested.

DATA INPUTS (D4, D3, D2, D1, Pins 4, 5, 6, 7)

These pins are the Data inputs to the internal memory. A binary coded digit number entered will result in an equivalent number of pulses at the $\overline{OPL}$ (outpulsing) output, except for the code 0000, which will outpulse 10 pulses.

NEGATIVE POWER SUPPLY (V_{SS}, Pin 8)

This pin is the negative power supply connection. Normally this pin is system ground.

HOLD (HOL, Pin 9)

When taken low (HOL = V_{SS}), the Hold input disables the outpulsing at the completion of the digit being outpulsed. When taken high, outpulsing resumes. This feature can be used in multi-dial-tone phone systems to provide longer interdigit pauses when necessary.

RE-DIAL (RED, Pin 10)

The Re-Dial input, when taken low (RED = V_{SS}) automatically outpulses the digits entered into memory after the last time a call was requested.

OUTPULSING ($\overline{OPL}$, Pin 11)

The Outpulsing output sends out bursts of pulses equivalent to the digits of the telephone number stored in the memory. The duty cycle and interdigit time of the digit pulse bursts are controlled, respectively by the MBR (Pin 15) and IDT (Pin 14).

DIAL ROTATING OUTPUT (DRO, Pin 12)

The Dial Rotating (also known as "Off Normal") Output provides a signal which indicates that digit pulse bursts are being sent. In the MC14409, DRO goes high (V_{DD}) at the beginning of the first digit pulse burst and goes low (V_{SS}) between succeeding consecutive digit pulse bursts. In the MC14408, however, DRO goes high at the beginning of the first digit pulse burst and remains high until the last digit pulse burst of the telephone number has been sent (see Timing Diagram, Figure 3).

CALL REQUEST (CRQ, Pin 13)

The Call Request input when taken low (CRQ = V_{SS}) resets internal counters and prepares the internal logic to either accept new digit inputs to be dialed, or to re-dial (see RED, Pin 10) the digits stored in the memory.

INTERDIGIT TIME (IDT, Pin 14)

The Interdigit Timing input determines the length of time between consecutive digit pulse bursts. See the Interdigit Time (t_{ID}) in the switching characteristics for the length of time.

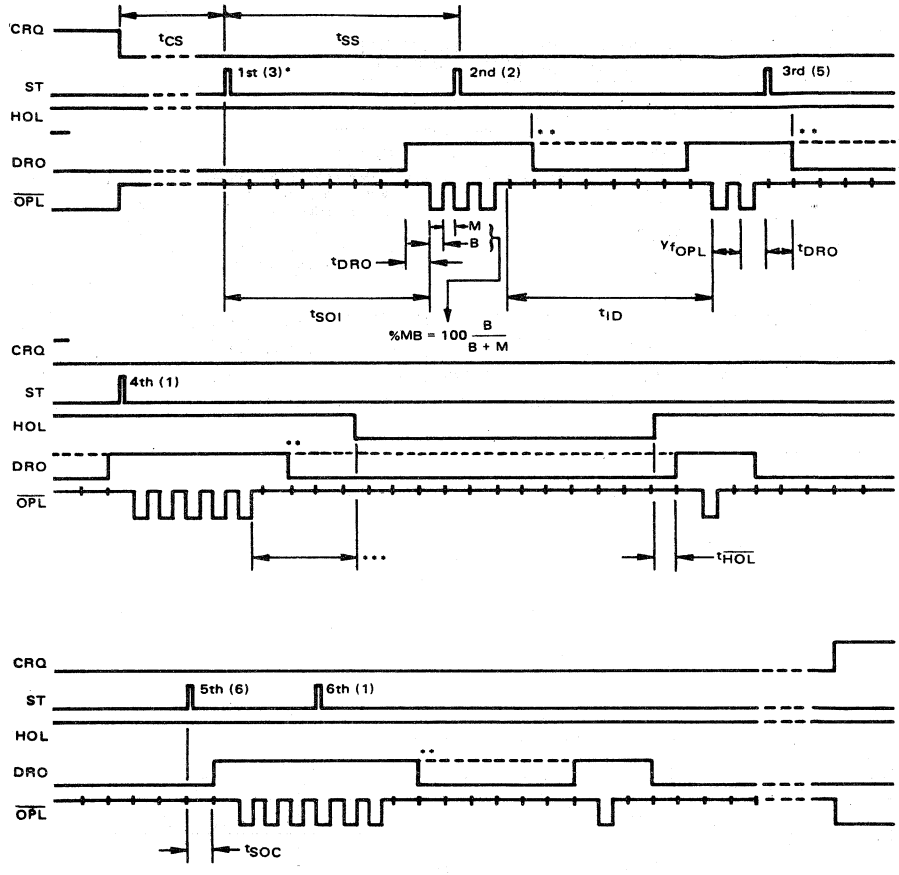
MAKE-BREAK RATIO (MBR, Pin 15)

The Make-to-Break Ratio input controls the duty cycle of the digit pulse bursts at the $\overline{OPL}$ output. For MBR = V_{DD}, duty cycle = 67% low, 33% high; and for MBR = V_{SS}, duty cycle = 61% low, 39% high.

POSITIVE POWER SUPPLY (V_{DD}, Pin 16)

This pin is the package positive power supply pin.

FIGURE 3 – PHONE DIALER SYSTEM TIMING DIAGRAM



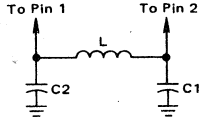
Notes:

(*)1st, 2nd, 3rd, etc., denotes Strobe pulse sequence – i.e., which digit in the phone number is being dialed. The number in parentheses denotes the numerical value of the digit being dialed. The examples define the various voltage – level and timing requirements, not a complete phone number.

(**)For the MC14408 the DRO signal will remain high provided digits remain in the memory, or a digit for continuing outpulsing is strobed in before the anticipated falling edge of the most significant digit in the memory. (i.e., [200 % MB] ms after the most significant outpulsing edge).

(***)For the HOL signal to hold a next digit (e.g. the 4th, etc.,) the HOL falling edge must not appear after [t_{ID}-%MB + 100] ms the last outpulsing edge of the previous digit.

FIGURE 4 – COMPONENT SELECTION FOR OSCILLATOR/CLOCK FREQUENCY



$$f_{cl} = \frac{7.118}{\sqrt{LC}}$$ where f_{cl} in kHz, L in mH, C = C1 = C2 in μF

$\%f_{cl} = -0.5\,[\%C + \%L] \pm 3.0$ where $\%f_{cl}$, %C, %L are the frequency capacitor, and inductor tolerances in percent. The ±3.0% accounts for supply voltage and ambient temperature variations.

EXAMPLE

L	%L	C=C1=C2	%C	f_{cl}	$\%f_{cl}$	OUTPULSING RATE $f_{OPL} = f_{cl}/1.6$
5.0 mH	±5.0	0.04 μF	±5.0	≈16 kHz	±8.0	≈10 pps
5.0 mH	±5.0	0.01 μF	±5.0	≈32 kHz	±8.0	≈20 pps

FIGURE 5 – TRUTH TABLE

INPUTS							OUTPUTS	
$\overline{CRO}$	D4 D3 D2 D1	ST	$\overline{RED}$	$\overline{HOL}$	IDT	MBR	$\overline{OPL}$	DRO †
1	X X X X	X	X	X	X	X	0	0
0	X X X X	0	1	1	X	X	1 (Steady State)	0 (Steady State)
0	X X X X (nth Digit)	⊓	1	1	X	X	Number of pulses (⊔) of nth digit = binary combination of D4, D3, D2, D1. *	1 During outpulsing 0 Otherwise
0	X X X X	0	⊔	1	X	X	Digits of number in memory re-sent.	1 During outpulsing 0 Otherwise
0	X X X X	X	1	0	X	X	1 { After conclusion of digit being outpulsed.	0 { After conclusion of digit being outpulsed
X	X X X X	X	X	X	0 1	X	300 ms Interdigit time 800 ms Interdigit time { f_{cl} ÷ 16 kHz	
X	X X X X	X	X	X	X	0 1	61% (≈1.6:1) Make-Break Ratio 67% (≈2:1) Make-Break Ratio	

X = Don't Care

With the exception of 0000 which will give 10 pulses.

† Refer to timing diagram Figure 3.

FIGURE 6– KEYPAD TO PULSE DIALER FLOW DIAGRAM

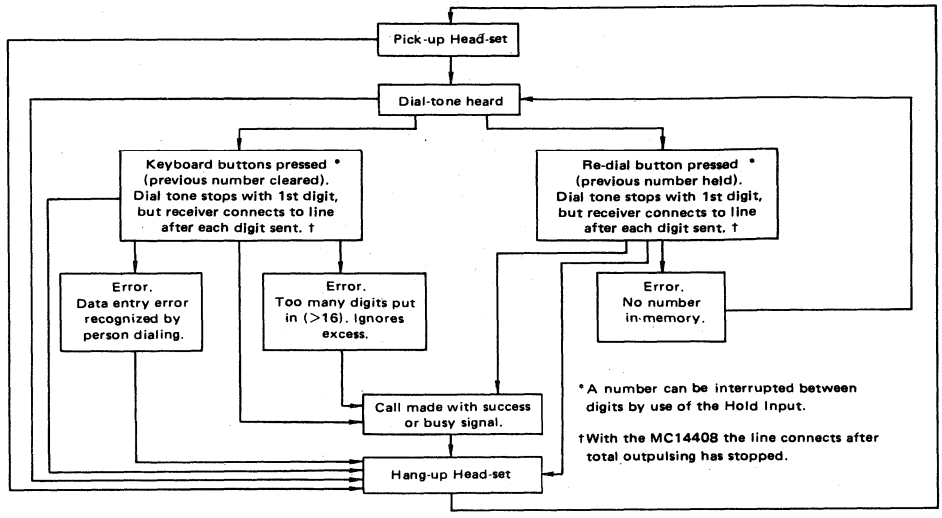
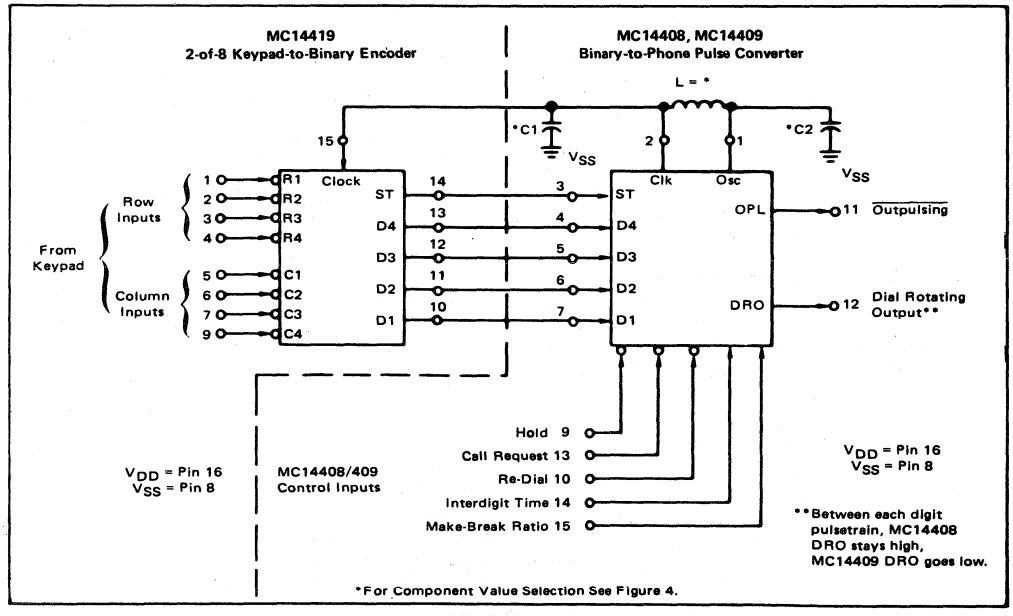


FIGURE 7– PHONE DIALER SYSTEM



Circuit diagrams utilizing Motorola products are incuded as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

FIGURE 8 – STANDARD K-500 TELEPHONE

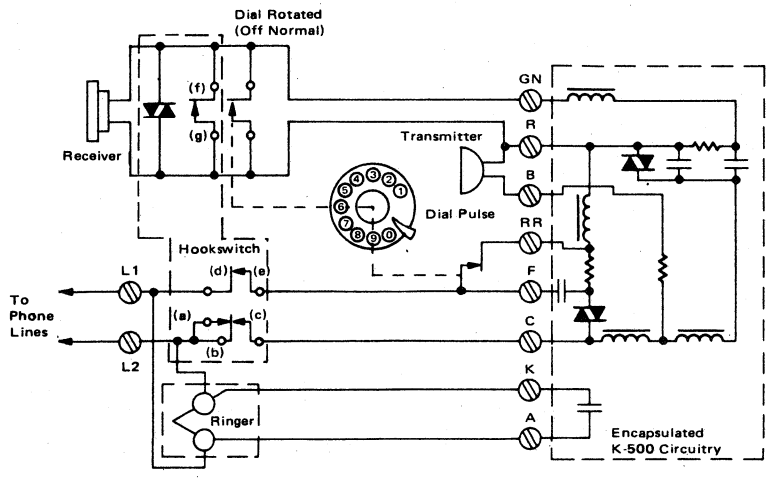
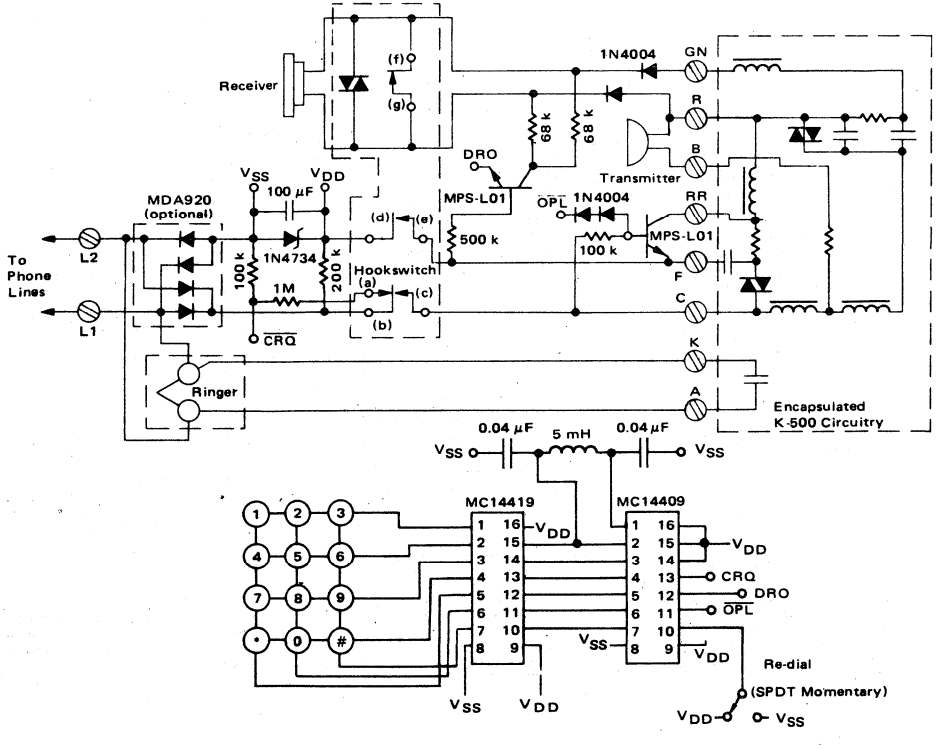


FIGURE 9 – MODIFIED K-500 TELEPHONE



MOTOROLA

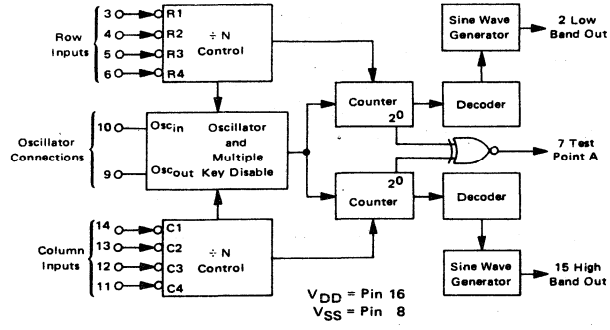
MC14410

2-OF-8 TONE ENCODER

The MC14410 2-of-8 tone encoder is constructed with complementary MOS enhancement mode devices. It is designed to accept digital inputs in a 2-of-8 code format and to digitally synthesize the high and low band sine waves specified by telephone tone dialing systems. The inputs are normally originated from a 4 x 4 matrix keypad, which generates 4 row and 4 column input signals in a 2-of-8 code format (1 row and 1 column are simultaneously connected to V_{SS}). The master clocking for the MC14410 is achieved from a crystal controlled oscillator which is included on the chip. Internal clocks, which operate the logic, are enabled only by one or more row and column signals being activated simultaneously. The two sine wave outputs have NPN bipolar structures on the same substrate which allows for low output impedance and large source currents. Applications of this device include telephone tone dialing, radio and mobile telephones, process control, point-of-sale terminals, and credit card verification terminals.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Supply Voltage Range = 4.4 Vdc to 6.0 Vdc
- On-Chip Oscillator (Crystal or External Clock Source may be applied to Pin 10)
- On-Chip Pull-Up Resistors on Row and Column Inputs
- Designed with Multiple Key Lockout (Eliminates Need for Mechanical Lockout in Keypad)
- Two Sine Wave Generators On-Chip
- Frequency Accuracy ±0.2%
- Low Harmonic Distortion
- Single Tone Capability
- Fast Oscillator Turn-On and Turn-Off Times

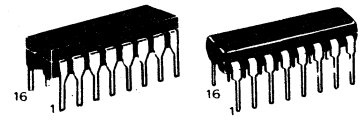
BLOCK DIAGRAM



CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

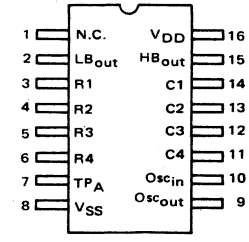
2-OF-8 TONE ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a peak sinewave voltage.

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	V_{SS} -0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	4.4	6.0	4.4	5.0	6.0	4.4	6.0	Vdc
Output Voltage "0" Level Pins 7 and 9	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) "0" Level	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 0.5 or 4.5 Vdc) "1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}									mAdc
Pin 7		5.0	-0.05	–	-0.05	-0.4	–	-0.04	–	
Pin 9			-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}									mAdc
Pin 7		5.0	0.05	–	0.05	0.20	–	0.04	–	
Pin 9			0.23	–	0.20	0.78	–	0.16	–	
Input Pull-Up Resistor Source Current (V_{in} = 0 Vdc) Pins 3-6, 11-14	I_{IL}	6.0	–	140	–	30	100	–	80	μAdc
Input Capacitance (V_{in} = 0 Vdc)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Current	I_Q									mAdc
		4.4	–	0.48	–	0.2	0.4	–	0.33	
		6.0	–	1.3	–	0.55	1.1	–	0.9	
Total Supply Current (Dynamic plus Quiescent)	I_T									mAdc
(R_L = 15 kΩ, f = 1 MHz)		4.4	–	1.7	–	0.7	1.4	–	1.15	
		6.0	–	3.5	–	1.45	2.9	–	2.4	
Low Band Output Voltage Swing Pin 2 Only	V_{Lpp}									mVpp
		4.4	400	600	500	600	700	550	750	
		6.0	800	1000	900	1000	1100	950	1150	
High Band Output Voltage Swing Pin 15 Only	V_{Hpp}									mVpp
		4.4	600	900	700	850	1000	800	1100	
		6.0	1100	1400	1200	1350	1500	1300	1600	
Low Band–High Band Voltage Differential	ΔV	5.0	–	–	–	2.5	–	–	–	dB
Low Band–High Band Output Impedance Pin 2,15	z_o	–	–	–	–	80	–	–	–	Ω
Low Band–High Band Pin 2,15 2nd thru 14th Harmonics (R_L = 15 kΩ)	V_{2H}-V_{14H}	4.4 to 6.0	–	-20	–	-30	-25	–	-25	dB
Maximum Clock Pulse Frequency	f_{cl}	4.4	–	–	–	1.0	–	1.1	–	MHz
Turn-on Time (Power on to oscillation)	t_{on}	5.0	–	–	–	8.0	–	–	–	ms

TABLE 1 – FUNCTIONAL TRUTH TABLE

ACTIVE LOW INPUTS		OUTPUTS	
Activated Row Lines	Activated Column Lines	Low Band Pin 2	High Band Pin 15
None	X**	dc level	dc level
X**	None	dc level	dc level
One	One	f_L*	f_H*
Two or more	One	dc level	f_H*
One	Two or more	f_L*	dc level
Two or more	Two or more	dc level	dc level

*See Table 2
**X = Don't care

TABLE 2 – OUTPUT FREQUENCY TABLE

Input Line Activated (low)	Frequency Generated**	
	f_L (Hz)	f_H (Hz)
R1	697	–
R2	770	–
R3	852	–
R4	941	–
C1	–	1209
C2	–	1336
C3	–	1477
C4	–	1633

**All frequencies are accurate to ±0.2% (crystal tolerance not included).

FIGURE 1 – TYPICAL SINE WAVE OUTPUT
(Pins 2 or 15, No External Filtering)

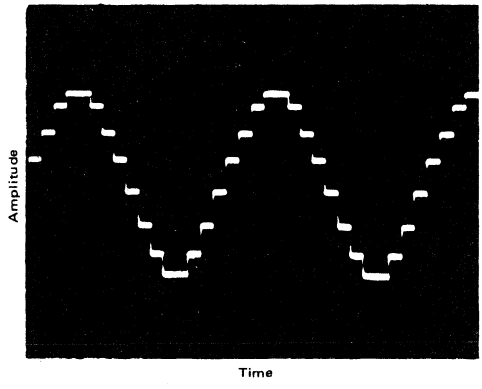


FIGURE 2 – TYPICAL FREQUENCY SPECTRUM
(Pins 2 or 15, No External Filtering)

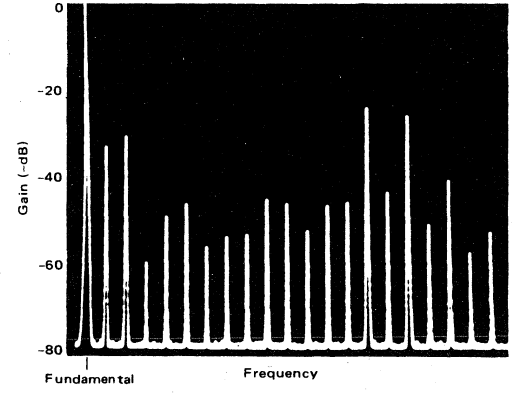


FIGURE 3 – TYPICAL CRYSTAL CIRCUIT

R_f = 15 MΩ ± 10%

CRYSTAL SPECIFICATION

Crystal Mode	Parallel
Frequency	1 MHz ± 0.1%
R_S	540Ω typ
C_0	7.0 pF typ
Temperature Range	-40°C to +85°C
Test Level	1 mW
Test Set	TS–330/TSM or Equivalent

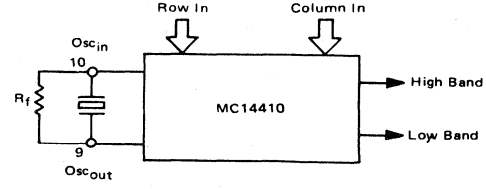


FIGURE 4 – TYPICAL TELEPHONE INTERFACE APPLICATION

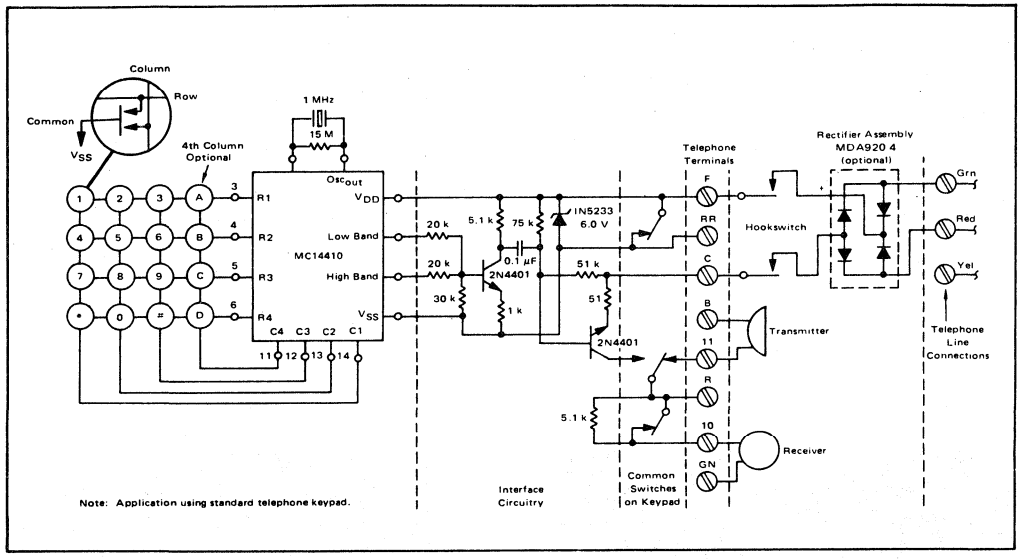


FIGURE 5 – LOW LEVEL OUTPUT TONE GENERATOR APPLICATION

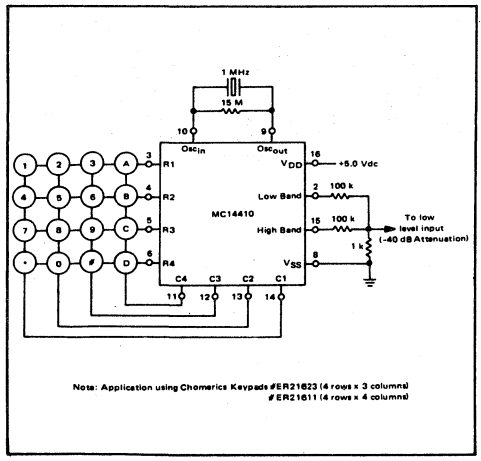
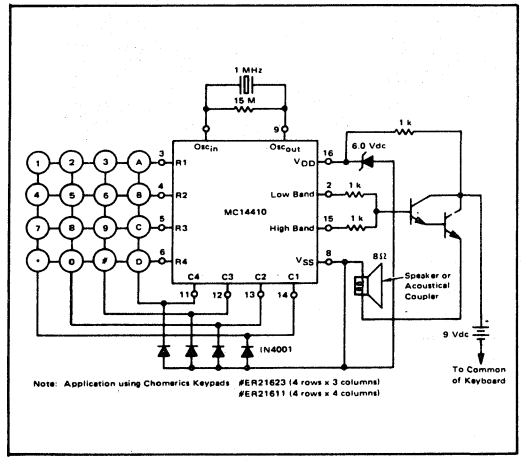


FIGURE 6 – BATTERY POWERED OPERATION (Driving Audio Speaker)



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14411

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

BIT RATE GENERATOR

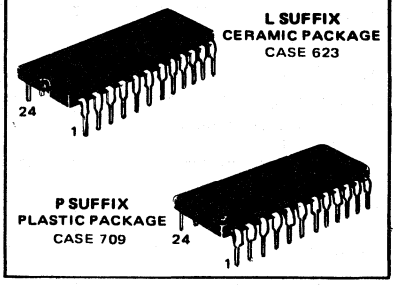
BIT RATE GENERATOR

The MC14411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

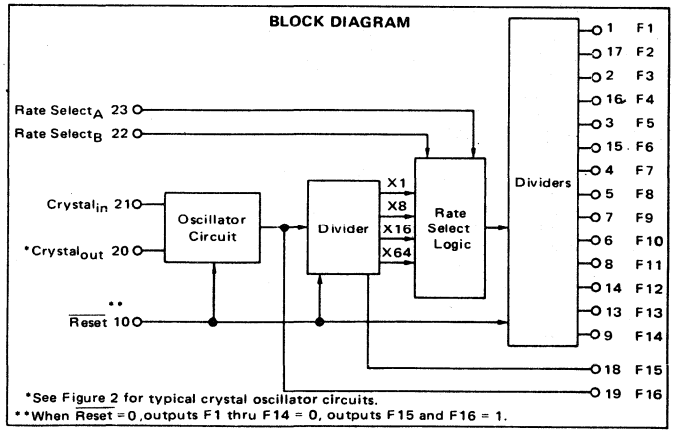
- Single 5.0 Vdc (± 5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (1.8432 MHz)
- Sixteen Different Output Clock Rates
- 50% Output Duty Cycle
- Programmable Time Bases for One of Four Multiple Output Rates
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock May be Applied to Pin 21



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12.)

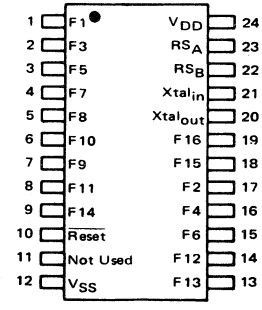
Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	5.25 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



*See Figure 2 for typical crystal oscillator circuits.
**When $\overline{Reset}$ = 0, outputs F1 thru F14 = 0, outputs F15 and F16 = 1.

PIN ASSIGNMENT



V_{DD} = Pin 24
V_{SS} = Pin 12

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	4.75	5.25	4.75	5.0	5.25	4.75	5.25	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
Output Voltage "1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
Input Voltage (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	mAdc
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
Input Current	I_{in}	–	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q	5.0	–	2.5	–	0.015	2.5	–	15	mW
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	(P_D = (7.5 mW/MHz) f + P_Q							mW
Output Rise Time** t_{TLH} = (3.0 ns/pF) C_L + 25 ns	t_{TLH}	5.0	–	–	–	70	200	–	–	ns
Output Fall Time** t_{THL} = (1.5 ns/pF) C_L + 47 ns	t_{THL}	5.0	–	–	–	70	200	–	–	ns
Input Clock Frequency	f_{CL}	5.0	–	1.85	–	–	1.85	–	1.85	MHz

† For dissipation at different external load capacitance (C_L) refer to corresponding formula:

$P_T(C_L) = P_D + 2.6 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$

where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

**The formula given is for the typical characteristics only.

TABLE 1 – OUTPUT CLOCK RATES

Rate Select B	Rate Select A	Rate
0	0	X1
0	1	X8
1	0	X16
1	1	X64

Output Number	Output Rates (Hz) X64	X16	X8	X1
F1	614.4 k	153.6 k	76.8 k	9600
F2	460.8 k	115.2 k	57.6 k	7200
F3	307.2 k	76.8 k	38.4 k	4800
F4	230.4 k	57.6 k	28.8 k	3600
F5	153.6 k	38.4 k	19.2 k	2400
F6	115.2 k	28.8 k	14.4 k	1800
F7	76.8 k	19.2 k	9600	1200
F8	38.4 k	9600	4800	600
F9	19.2 k	4800	2400	300
F10	12.8 k	3200	1600	200
F11	9600	2400	1200	150
F12	8613.2	2153.3	1076.6	134.5
F13	7035.5	1758.8	879.4	109.9
F14	4800	1200	600	75
F15	921.6 k	921.6 k	921.6 k	921.6 k
F16*	1.843M	1.843M	1.843M	1.843M

*F16 is buffered oscillator output.

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS

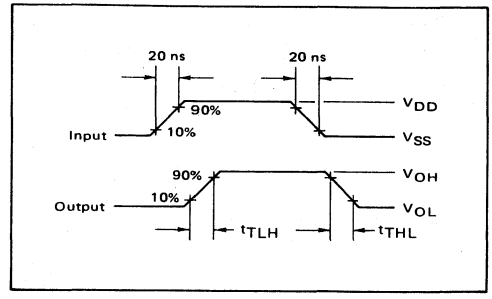
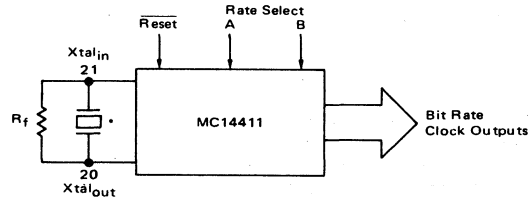


FIGURE 2 – TYPICAL CRYSTAL OSCILLATOR CIRCUIT



R_f = 15 MΩ±10%

CRYSTAL SPECIFICATION

Crystal Mode	Parallel
Frequency	1.8432 MHz ±0.05% @ 13 pF
R_S	540 Ω max
C_0	7.0 pF max
Temperature Range	0 to 70°C
Test Level	1 mW
Test Set	TS – 330/TSM or Equivalent

*Suggested Crystal Suppliers:
Tyco CTS Knights
Motorola Crystal Products

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MOTOROLA

MC14412

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

UNIVERSAL LOW SPEED
(0-600 bps)
MODEM

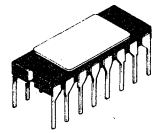
UNIVERSAL LOW SPEED MODEM (0–600 bps)

The MC14412 contains a complete FSK (Frequency-Shift Keying) modulator and demodulator compatible with both foreign (C.C.I.T.T. standards) and U.S.A. low speed (0 to 600 (bps) communication networks.

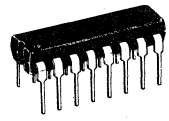
- On Chip Crystal Oscillator
- Echo Suppressor Disable Tone Generator
- Originate and Answer Modes
- Simplex, Half-Duplex, and Full Duplex Operation
- On Chip Sine Wave Generator
- Modem Self Test Mode
- Single Supply: V_{DD} = 4.75 to 15 Vdc MC14412FP, MC14412FL
  V_{DD} = 4.75 to 6.0 Vdc MC14412VP, MC14412VL
- Selectable Data Rates: 0-200, 0-300, 0-600 bps
- Post Detection Filter
- TTL or CMOS Compatible Inputs and Outputs

TYPICAL APPLICATIONS:

- Stand Alone Low-Speed Modems
- Built-In Low Speed Modems
- Remote Terminals, Acoustical Couplers
- Credit Verification
- Point of Sale
- Remote Data Collection
- Remote Process Control
- Radio Data Transmission



L SUFFIX
CERAMIC PACKAGE
CASE 690



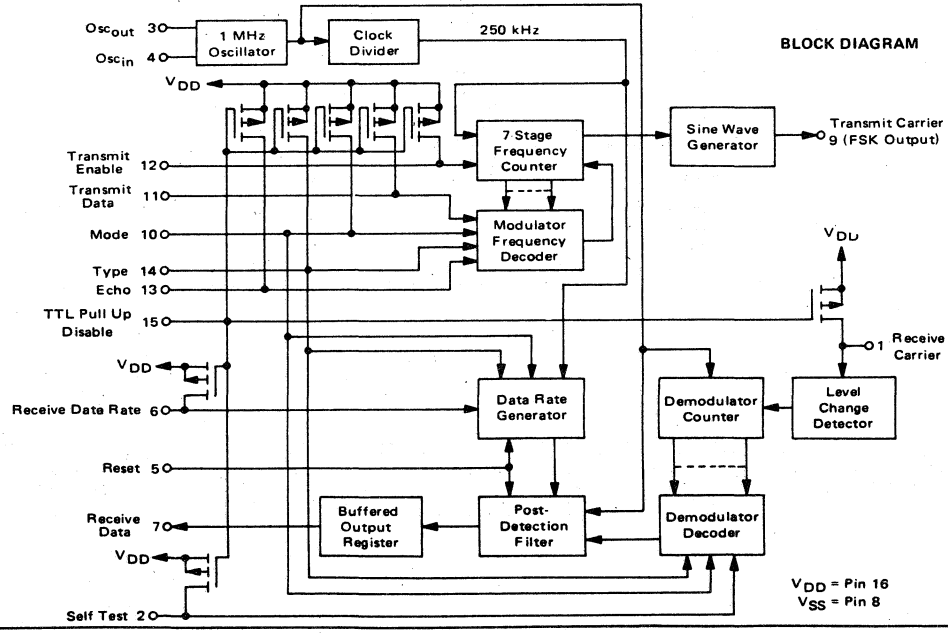
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC144XX

Suffix	Denotes
L	Ceramic Package
P	Plastic Package
F	4.75 to 15 Vdc
V	4.75 to 6.0 Vdc

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltages MC14412FP MC14412VP	V_{DD}	-0.5 to 15 -0.5 to 6.0	Vdc
Input Voltages, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin (except Pin 8, 7)	I	10	mAdc
DC Current Drain (Pin 8, 7)	I	35	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}** Vdc	−40°C Min	−40°C Max	+24°C Min	+24°C Typ	+24°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage* "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Pin 15 Δ from V_{DD}		5 to 15	0.75	–	0.8	2.0	–	0.85	–	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5) (Pin 7)		5	−0.62	–	−0.5	−1.5	–	−0.35	–	
(V_{OH} = 9.5)		10	−0.62	–	−0.5	−1.0	–	−0.35	–	
(V_{OH} = 13.5)		15	−1.8	–	−1.5	−3.6	–	−1.1	–	
(V_{OL} = 0.4)	I_{OL}	4.75	2.3	–	2.0	4.0	–	1.6	–	mAdc
(V_{OL} = 0.5)		10	5.3	–	4.5	10	–	3.6	–	
(V_{OL} = 1.5)		15	15	–	13	35	–	10	–	
Input Current (Pin 15 = V_{DD})	I_{in}	–	–	–	–	±0.00001	±0.1	–	–	μAdc
Input Pull-Up Resistor Source Current (Pin 15 = V_{SS}, V_{in} = 2.4 Vdc) Pins 1,2,5,6,10,11,12,13,14	I_P	5	285	–	250	460	–	205	–	μAdc
Input Capacitance	C_{in}	–	–	–	–	5.0	–	–	–	pF
Total Supply Current (Pin 15 = V_{DD})	I_T	5	–	4.5	–	1.1	4.0	–	3.5	mAdc
		10	–	13	–	4.0	12	–	11	
		15	–	27	–	8.0	25	–	23	
Modulator/Demodulator Frequency Accuracy (Excluding Crystal)	ACC	5 to 15	–	–	–	0.5	–	–	–	%
Transmit Carrier Output 2nd Harmonic	V_{2H}	5 to 10	–	–	-20	-26	–	–	–	dB
		10 to 15	–	–	-25	-32	–	–	–	
Transmit Carrier Output Voltage (R_L = 100 kΩ) (Pin 9)	V_{out}	5	–	–	0.2	0.30	–	–	–	V_{RMS}
		10	–	–	0.5	0.85	–	–	–	
		15	–	–	1.0	1.5	–	–	–	
Receive Carrier Rise and Fall Times (Pin 1)	t_{TLH}, t_{THL}	5	–	15	–	–	15	–	15	μs
		10	–	5.0	–	–	5.0	–	5.0	
		15	–	4.0	–	–	4.0	–	4.0	

*DC Noise Immunity (V_{IL}, V_{IH}) is defined as the maximum voltage change from an ideal "0" or "1" input level, that the curcuit will withstand before accepting an erroneous input.

**Note: Only 5-Volt specifications apply to MC14412VP devices.

PIN ASSIGNMENT

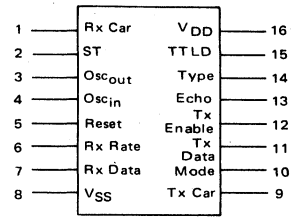


FIGURE 1 – TYPICAL LOW-SPEED MODEM APPLICATION

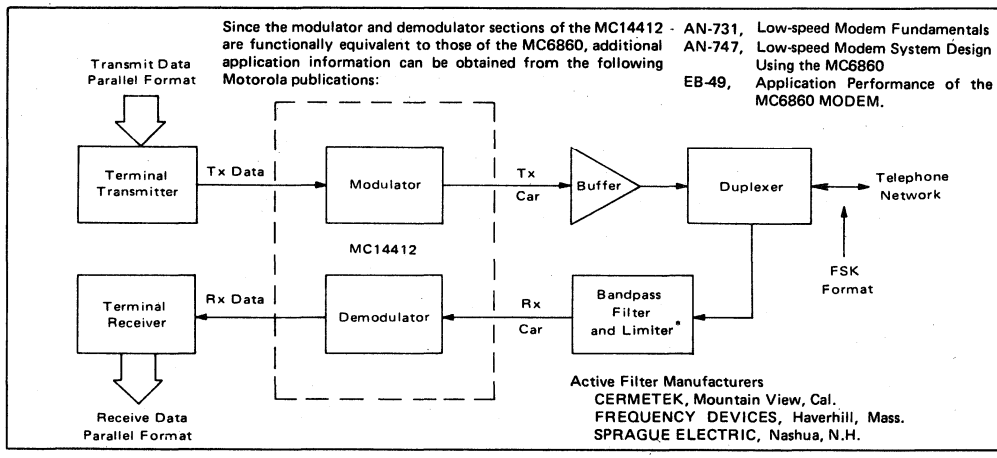
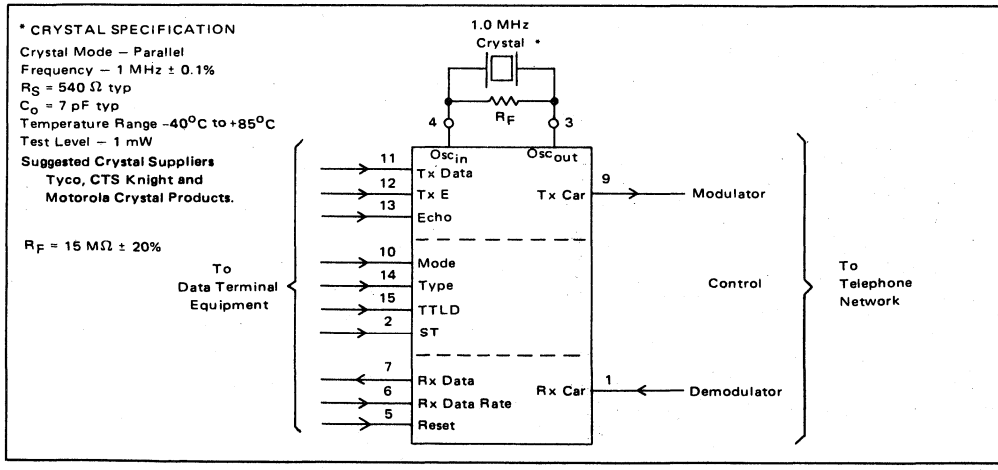


FIGURE 2 – MC14412 INPUT/OUTPUT SIGNALS



DEVICE OPERATION (continued)

RESET (Pin 5)

This input is provided to decrease the test time of the chip. In normal operation, this input may be used to disable the demodulator (Reset = "1") – otherwise it should be tied low = "0".

CRYSTAL (Osc_{in}, Osc_{out}, Pin 4, Pin 3, respectively)

A 1.0 MHz crystal is required to utilize the on chip oscillator. A 1.0 MHz square wave clock can also be applied to the Osc_{in} input to satisfy the clock requirement (see Figure 2).

When utilizing the 1.0 MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be < 9 pF at the crystal input (pin 4).

TTL PULL-UP DISABLE (TTLD, Pin 15)

To improve TTL interface compatibility, all of the inputs to the MODEM have controllable P-Channel devices which act as pull-up resistors when TTLD input is low ("0"). When the input is taken high ("1") the pull-up is disabled, thus reducing power dissipation when interfacing with CMOS.

FIGURE 3 – M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

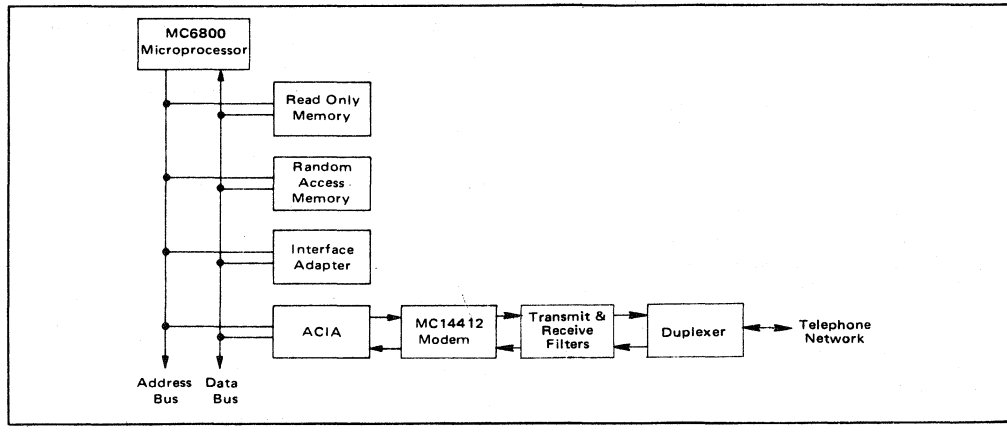


FIGURE 4 – TRANSMIT CARRIER SINEWAVE

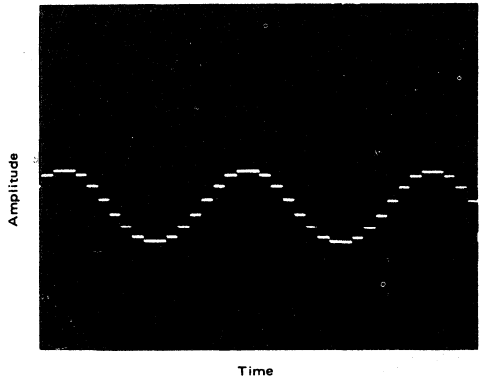
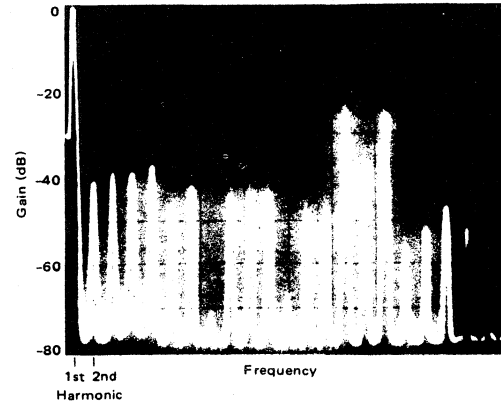


FIGURE 5 – TYPICAL TRANSMIT CARRIER FREQUENCY SPECTRUM



DEVICE OPERATION

GENERAL

Figure 1 shows the modem in a system application. The data to be transmitted is presented in serial format to the modulator for conversion to FSK signals for transmission over the telephone network. The modulator output is buffered/amplified before driving the 600 ohm telephone line.

The FSK signal from the remote modem is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal. The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

INPUT/OUTPUT FUNCTIONS

Figure 2 shows the I/O interface for the MC14412 low-speed modem. The following is a description of each individual signal.

TYPE (Pin 14)

The Type input selects either the U.S. or C.C.I.T.T. operational frequencies for both transmitting and receiving data. When the Type input = "1", the U.S. standard is selected and when the Type input = "0", the C.C.I.T.T. standard is selected.

TRANSMIT DATA (Tx Data, Pin 11)

Transmit Data is the binary information input. Data entered for transmission is modulated using FSK techniques. When operating in the U.S. standard (Type = "1") a logic "1" input level represents a Mark or when operating in the CCITT standard (Type = "0") a logic "1" input level represents a Mark.

TRANSMIT CARRIER (Tx Car, Pin 9)

The Transmit Carrier is a digital-synthesized sine wave derived from a 1.0 MHz oscillator reference. The frequency characteristics are as follows:

United States Standard Transmit Frequencies — Type = "1", Echo = "0"

Mode		Tx Data		Tx Car
Originate	"1"	Mark	"1"	1270 Hz
Originate	"1"	Space	"0"	1070 Hz
Answer	"0"	Mark	"1"	2225 Hz
Answer	"0"	Space	"0"	2025 Hz

C.C.I.T.T. Standard Transmit Frequencies — Type = "0", Echo = "0"

Mode		Tx Data		Tx Car
Channel	"1"	Mark	"1"	980 Hz
No. 1	"1"	Space	"0"	1180 Hz
Channel	"0"	Mark	"1"	1650 Hz
No. 2	"0"	Space	"0"	1850 Hz

Echo Suppressor Disable Tone — Type = "0", Echo = "1"

Mode	Tx Data	Tx Car
Chan. No. 2 "0"	"1"	2100 Hz

TRANSMIT ENABLE (Tx Enable, Pin 12)

The Transmit Carrier output is enabled when the Tx Enable input = "1". No output tone can be transmitted when Tx Enable = "0"

MODE (Pin 10)

The Mode input selects the pair of transmitting and receive frequencies used during modulation and demodulation. When Mode = "1", the U.S. originate mode is selected (Type input = "1") or the C.C.I.T.T. Channel No. 1 (Type input = "0"). When mode = "0", the U.S. answer mode is selected (Type input = "1") or the C.C.I.T.T. Channel No. 2 (Type input = "0").

ECHO (Pin 13)

When the Echo input = "1" (Type = "0", Mode = "0", Tx Data = "1") the modulator will transmit a 2100 Hz tone for disabling line echo suppressors. During normal data transmission, this input should be low = "0".

RECEIVE DATA (Rx Data, Pin 7)

The Receive Data output is the digital data resulting from demodulating the Receive Carrier.

RECEIVE CARRIER (Rx Car, Pin 1)

The Receive Carrier is the FSK input to the demodulator. This input must have either a CMOS or TTL compatible logic level input (see TTL pull-up disable) at a duty cycle of 50% ± 4%, that is a square wave resulting from a signal limiter.

RECEIVE DATA RATE (Rx Rate, Pin 6)

The demodulator has been optimized for signal to noise performance at 200, 300, and 600 bps. The Receive Carrier must change frequency for more than half of the selected data rate period before the Receive Data output will change.

Data Rate	Rx Rate	Type
0 - 200 bps	"1"	"0"
0 - 300 bps	"1"	"1"
0 - 600 bps	"0"	"1"

SELF TEST (ST, Pin 2)

When a high level (ST = "1") is placed on this input, the demodulator is switched to the modulator frequency.

MOTOROLA

MC14415

QUAD PRECISION TIMER/DRIVER

The MC14415 quad timer/driver is constructed with complementary MOS enhancement mode devices. The output pulse width of each digital timer is a function of the input clock frequency. Once the proper input sequence is detected the output buffer is set (turned on), and after 100 clock pulses are counted, the output buffer is reset (turned off).

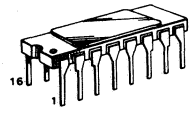
The MC14415 was designed specifically for application in high speed line printers to provide the critical timing of the hammer drivers, but may be used in many applications requiring precision pulse widths.

- Four Precision Digital Time Delays
- Schmitt Trigger Clock Conditioning
- NPN Bipolar Output Drivers
- Timing Disable Capability Using Inhibit Output
- Positive or Negative Edge Strobing on the Inputs
- Synchronous Polynomial Counters Used for Delay Counting
- Power Supply Operating Range
  = 3.0 Vdc to 18 Vdc (MC14415EFL/FL/FP)
  = 3.0 Vdc to 6.0 Vdc (MC14415EVL/VL/VP)

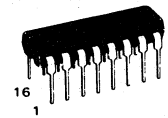
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD PRECISION TIMER/DRIVER



L SUFFIX
CERAMIC PACKAGE
CASE 690

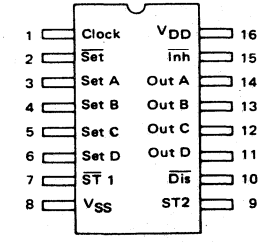


P SUFFIX
PLASTIC PACKAGE
CASE 648

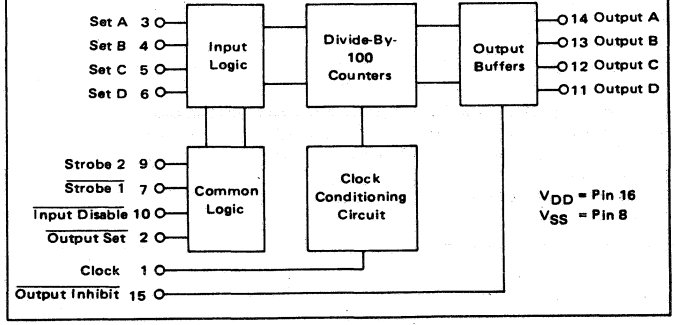
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage – MC14415EFL/FL/FP – MC14415EVL/VL/VP	V_{DD}	 +18 to -0.5 +6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Input Pin	I_{in}	10	mAdc
DC Current Drain per Output Pin	I_{out}	20	mAdc
Operating Temperature Range – MC14415EFL/EVL – MC14415FL/FP/VL/VP	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

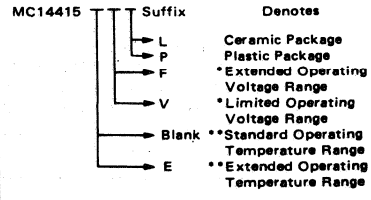
PIN ASSIGNMENT



BLOCK DIAGRAM



ORDERING INFORMATION



*See Features (above, left)
**See Maximum Ratings

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage (No Load)	"0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	–	–	–	–	
	"1" Level		5.0	–	–	3.0	4.14	–	–	–	Vdc
			10	–	–	8.0	9.09	–	–	–	
			15	–	–	–	14.12	–	–	–	
Noise Immunity		V_{NL}									Vdc
($\triangle V_{out} \leq$ 1.5 Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 3.0 Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 4.5 Vdc)			15	–	–	–	6.75	–	–	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 3.0 Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 4.5 Vdc)			15	–	–	–	6.75	–	–	–	
Output Drive Voltage (NPN Driver)		V_{OH}									Vdc
(I_{OH} = 0 mA)	Source		5.0	–	–	3.0	4.14	–	–	–	
(I_{OH} = 5.0 mA)				–	–	2.7	3.44	–	–	–	
(I_{OH} = 10 mA				–	–	2.5	3.30	–	–	–	
(I_{OH} = 15 mA)				–	–	2.2	3.08	–	–	–	
(I_{OH} = 0 mA)			10	–	–	8.0	9.09	–	–	–	Vdc
(I_{OH} = 5.0 mA)				–	–	7.7	8.45	–	–	–	
(I_{OH} = 10 mA)				–	–	7.5	8.30	–	–	–	
(I_{OH} = 15 mA)				–	–	7.1	8.14	–	–	–	
(I_{OH} = 0 mA)			15	–	–	–	14.12	–	–	–	Vdc
(I_{OH} = 5.0 mA)				–	–	–	13.81	–	–	–	
(I_{OH} = 10 mA)				–	–	–	13.70	–	–	–	
(I_{OH} = 15 mA)				–	–	–	13.61	–	–	–	
Output Drive Current		I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)	Sink		5.0	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)			10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	
Input Leakage Current		I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation		P_Q									mW
			5.0	–	0.25	–	0.00005	0.25	–	3.5	
			10	–	1.0	–	0.00022	1.0	–	14	
			15	–	–	–	0.00050	–	–	–	
Power Dissipation** (Dynamic plus Quiescent) (C_L = 15 pF)		P_D	5.0	P_D = (56 mW/MHz) f + P_Q							mW
			10	P_D = (225 mW/MHz) f + P_Q							
			15	P_D = (510 mW/MHz) f + P_Q							

*T_{low} = -55°C for MC14415EFL, EVL; -40°C for MC14415FL,FP,VL,VP
T_{high} = +125°C for MC14415EFL,EVL; +85°C for MC14415FL,FP,VL,VP

**The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time*	t_{TLH}					ns
t_{TLH} = (2.0 ns/pF) C_L + 10 ns		5.0	–	40	85	
t_{TLH} = (1.25 ns/pF) C_L + 6 ns		10	–	25	60	
t_{TLH} = (1.10 ns/pF) C_L + 3 ns		15	–	20	–	
Output Fall Time*	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 47 ns		5.0	–	70	150	
t_{THL} = (0.75 ns/pF) C_L + 24 ns		10	–	35	80	
t_{THL} = (0.55 ns/pF) C_L + 17 ns		15	–	25	–	
Turn-Off Delay Time*	t_{PLH}					ns
t_{PLH} = (2.7 ns/pF) C_L + 560 ns		5.0	–	600	1200	
t_{PHL} = (1.2 ns/pF) C_L + 282 ns		10	–	300	600	
t_{PLH} = (0.91 ns/pF) C_L + 286 ns		15	–	150	–	
Turn-On Delay Time*	t_{PHL}					ns
t_{PHL} = (2.4 ns/pF) C_L + 564 ns		5.0	–	600	1200	
t_{PHL} = (1.0 ns/pF) C_L + 285 ns		10	–	300	600	
t_{PHL} = (0.75 ns/pF) C_L + 289 ns		15	–	150	–	
Turn-On Delay Time (Inhibit to Output)	t_{PHL}					ns
		5.0	–	300	550	
		10	–	225	425	
		15	–	110	–	
Turn-Off Delay Time (Inhibit to Output)	t_{PLH}					ns
		5.0	–	300	550	
		10	–	225	425	
		15	–	110	–	
Input Pulse Coincidence (Figure 3)	PC_{min}					ns
		5.0	500	450	–	
		10	450	350	–	
		15	–	–	–	
Input Pulse Width (Figure 1)	t_{WH}					ns
		5.0	500	450	–	
		10	450	350	–	
		15	–	–	–	
Input Clock Frequency	f_{cl}					MHz
		5.0	–	0.7	–	
		10	–	1.0	–	
		15	–	1.5	–	
Clock Input Rise and Fall Times (Figure 1)	t_{TLH}, t_{THL}	5.0	–	–	15	µs
		10	–	–	5.0	
		15	–	–	–	

* The formula given is for the typical characteristics only.

FIGURE 1 – SWITCHING CHARACTERISTICS – WAVEFORM RELATIONSHIPS

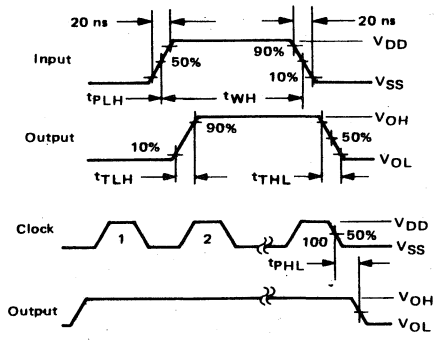


FIGURE 2 – AMBIENT TEMPERATURE POWER DERATING

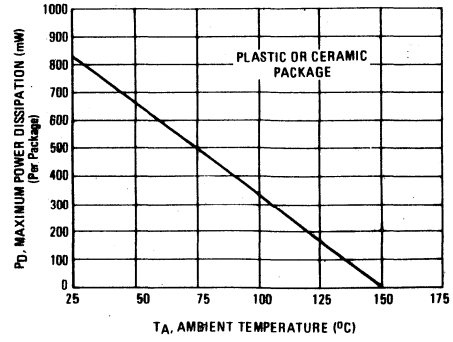
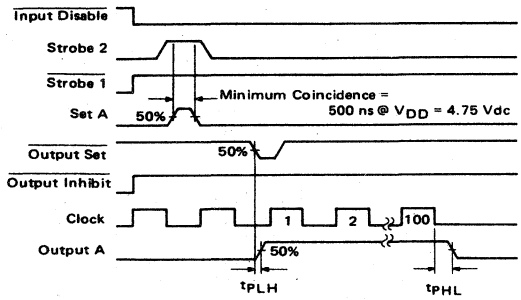
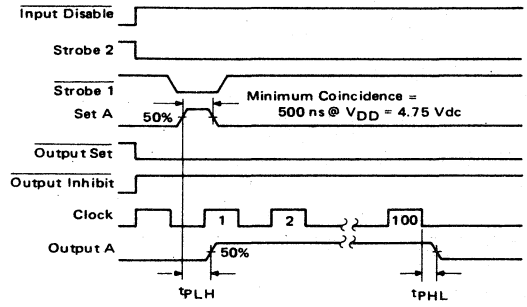


FIGURE 3 – TYPICAL OPERATION MODES AND FUNCTIONAL TIMING DIAGRAM

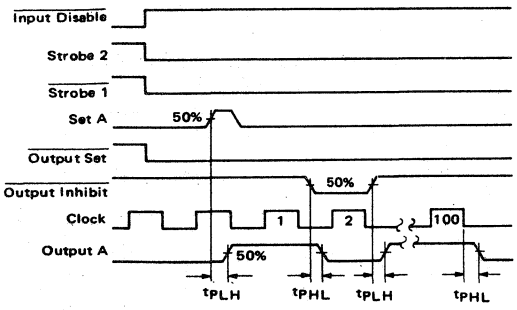
MODE 1 – $\overline{\text{OUTPUT SET}}$ INITIATES TIME DELAY



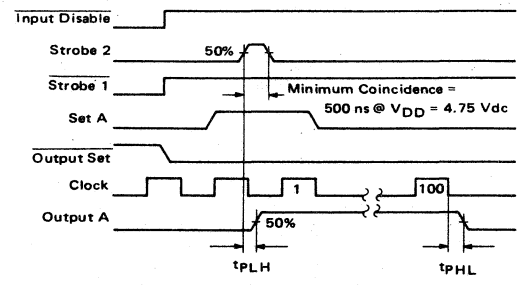
MODE 2 : SET A INITIATES TIME DELAY



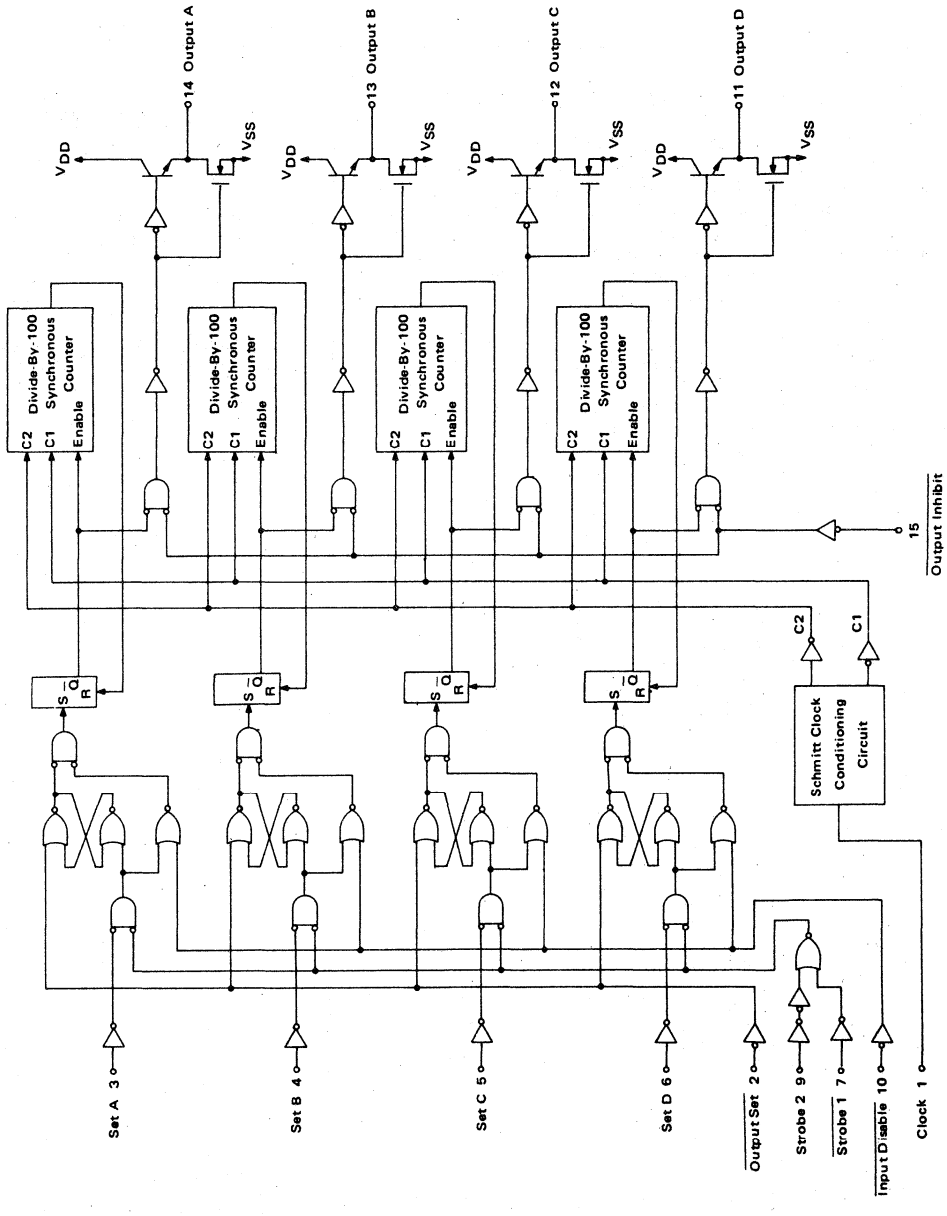
MODE 3: $\overline{\text{OUTPUT INHIBIT}}$ DISABLES TIME DELAY



MODE 4: POSITIVE-EDGE STROBE (ST2) INITIATES TIME DELAY



LOGIC DIAGRAM



MOTOROLA

MC14419

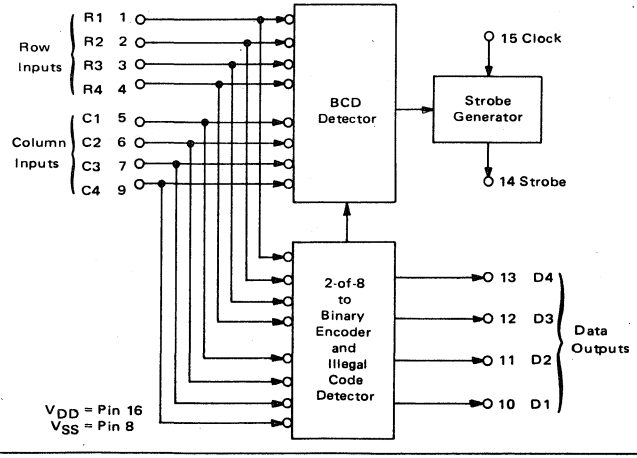
2-OF-8 KEYPAD-TO-BINARY ENCODER

The MC14419 is designed for phone dialer system applications, but finds many applications as a keypad-to-binary encoder. The device contains a 2-of-8 to binary encoder, a strobe generator, and an illegal state detector. The encoder has four row inputs and four column inputs, and is designed to accept inputs from 16 keyswitches arranged in a 4 x 4 matrix. For an output on the four data lines, one and only one row along with one and only one column input line must be activated. All other combinations are suppressed by the illegal state detector to eliminate false data output.

The strobe generator produces a strobe pulse when any of the 10 keys corresponding to numerals 0 through 9 are depressed. The strobe output can be used to eliminate erroneous data entry due to contact bounce. For a strobe output to occur, the key row and column input lines must remain stable for 80 clock pulses after activation. When the contact bounce has settled and 80 clock pulses have occurred, the output will be a single strobe pulse equal in width to that of the clock low state. The strobe generator will output one and only one pulse each time a numerical key is depressed. After the pulse has occurred, noise and bounce due to contact break will not cause another strobe pulse. With a 16 kHz input clock frequency, the pulse occurs 5 ms after the last bounce.

- Suppressed Output for Illegal Input Codes
- On-Chip Pullup Resistors for Row and Column Inputs
- Clock Input Conditioning Circuit
- Low Current Drain in Standby Mode
  5.0 μA Typical @ 5.0 Vdc
- Subsystem Complement to the MC14408/14409 Phone Pulse Converter
- Codes for Numbers 0-9 Produce a Strobe Pulse

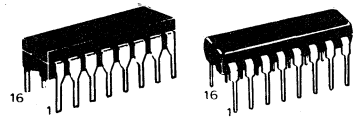
BLOCK DIAGRAM



CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

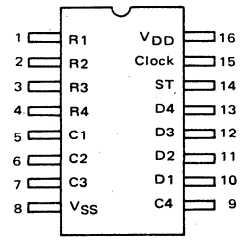
2-OF-8 KEYPAD-TO-BINARY ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



VDD = Pin 16
VSS = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage Operating Range	V_{DD}	–	3.0	6.0	3.0	5.0	6.0	3.0	6.0	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	1.5	–	1.5	2.25	–	1.4	–	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.25	–	3.6	–	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	mAdc
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
Input Leakage Current (V_{in} = V_{DD})	I_{IH}	5.0	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Pullup Resistor Source Current (Row and Column Inputs) (V_{in} = V_{SS})	I_{IL}	5.0	265	460	190	250	330	125	215	μAdc
Input Capacitance (V_{in} = V_{SS})	C_{in}	–	–	–	–	5.0	–	–	–	pF
Standby Supply Current (f_{clock} = 16 kHz, No Keys Depressed)	I_{DDS}	3.0	–	3.0	–	1.0	3.0	–	6.0	μAdc
		5.0	–	15	–	5.0	15	–	30	
		6.0	–	60	–	20	60	–	120	
Standby Supply Current as a Function of Clock Frequency* (No Keys Depressed)	I_{DDS}	5.0	I_{DDS} = 0.09 μA/kHz + 3.0 μA							μAdc

*The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise and Fall Times, D1 thru D4 (Figure 1)	t_{TLH}, t_{THL}	5.0	–	300	–	ns
Propagation Delay Time, Row or Column Input to Data Output (Figure 1)	t_{PLH}, t_{PHL}	5.0	–	1000	–	ns
Clock Pulse Frequency Range	PRF	3.0 to 6.0	–	–	80	kHz

FIGURE 1 – SWITCHING TIME WAVEFORMS

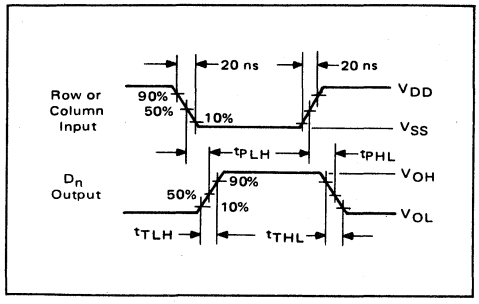
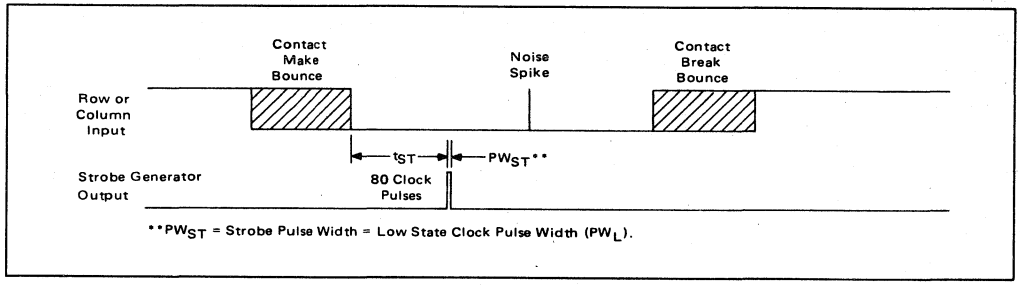


FIGURE 2 – TYPICAL STROBE PULSE DELAY TIMES

PRF Clock Frequency kHz	t_{ST}* Strobe Pulse Delay Time ms
4.0	20
8.0	10
16	5.0
32	2.5
80	1.0

*t_{ST} = (1/PRF) • 80, with PRF in kHz, t_{ST} in ms.

FIGURE 3 – STROBE GENERATOR TIMING DIAGRAM



**PW_{ST} = Strobe Pulse Width = Low State Clock Pulse Width (PW_L).

TRUTH TABLE

	Inputs								Outputs				
	Row				Column								
Key**	R4	R3	R2	R1	C4	C3	C2	C1	D4	D3	D2	D1	Strobe
1	1	1	1	0	1	1	1	0	0	0	0	1	
2	1	1	1	0	1	1	0	1	0	0	1	0	
3	1	1	1	0	1	0	1	1	0	0	1	1	
A	1	1	1	0	0	1	1	1	1	1	0	0	0
4	1	1	0	1	1	1	1	0	0	1	0	0	
5	1	1	0	1	1	1	0	1	0	1	0	1	
6	1	1	0	1	1	0	1	1	0	1	1	0	
B	1	1	0	1	0	1	1	1	1	1	0	1	0
7	1	0	1	1	1	1	1	0	0	1	1	1	
8	1	0	1	1	1	1	0	1	1	0	0	0	
9	1	0	1	1	1	0	1	1	1	0	0	1	
C	1	0	1	1	0	1	1	1	1	1	1	0	0
*	0	1	1	1	1	1	1	0	1	0	1	0	0
0	0	1	1	1	1	1	0	1	0	0	0	0	
#	0	1	1	1	1	0	1	1	1	0	1	1	0
D	0	1	1	1	0	1	1	1	1	1	1	1	0
	All Other Combinations								0	0	0	0	0

**See Figure 4 for keypad designation.

FIGURE 4 – TYPICAL KEYPAD INTERFACE APPLICATION

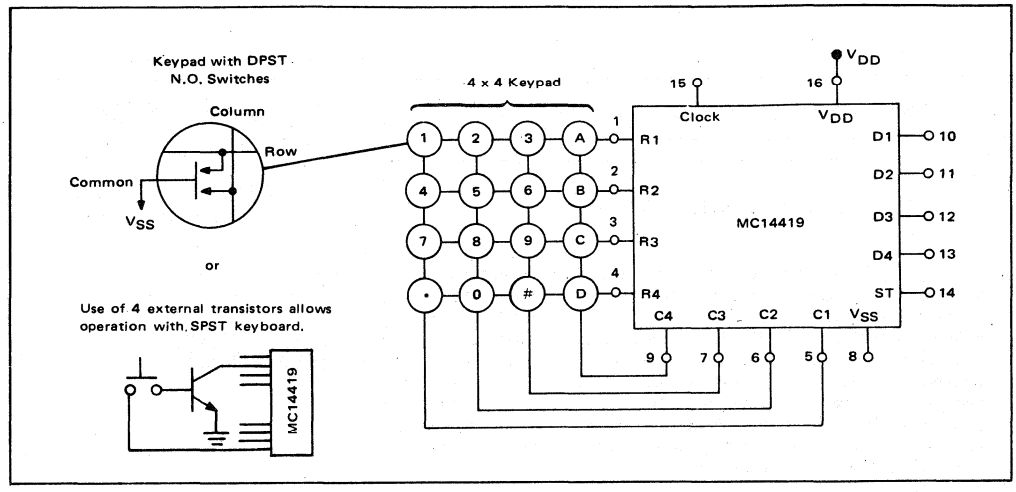
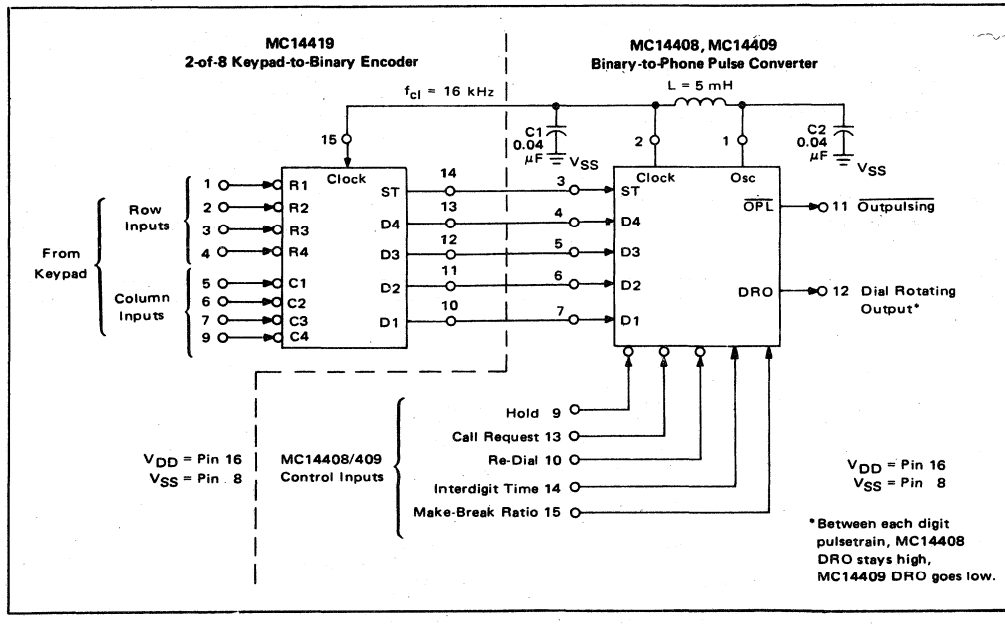


FIGURE 5 – PHONE DIALER SYSTEM



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14422

Advance Information

CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

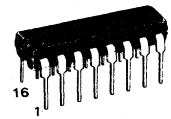
REMOTE CONTROL TRANSMITTER

REMOTE CONTROL TRANSMITTER

The MC14422 is a remote control transmitter circuit designed for use in television receivers, security controls, toys, industrial remote controls, and remote control locks. The circuit is intended for use with the MC6525 or MC6526 NMOS remote control receiver.

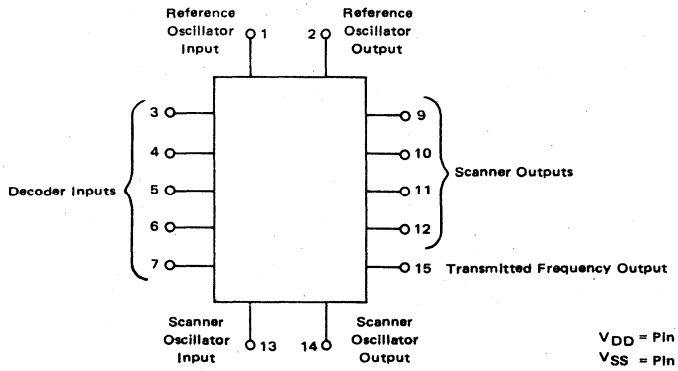
Using digital frequency multiplexing, the MC14422 generates five frequencies which are transmitted sequentially to form a code corresponding to a particular function in the receiver circuit. The wide channel spacing between these frequencies eliminates problems due to doppler effect. The frequency multiplex system inherently provides a good degree of noise immunity.

- 22 Channel Capacity
- Transmission of Information Is Achieved by Time Multiplexing Five Frequencies
- No Possibility of Doppler Effect Interference
- Extremely Low External Component Count
- Low Power Consumption
- Designed for Use with the MC6525 or MC6526 Remote Control Receiver



P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +10	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	0 to +55	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{DD}	5.0	–	8.0	Vdc
Supply Current		I_{DD}				
(V_{DD} = 8.0 Vdc)	Idle		–	0.4	100	μAdc
	Operating		–	–	10	mAdc
Output Drive Current		I_{OH}				
(V_{OH} = 4.0 Vdc, V_{DD} = 5.0 Vdc	Source					
Scanner Output			-50	–	–	μAdc
Transmitted Frequency Ouptut			-0.5	–	–	mAdc
Scanner Oscillator Output			-0.1	–	–	mAdc
Reference Oscillator Output			-0.3	–	–	mAdc
(V_{OL} = 1.0 Vdc, V_{DD} = 5.0 Vdc)	Sink	I_{OL}				
Scanner Output			50	–	–	μAdc
Transmitted Frequency Output			0.2	–	–	mAdc
Scanner Oscillator Output			0.1	–	–	mAdc
Reference Oscillator Output			0.3	–	–	mAdc
Input Current		I_{IH}				μAdc
(V_{IH} = 8.0 Vdc, V_{DD} = 8.0 Vdc)	Sink					
Scanner Oscillator Input			–	–	1.0	
Reference Oscillator Input			4.0	–	400	
(V_{IH} = 7.0 Vdc, V_{DD} = 8.0 Vdc)	Source					
Decoder Input			-1.0	–	–	
(V_{IL} = 0 Vdc, V_{DD} = 8.0 Vdc)	Source	I_{IL}				μAdc
Scanner Oscillator Input			–	–	1.0	
Reference Oscillator Input			-4.0	–	-400	
(V_{IL} = 1.0 Vdc, V_{DD} = 5.0 Vdc)	Sink					
Decoder Input			–	–	-25	
Reference Oscillator Frequency (V_{DD} = 5.0 Vdc)		f_{ref}	–	–	1.0	MHz

CIRCUIT OPERATION

As shown in Figure 1, until a matrix switch is depressed, the decoder inputs (pins 3 through 7) are high, all scanner outputs (pins 9 through 12) are low, and both the scanner and reference oscillators, as well as the output gate control circuit, are switched off. This is referred to as the "idle" mode. In this mode, with a significant part of the circuit switched off, current consumption is reduced to a minimum. The decoder section, however, remains in continuous operation so that a switch matrix command can be recognized. When a switch is depressed, the decoder will set the five latches in accordance with the correct code (see Figure 2). At the same time, a latch is triggered which activates the idle line and turns on the reference oscillator, the scanner oscillator, the row enable, and the output gate control.

When the switch is operated just prior to time period t1, the following happens:

1. The scanner outputs become active and take up their respective code corresponding to t1 when the next negative going edge of the scanner oscillator occurs.
2. The reference oscillator is switched on.
3. The output gate control idle input is enabled.

Note: No output can occur at the transmitted frequency output (pin 15) until the negative going edge of the pin 12 scanner output signal has occurred at the end of time t4.

The timing example of Figure 1 uses the matrix connection of pin 4 connected to pin 11. Table 1 shows that the code for this connection is f_a transmitted in time period t2 and f_b transmitted in time period t3. After the negative going edge of the pin 12 scanner pulse has enabled the output gate control, an output cycle can begin. Therefore, in this case no output occurs in the time period t1, f_a and f_b are transmitted in time periods t2 and t3 respectively, and no output occurs during time t4.

The code is repeated continuously at pin 15 until the matrix switch is released. At this point the circuit completes the scan cycle and the trailing edge of the pin 12 scanner signal returns the circuit to its "idle" position.

The transmitted frequencies are generated by dividing a reference oscillator frequency by a variable divider circuit which is controlled by the decoder outputs.

TABLE 1 – TRANSMITTED FREQUENCY CODE

Channel Number	Matrix Connections Pin to Pin		Transmitted Frequencies t1	t2	t3	t4
1	7	12	f_e			
2	7	9	f_e	f_a		
3	7	10	f_e		f_b	
4	7	11	f_e	f_a	f_b	
5	6	12	f_e			f_c
6	6	9	f_e	f_a		f_c
7	6	10	f_e		f_b	f_c
8	6	11	f_e	f_a	f_b	f_c
9	5	12	f_e			f_d
10	5	9	f_e	f_a		f_d
11	5	10	f_e		f_b	f_d
12	5	11	f_e	f_a	f_b	f_d
13	4	12			f_b	
14	4	11		f_a	f_b	
15	3	9				f_c
16	3	10		f_a		f_c
17	4	9			f_b	f_c
18	4	10		f_a	f_b	f_c
19	3	12				f_d
20	3	11		f_a		f_d
21	3,4	12			f_b	f_d
22	3,4	11		f_a	f_b	f_d

TABLE 2 – OUTPUT FREQUENCIES

Frequencies	Output Frequency	Division Ratio
f_a	34.688 kHz	f2/26.5
f_b	36.048 kHz	f2/25.5
f_c	37.519 kHz	f2/24.5
f_d	39.116 kHz	f2/23.5
f_e	42.755 kHz	f2/21.5

f2 = 919.222 kHz reference frequency

FIGURE 1 – TIMING DIAGRAM
(Pin 4 Connected to Pin 11)

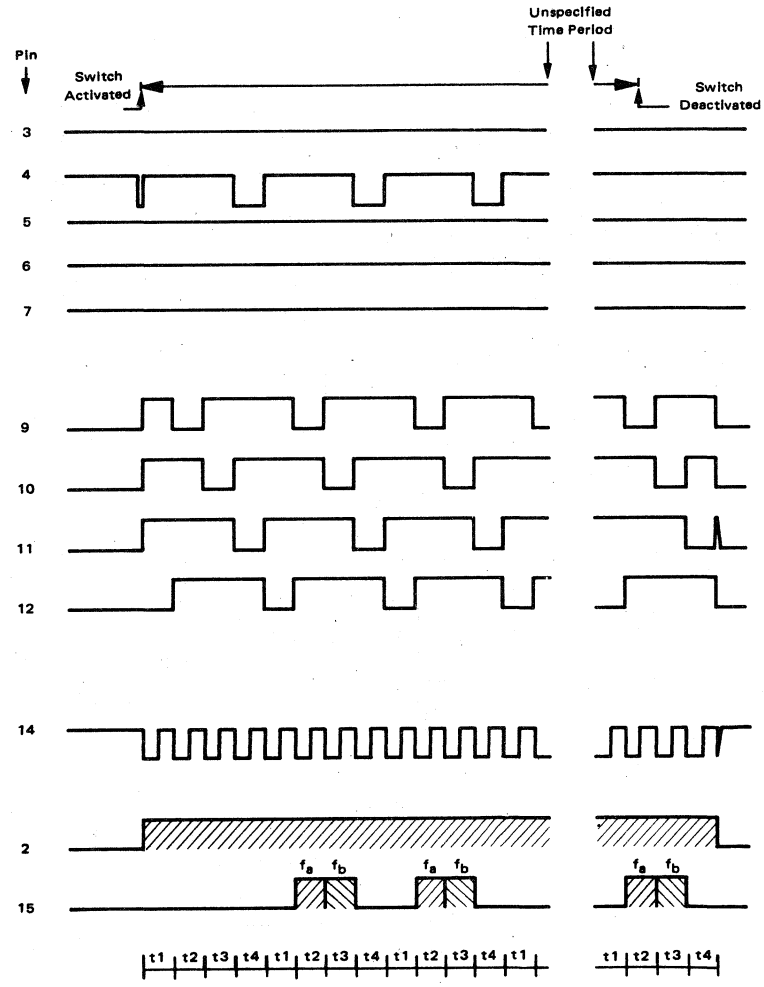


FIGURE 2 – TYPICAL APPLICATION

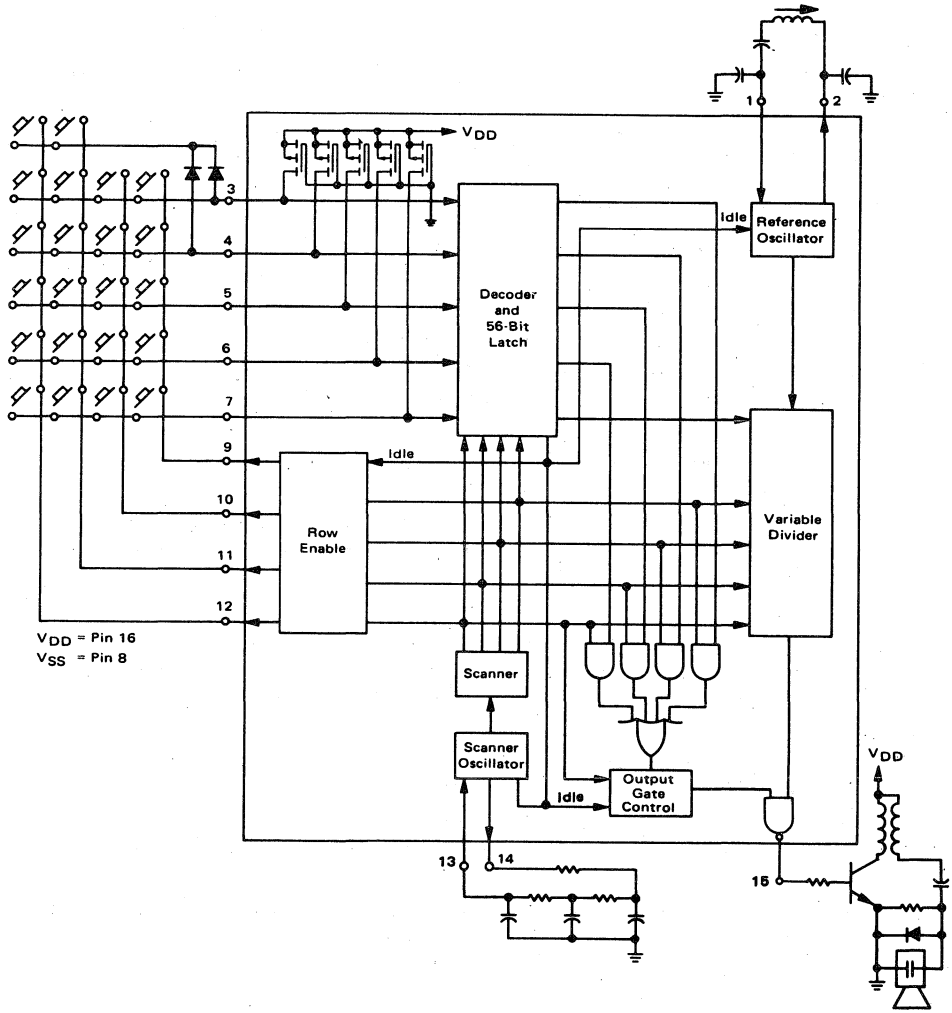


FIGURE 3 - REFERENCE OSCILLATOR EXTERNAL COMPONENTS

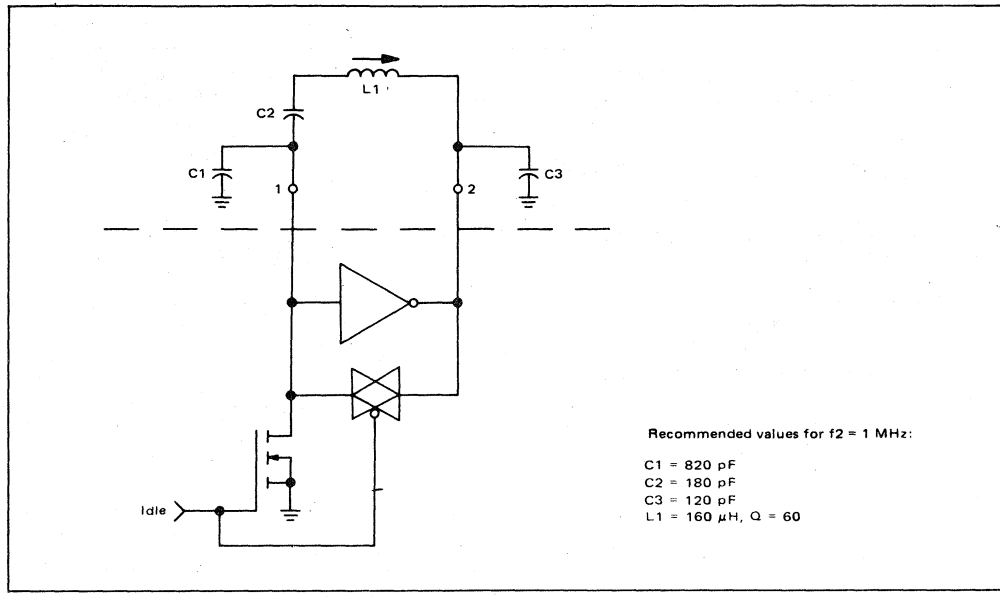
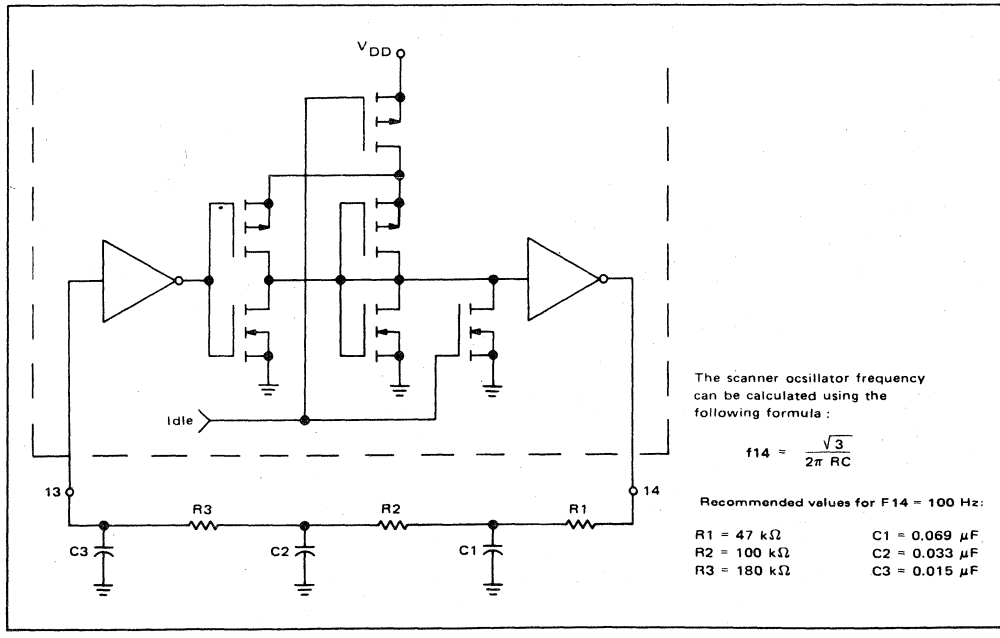


FIGURE 4 - SCANNER OSCILLATOR EXTERNAL COMPONENTS



MOTOROLA

MC14424

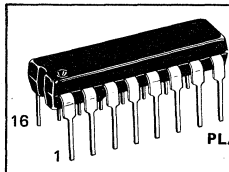
ADVANCE INFORMATION

CMOS
REMOTE CONTROL TRANSMITTER

REMOTE CONTROL TRANSMITTER

The MC14424 is a remote control transmitter circuit in CMOS high performance technology.

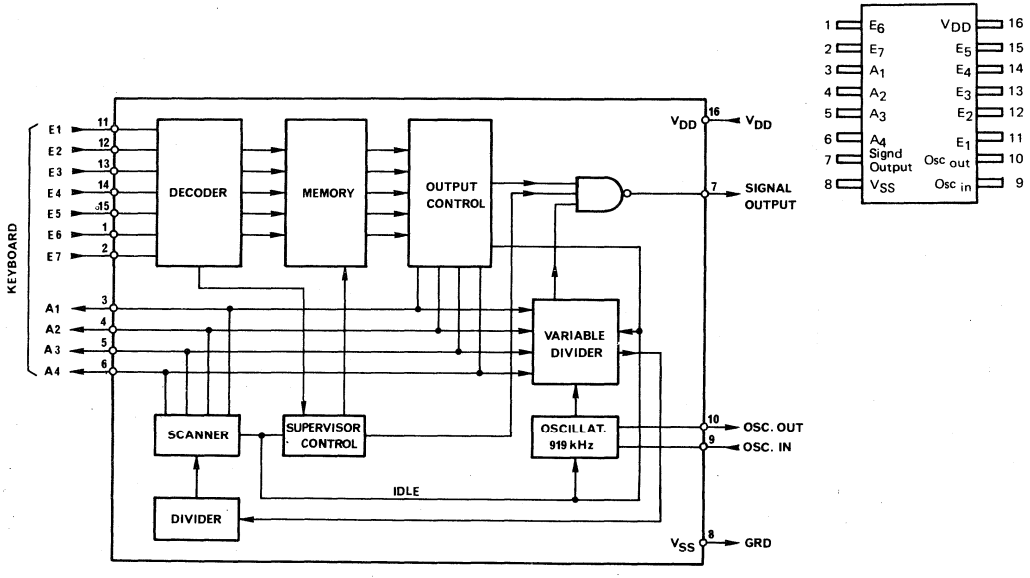
- 31 channel capability
- Transmission of information is achieved by time multiplexing 5 modulation frequencies
- The chosen frequency band is free from line frequency harmonics generated in television receivers
- Suitable for application with ultrasonic or infrared transducers
- Extremely low external component count
- Low power consumption
- Designed to be used in conjunction with the remote control receiver integrated circuits MC6525, MC6526, MC6527, MC6529.



PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

FIGURE 1 – BLOCK DIAGRAM & PIN ASSIGNEMENT



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+10 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	0 to +55	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

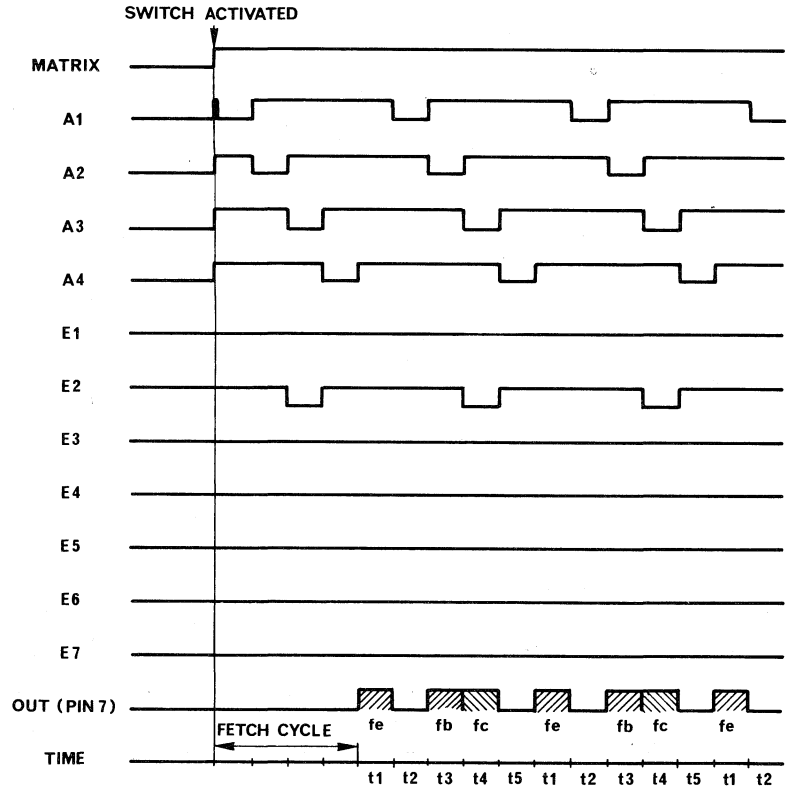
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	3.8	–	9.8	Vdc
Supply Current		I_{DD}				μAdc
(V_{DD} = 9.8 Vdc)	Idle		–	0.1	15	
	Operating		–	2		mAdc
Output Drive Current		I_{OH}				
(V_{OH} = 2.8 Vdc, V_{DD} = 3.8 Vdc)	Source					
Scanner Output			−58	–	–	μAdc
Transmitted Frequency Output			−1.15	–	–	mAdc
Reference Oscillator Output			−1.4	–	–	
(V_{OL} = 1 Vdc, V_{DD} = 3.8 Vdc)		I_{OL}				mAdc
Scanner Output	Sink		0.69	–	–	
Transmitter Frequency Output			0.23	–	–	
Reference Oscillator Output			2.1	–	–	
Input Current		I_{IH}				μAdc
(V_{IH} = 9.8 Vdc, V_{DD} = 9.8 Vdc)	Sink		2.3	–	170	
Reference Oscillator Input						
(V_{IH} = 8.8 Vdc, V_{DD} = 9.8 Vdc)	Source		−11	–	–	
Decoder Input						
(V_{IL} = 0 Vdc, V_{DD} = 9.8 Vdc)	Source	I_{IL}	−2.3	–	−170	μAdc
Reference Oscillator Input						
(V_{IL} = 1 Vdc, V_{DD} = 3.8 Vdc)	Sink		–	–	−85	
Decoder Input						
Reference Oscillator Frequency		f_{ref}				MHz
(V_{DD} = 3.8 Vdc)			0.1	0.919	1.0	

CIRCUIT OPERATION

In the stand-by mode, the scanning outputs A1, A2, A3, A4 are forced to "0" by the scan output stages, decoder inputs E1....E7 (see block diagram, Fig. 1) are forced to "1" by internal pull-up devices. If any of the keys of the matrix is now operated, the appropriate input will be forced to "0" and hence the circuit is instructed that a key has been operated. The supervisory control will now enable the reference oscillator and will release the scanning outputs. During the first scan cycle, called the fetch cycle, the IC is identifiying the key which initiated the fetch cycle. The memory will load the corresponding 5 bit word containing the modulation frequency combination to be supplied the output.

In the operating mode, the variable divider is generating sequentially five modulation frequencies (see Fig. 4). The sequence is controlled by the scanner. Frequency f_e is generated at time t_1, f_d at time t_2, f_b at time t_3, f_c at time t_4 and f_a at time t_5 (see timing diagram, Fig. 2). Following the fetch cycle, the output control block will enable the output buffer according to the wanted frequency combination, always beginning at t_1. Transmitted frequencies f_a...f_e and the scanner timing of 10 msec are both derived from a reference LC oscillator externally adjustable at 919 KHz.



EXAMPLE ABOVE: CHANNEL 7, CONNECTION A3 – E2

FIGURE 2 – TIMING DIAGRAM

FIGURE 4 – OUTPUT FREQUENCIES

COMMAND[1]		Transmitted frequencies						Matrix connections	
		Channel	f_a	f_b	f_c	f_d	f_e	Pin	to Pin
Program + ON									
1		1	0	0	0	0	1	11	3
2		2	1	0	0	0	1	11	4
3		3	0	1	0	0	1	11	5
4		4	1	1	0	0	1	11	6
5		5	0	0	1	0	1	12	3
6		6	1	0	1	0	1	12	4
7		7	0	1	1	0	1	12	5
8		8	1	1	1	0	1	12	6
9		9	0	0	0	1	1	13	3
10		10	1	0	0	1	1	13	4
11		11	0	1	0	1	1	13	5
12		12	1	1	0	1	1	13	6
13		13	0	0	1	1	1	14	3
14		14	1	0	1	1	1	14	4
15		15	0	1	1	1	1	14	5
16		16	1	1	1	1	1	14	6
Colour saturation	CS–	17	0	1	0	0	0	15	5
	CS+	18	1	1	0	0	0	1	3
Volume	VO–	19	0	0	1	0	0	15	3
	VO+	20	1	0	1	0	0	1	4
Brightness	BR–	21	0	1	1	0	0	15	6
	BR+	22	1	1	1	0	0	1	6
Standby	STB	23	0	0	0	1	0	2	3
Sound killer	SK	24	1	0	0	1	0	2	4
General Purpose	Q25	25	0	1	0	1	0	2	5
General Purpose	Q26	26	1	1	0	1	0	2	6
General Purpose	Not decoded by receiver	27	1	0	0	0	0	15	4
General Purpose		28	0	0	1	0	0	1	5
General Purpose		29	1	0	1	1	0	1 & 2	4
General Purpose		30	0	1	1	1	0	1 & 2	5
General Purpose		31	1	1	1	1	0	1 & 2	6

[1] When used in conjunction with the MC6529 receiver.

FIGURE 3 – TRANSMITTED FREQUENCY CODE

Frequencies	Timing	Output frequency	Division ratio
f_a	t_5	34.688 KHz	$\frac{f_2}{26.5}$
f_b	t_3	36.048 KHz	$\frac{f_2}{25.5}$
f_c	t_4	37.519 KHz	$\frac{f_2}{24.5}$
f_d	t_2	39.116 KHz	$\frac{f_2}{23.5}$
f_e	t_1	42.755 KHz	$\frac{f_2}{21.5}$

f_2 = 919.222 KHz reference frequency

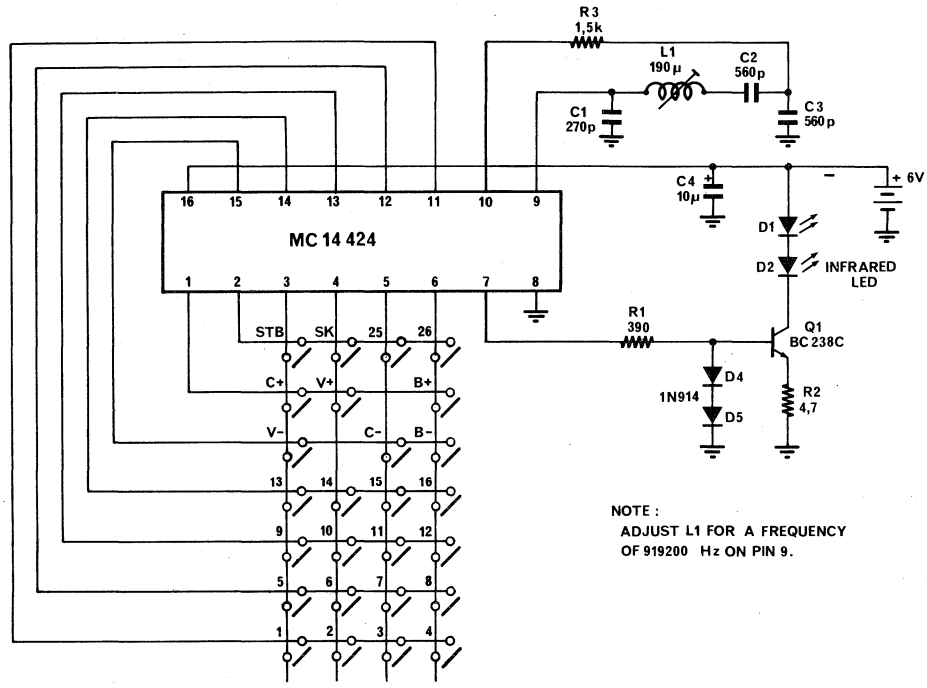


FIGURE 5 – INFRARED REMOTE CONTROL TRANSMITTER TYPICAL CIRCUIT DIAGRAM

MOTOROLA

MC14425

TUNING MEMORY SYSTEM CONTROL CIRCUIT

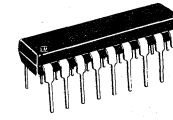
The MC14425 Control circuit will perform the following functions when used in conjunction with the MC14426 Memory and the UAA1008 or UAA1008A Linear Processors.

- LC Clock generator
- UP/DOWN Counter providing information for memory
- Rate multiplier for D/A conversion
- Shift register for memory data access and storage of new data
- 2, 3 or 4 TV band counter with automatic or manual switching
- Control section for automatic or manual search of TV stations
- Automatic volume muting control during search and program change

CMOS

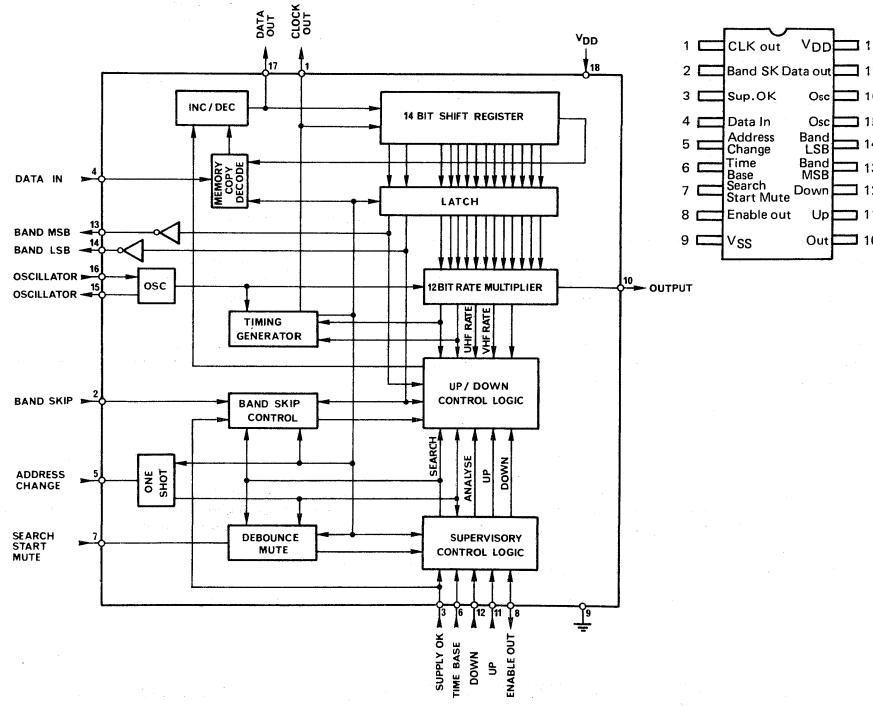
(LOW-POWER COMPLEMENTARY MOS)

TUNING MEMORY SYSTEM CONTROL CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 701

FIGURE 1 – MC14425 BLOCK DIAGRAM AND PIN-OUT



MAXIMUM RATINGS (T_A = 25 °C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6 to −0.5	Vdc
Input Voltage, All inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70 °C) Voltages referenced to V_{SS}, pin 9.

Characteristics		Symbol	Min.	Typ.	Max.	Unit
Power Supply Operating Range		V_{DD}	4.95	5.2	6	Vdc
Input Current, All inputs (except pins 5, 7)		I_{in}	–	10	–	pAdc
Enable Output Current	(V_{DD} −0.4 V) (V_{OL} = 0.4 V)	I_{OH} I_{OL}	280 280	– –	– –	μAdc
Band Switching Output Current	(V_{DD} −0.4 V) (V_{OL} = 0.4 V)	I_{OH} I_{OL}	280 280	– –	– –	μAdc
Other Output Currents	(V_{DD} −0.4 V) (V_{OL} = 0.4 V)	I_{OH} I_{OL}	280 280	– –	– –	μAdc
One Shot Output, Search & Mute (see[1])	(V_{OL} = 0.4 V)	I_{OL}	280	–	–	μA
Oscillator	(V_{DD} −0.4 V) (V_{OL} = 0.4 V)	I_{OH} I_{OL}	160 160	– –	– –	μA
Power Dissipation @ 200 kHz		P_D		5		mW
Oscillator Frequency		f_o	50		350	kHz

[1] An external pull-up resistor must be provided on pin 7.

BAND SELECTION LOGIC TABLE

Band	Pin 14	Pin 13	Ramp Speed[1]
UHF	0	0	10 sec.
VHF 1	1	0	2.5 sec.
VHF 3	0	1	2.5 sec.
CABLE	1	1	2.5 sec.

[1] At 200 KHz Clock frequency

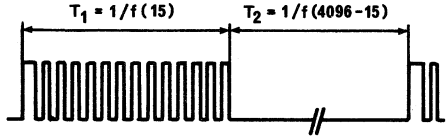
Band Skip	Connect
CABLE	Pin 2 to Pin 13
VHF 3 & CABLE	Pin 2 to Pin 14

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

INPUT/OUTPUT FUNCTIONS

CLOCK OUT – Clock pulses (PIN 1) control the transfer of data between the MC14425 control chip and the MC14426 memory chip via pins 4 and 17. For best system performance the oscillator circuit should generate a pulse train of approximately 200 KHz, however frequency value is not critical.
The clock out signal timing is shown below.



f = Oscillator frequency;
$T_1 + T_2$ = Rate Multiplier;
T_1 = Shift Cycle.

BRM OUTPUT – The binary rate multiplier output is available on pin 10.
The binary word cycle is approximately 20msec for a clock frequency of 200KHz (5 μsec pulse width). The output provides pulses symmetrically spaced to facilitate the filtering when doing D/A convertion.
In the block diagram of Figure 1 the least significant bit is to the right. Bits 13 and 14 represent band information, therefore overflow of the rate multiplier control word automatically increments band information.

SEARCH & MUTE – Search mode is initiated by presenting a 0 on pin 7. For trouble free operation the signal on pin 7 is debounced internally on both edges for 10msec. As soon as search is initiated and the debounce cycle is terminated this pin becomes an output for the mute signal which is available during the whole cycle. The search cycle ends when a valid station is found and the one shot (R/C on pin 5) has timed out. The mute signal is available also at address change and during any other time the one shot is active. Each time the oneshot is reset the mute output will momentarily go to high and back to low for less than 10 msec. It is therefore recommended to introduce a proper time constant on this line to smooth out the mute function.
Mute is also provided when supply OK input (pin 3) is V_{SS}.
Three search modes are present:

1. Fast search, generally used for VHF applications, with a rate of change of 32 steps per clock cycle and a scan time of 2.5 seconds.
2. Slow search, generally used for UHF applications, with a rate of change of 8 steps per clock cycle and a scan time of 10 seconds.
3. Tracking mode, used for manual search or normal locked on conditions, with a rate of change of 1 step per clock cycle and a scan time of 80 seconds.

Search mode is terminated by the simultaneous presence of a 1 on both inputs UP (pin 11) and DOWN (pin 12).

SUPPLY OK – An input (pin 3) is provided to ensure that during power failures, flash-overs, low supply voltages, etc... no memory information can be modified or lost. In operating conditions it should receive a 1 from the linear processor UAA1008. When at 0 the Search FF, analyse FF and Band skip FF are all reset. The UP/DOWN control logic is not inhibited and a 1 on the UP or DOWN inputs still could modify the content of the shift register.
However, due to the fact that the memory circuit does not send any information when Supply OK is at 0, no data can be modified.

TIME BASE – This input (pin 6) receives a 1 whenever coincidence between fly-back and video sync signals has been detected by the linear processor circuit UAA1008. In the search mode the presence of a 1 on pin 6 is checked by the analyse flip-flop set by the one shot. If time base information is present before the one shot is timed out (usually 400 msec. from ramp stop) the analyse FF is reset, search/mute ends and a stable situation reached.
Should time base be 0 when the one shot times out, search will resume if the system was in search mode.
If in Memory/Normal mode, the presence of a 1 on pin 6 will force Enable Out to low, if at 0 Enable Out will go to the tristate condition.

ENABLE OUT – This output (pin 8) is used to control the AFC OUT gate and UP/DOWN overlap in the linear processor circuit UAA1008.
Its truth-table is the following:

Search FF (internal)	Analyse FF (internal)	Time Base IN (PIN 6)	Enable OUT (PIN 8)
0	0	0	Tristate
0	0	1	0
0	1	0	0
0	1	1	0
1	X	X	1

X : Don't care

- The first line of the truth table indicates that the system is in its memory mode and that no TV station is received.
- The second line indicates that a valid TV station is received and system is in its normal memory mode.
- The third line shows the states during the "oneshot" period, e.g. the search function has been interrupted temporarily and waits for Time Base signal.
- The fourth line is as above but Time Base is present.
- The fifth line represents Search mode, the search FF is set and enable out is forced to 1.

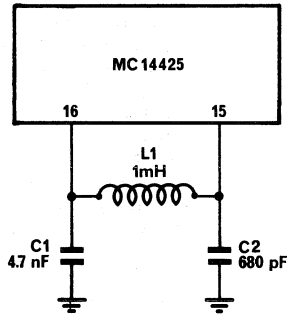
UP & DOWN – These two inputs (pin 11 & 12) have two modes of operation.
When the system is in search, only the simultaneous presence of an UP and a DOWN signal, both of them at 1,

will interact with the system by stopping the search ramp. A 1 on only one of the two inputs neither stops search nor reduces search speed.
When the circuit is not in search, a 1 on the UP or DOWN inputs results in adding or subtracting a one to or from the content of the 14 bit shift register during each rate multiplier cycle.

BAND CODE – Refer to band selection logic table for output code (pin 13 MSB, pin 14 LSB).
A maximum of four bands are available. Three or two bands only can be obtained by connecting pin 2 to pin 13 or 14 as per table 1.
Note that no debounce network is included on pin 2 input. Therefore, if manual band skip is required, provision for a bounce-free input signal has to be made.

APPLICATION INFORMATION

RECOMMENDED OSCILLATOR CONFIGURATION



$f_o = 200$ KHz

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MOTOROLA

MC14426

TUNING MEMORY SYSTEM MEMORY CIRCUIT

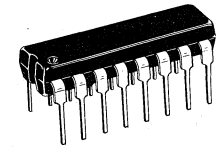
The MC14426 Memory Circuit provides the storage of the tuning voltage and band information for 8 TV stations when used in conjunction with the MC14425/9 Control Unit.

- 8 static shift registers of 14 bit length
- Expansion of up to 32 channels possible without external logic
- Output available indicating address change
- Low voltage (1 volt) technology requires a single cell battery as back up power source
- Extremely low power consumption

CMOS

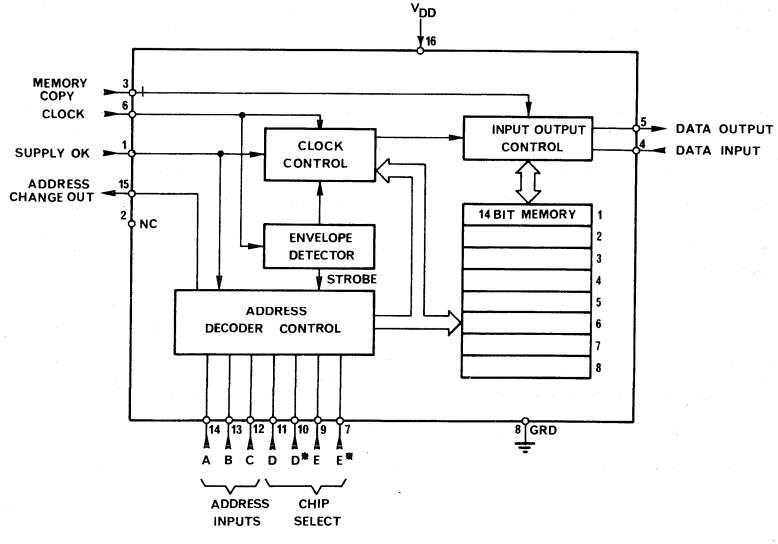
(LOW-POWER COMPLEMENTARY MOS)

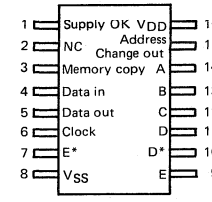
TUNING MEMORY SYSTEM MEMORY CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 – MC14426 BLOCK DIAGRAM AND PIN-OUT





MAXIMUM RATINGS (T_A = 25 °C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6 to −0.5	Vdc
Input Voltage, All inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current drain per pin	I	10	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C) Voltages referenced to V_{SS}, pin 8

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Operating Supply Voltage		V_{DD}	4.0	5.2	6.0	Vdc
Standby Supply Voltage[1]		V_{DD}	1.2	1.5	6.0	Vdc
Quiescent Current	(V_{DD} = 1.5 V) (V_{DD} = 5 V)	I_{DD}		0.008 0.5	2.0 15.0	μAdc
Input Voltage	(V_{DD} = 5 V)	V_{IL} V_{IH}	 4.5		0.5	Vdc
Input Voltage	(V_{DD} = 5 V)	V_{IL} V_{IH}	 4.0		1.0	Vdc
Input Current all Inputs Except Pin 3.	(V_{DD} = 5 V)	I_{IN}		10		pAdc
Input Current[2]	(V_{DD} = 5 V)	I_{IN}	−1.5	−3.0	−6.0	μAdc
Input Capacitance all Inputs	(V_{IN} = 0 V)	C_{IN}		5.0	12.0	pF
Output Current all Outputs (sinking)	(V_{OL} = 0.4 V)	I_{OL}	0.4			mAdc
Three State Output Leakage Current (sinking)	(V_{DD} = 5 V)	I_{TL}	±0.001	±0.001	±5.0	μA
Clock Input Frequency	(V_{DD} = 5 V)	$f_{max.}$ $f_{min.}$	400	700 25	 100	kHz

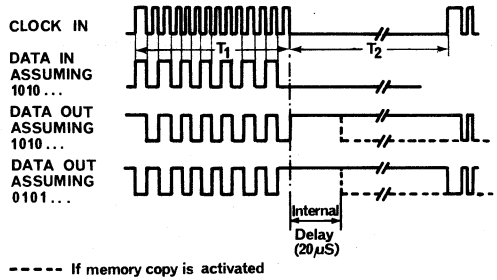
[1] Standby mode is obtained by lowering Supply OK input to V_{SS} during a few read/write cycles. V_{DD} can then be lowered to its standby value, Pin 1 staying low.
In Standby mode no read/write operation can be performed.

[2] An internal pull-up resistor is present on pin 3.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.
Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

INPUT/OUTPUT FUNCTIONS

DATA IN/OUT – The input/output control section provides the interface between the memory and the control circuit MC14425/9 via pins 5 and 4. The output network is active only when the chip is selected and supply OK (pin 1) is at 1. The relationship between clock and input/output signals is shown below:



----- If memory copy is activated

It should be noted that the memory copy information on pin 3 input is inserted into the serial data transfer line which goes to the control circuit during period T_2.

MEMORY COPY – This input is controlled by connecting pin 3 to V_{SS} (ground), which in turn holds down the memory output signal during period T_2. This function allows to transfer the content of the 14 bit shift register of the control circuit MC14425/9 into any memory location as long as this command is present.
Its utilisation is two-fold:

- To resume search for a TV station starting from the last selected station rather than from a random tuning voltage.
- To copy the content of a shift register into a different location. This permits to change the order of TV programs according to the user wish.

SUPPLY OK – In case of power failure this input (pin 1) is used to deactivate all functions of the chip so that no data is lost, rpovided that V_{DD} is held at 1 volt minimum. (See note 1.)
The supply OK signal is enabled in such a way that deactivation during transfer of information is prevented.

ADDRESS INPUTS – To select the 8 memory words only three A, B, C address bits are required. (pins 14, 13, 12.)

Channel	A	B	C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1
7	0	1	1
8	1	1	1

CHIP SELECT – To facilitate the parallel connection of several MC14426 memory circuits, four additional inputs D, D*, E, E* are provided for chip select.
The truth table of chip select inputs is given below.

Chip Selected	Channel	D	D*	E	E*
1	1 to 8	0	0	0	0
2	9 to 16	1	1	0	0
3	17 to 24	0	0	1	1
4	24 to 32	1	1	1	1
None	–	Any other combination			

D* and E* are programming inputs of the chip select network and are normally connected to V_{SS} or V_{DD}.
The logic levels on these inputs specify the levels of the D and E inputs for chip selection.
The chip is selected if D = D* and E = E*.
As shown in the above truth table up to four circuits (32 channels) can be connected in parallel without external decoding.

CLOCK IN – (pin 6) See MC14425/9 data sheet.

ADDRESS CHANGE – An additional function (pin 15) is available to mute the sound section of the TV set during each address change. The 400msec. one-shot on the control dircuit (MC14425/9) provides this feature. This one-shot is triggered by the address change signal supplied by the memory circuit. If the address is changed, the AC signal appears on the leading edge of the internal strobe pulse and lasts one ($T_1 + T_2$) cycle.

MOTOROLA

MC14429A

TUNING MEMORY SYSTEM CONTROL CIRCUIT

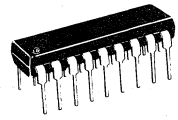
The MC14429A control circuit will perform the following functions when used in conjunction with the MC14426 Memory and the UAA1008A Linear Processor.

- LC Clock generator
- UP/DOWN Counter providing information for memory
- Rate multiplier for D/A conversion
- Shift register for memory data access and storage of new data
- 2, 3 or 4 TV band counter with automatic or manual switching
- Control section for automatic or manual search of TV stations
- Automatic volume muting control during search and program change

CMOS

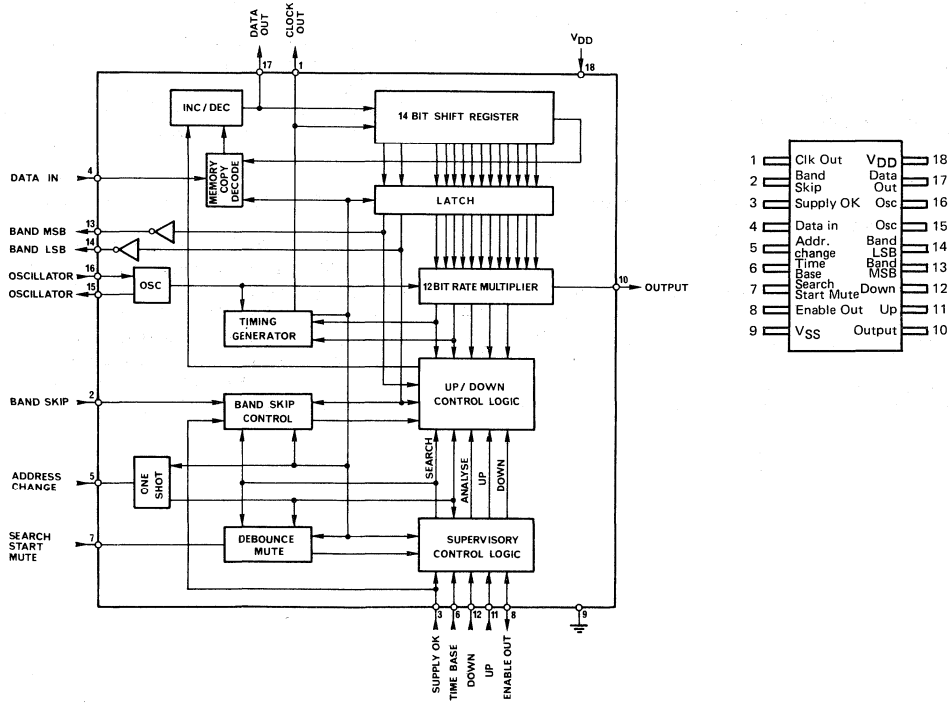
(LOW-POWER COMPLEMENTARY MOS)

TUNING MEMORY SYSTEM CONTROL CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 701

FIGURE 1 – MC14429A BLOCK DIAGRAM AND PIN-OUT



MAXIMUM RATINGS (T_A = 25 °C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6 to −0.5	Vdc
Input Voltage, All inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C) Voltages referenced to V_{SS}, pin 9

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Power Supply Operating Range		V_{DD}	4.95	5.2	6	Vdc
Input Current, All Inputs (except pins 5, 7)		I_{in}	—	10	—	pAdc
Enable Output Current	(V_{DD} −0.4 V) (V_{OL} = 0.4 V)	I_{OH} I_{OL}	280 280	— —	— —	μAdc
Band Switching Output Current	(V_{DD} −0.4 V) (V_{OL} = 0.4 V)	I_{OH} I_{OL}	280 280	— —	— —	μAdc
Other Output Currents	(V_{DD} −0.4 V) (V_{OL} = 0.4 V)	I_{OH} I_{OL}	280 280	— —	— —	μAdc
One Shot Output, Search & Mute (see[1])	(V_{OL} = 0.4)	I_{OL}	280	—	—	μA
Oscillator	(V_{DD} −0.4 V) (V_{OL} = 0.4 V)	I_{OH} I_{OL}	160 160	— —	— —	μA
Power Dissipation @ 300 kHz		P_D		7.5		mW
Oscillator Frequency		f_o	50		350	kHz

[1] An external pull-up resistor must be provided on pin 7.

BAND SELECTION LOGIC TABLE

Band	Pin 14	Pin 13	Ramp Speed[1]
UHF	0	0	7 sec.
VHF 1	1	0	7 sec.
VHF 3	0	1	7 sec.
CABLE	1	1	7 sec.

[1] At 300 KHz Clock frequency

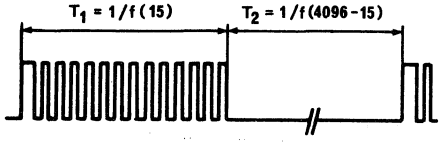
Band Skip	Connect
CABLE	Pin 2 to Pin 13
VHF 3 & CABLE	Pin 2 to Pin 14

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

INPUT/OUTPUT FUNCTIONS

CLOCK OUT – Clock pulses (PIN 1) control the transfer of data between the MC14429A control chip and the MC14426 memory chip via pins 4 and 17. For best system performance the oscillator circuit should generate a pulse train of approximately 300 KHz, however frequency value is not critical.
The clock out signal timing is shown below.



f = Oscillator frequency;
$T_1 + T_2$ = Rate Multiplier;
T_1 = Shift Cycle.

BRM OUTPUT – The binary rate multiplier output is available on pin 10.
The binary word cycle is approximately 13 msec for a clock frequency of 300 KHz (3.3 μsec pulse width). The output provides pulses symmetrically spaced to facilitate the filtering when doing D/A conversion.
In the block diagram of Figure 1. the least significant bit is to the right. Bits 13 and 14 represent band information, therefore overflow of the rate multiplier control word automatically increments band information.

SEARCH & MUTE – Search mode is initiated by presenting a 0 on pin 7. For trouble free operation the signal on pin 7 is debounced internally on both edges for 13 msec. As soon as search is initiated and the debounce cycle is terminated this pin becomes an output for the mute signal which is available during the whole cycle. The search cycle ends when a valid station is found and the one shot (R/C on pin 5) has timed out. The mute signal is available also at address change and during any other time the one shot is active. Each time the oneshot is reset the mute output will momentarily go to high and back to low for less than 13 msec. It is therefore recommended to introduce a proper time constant on this line to smooth out the mute function.
Mute is also provided when supply OK input (pin 3) is V_{SS}.
Two ramp modes are present:

1. Search mode, with a rate of change of 8 steps per clock cycle and a scan time of 7 seconds.
2. Tracking mode, used for manual search or normal locked on conditions, with a rate of change of 1 step per clock cycle and a scan time of 56 seconds.

Search mode is terminated by the simultaneous presence of a 1 on both inputs UP (pin 11) and DOWN (pin 12).

SUPPLY OK – An input (pin 3) is provided to ensure that during power failures, flash-overs, low supply voltages, etc... no memory information can be modified or lost. In operating conditions it should receive a 1 from the linear processor UAA1008A. When at 0 the Search FF, analyse FF and Band skip FF are all reset. The UP/DOWN control logic is not inhibited and a 1 on the UP or DOWN inputs still could modify the content of the shift register.
However, due to the fact that the memory circuit does not send any information when Supply OK is at 0, no data can be modified.

TIME BASE – This input (pin 6) receives a 1 whenever coincidence between fly-back and video sync signals has been detected by the linear processor circuit UAA1008A. In the search mode the presence of a 1 on pin 6 is checked by the analyse flip-flop set by the one shot. If time base information is present before the one shot is timed out (usually 400 msec. from ramp stop) the analyse FF is reset, search/mute ends and a stable situation reached.
Should time base be 0 when the one shot times out, search will resume.
If in Memory/Normal mode, the presence of a 1 on pin 6 will force Enable Out to low, if at 0 Enable Out will go to the tristate condition.

ENABLE OUT – This output (pin 8) is used to control the AFC OUT gate and UP/DOWN overlap in the linear processor circuit UAA1008A.
Its truth-table is the following:

Search FF (internal)	Analyse FF (internal)	Time Base IN (PIN 6)	Enable OUT (PIN 8)
0	0	0	Tristate
0	0	1	0
0	1	0	0
0	1	1	0
1	X	X	1
0	0	X	Tristate

X : Don't care

- The first line of the truth table indicates that the system is in its memory mode and that no TV station is received.
- The second line indicates that a valid TV station is received and system is in its normal memory mode.
- The third line shows the states during the "oneshot" period, e.g. the search function has been interrupted temporarily and waits for Time Base signal.
- The fourth line is as above but Time Base is present.
- The fifth line represents Search mode, the search FF is set and enable out is forced to 1.
- The sixth line represents Address Change, enable out goes tristate during the on time of the one shot.

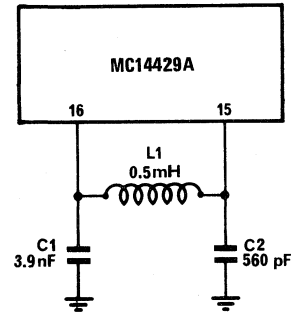
UP & DOWN – These two inputs (pin 11 & 12) have two modes of operation.
When the system is in search, only the simultaneous presence of an UP and a DOWN signal, both of them at 1,

will interact with the system by stopping the search ramp. A 1 on only one of the two inputs does not stop search nor reduce search speed. Logic has been included to improve the "Stop process" by making it independent of the up and down width when both at 1.
When the circuit is not in search, a 1 on the UP or DOWN inputs results in adding or subtracting a one to or from the content of the 14 bit shift register during each rate multiplier cycle.

BAND CODE – Refer to band selection logic table for output code. (pin 13 MSB, pin 14 LSB).
A maximum of four bands are available. Three or two bands only can be obtained by connecting pin 2 to pin 13 or 14 as per band selection logic table.
Note that no debounce network is included on pin 2 input. Therefore, if manual band skip is required, provision for a bounce-free input signal has to be made.

APPLICATION INFORMATION

RECOMMENDED OSCILLATOR CONFIGURATION



$f_o = 300$ KHz

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MOTOROLA

MC14430

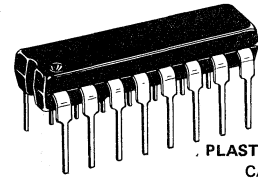
CMOS

INPUT ADDRESS ENCODER

INPUT ADDRESS ENCODER

The MC14430 is an integrated circuit designed for program selection address in TV and radio receivers by means of push button switches.

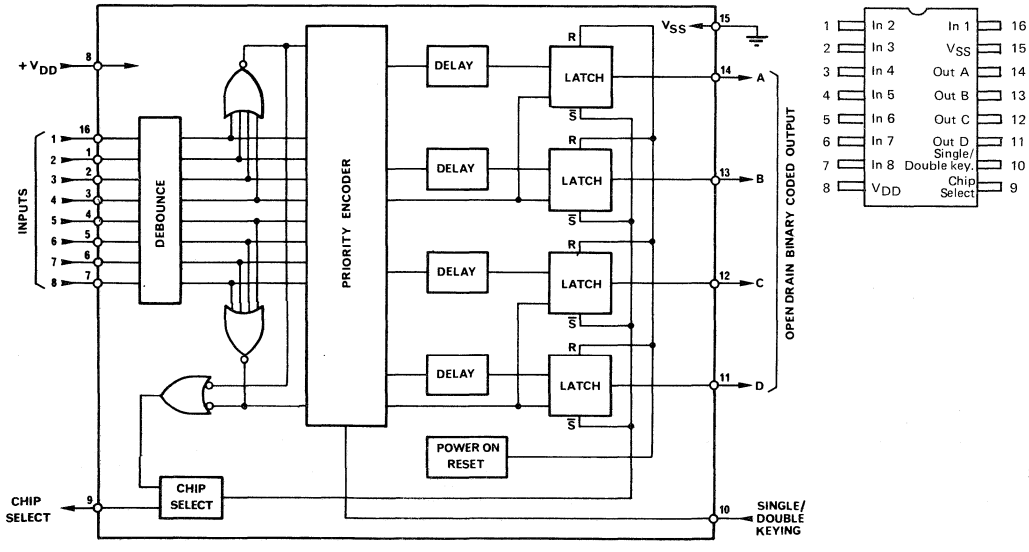
- 8 program inputs
- Binary coded open drain latched output
- Push button type keyboard allows for electrical isolation in live chassis applications
- Single or double keying operation possible
- Up to four circuits can be cascaded
- Normally closed or normally open switches can be used.



PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

FIGURE 1 – MC14430 BLOCK DIAGRAM & PIN-OUT



MAXIMUM RATINGS (T_A = 25 °C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+10 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

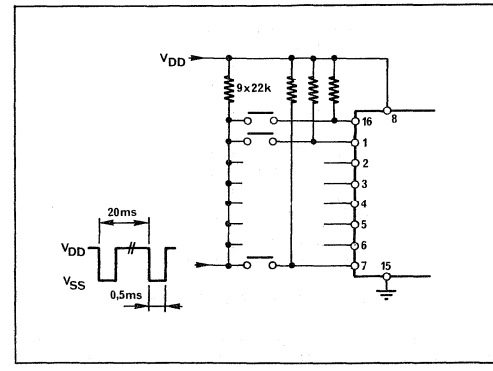
ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C)

Characteristics		Symbol	Min.	Typ.	Max.	Unit
Operating Supply Voltage		V_{DD}	4	5.2	6	Vdc
Quiescent Current per Package (Pins 16,1,2, 3,4,5,6,7 open or grounded)	V_{DD} = 5 V	I_{DD}	–	0.068	10	µAdc
Input Voltage	"O" Level "I" Level	V_{IL} V_{IH}	– 3.5	2.25 2.75	1.5 –	Vdc
Input Current	V_{DD} = 5 V V_{in} = 1 V V_{in} = 2 V V_{in} = 5 V	I_{in}	 – – –	 2.1 2.6 2.6	 – – 6.0	µAdc
Output Drive Current (V_{OL} = 0.5 V)	V_{DD} = 5 V	I_{OL}	2.5	6.2	–	mAdc
Output Drive Current (V_{OL} = 0.5 V)	V_{DD} = 5 V	I_{OL}	0.9	2.25	–	mAdc

APPLICATION INFORMATION

Incorrect encoding of the selected program number can occur whenever the last bounce, on opening a normally open switch, is 40 to 60 µsec. wide. Should the type of switch used have a characteristic within this timing, the switch configuration opposite is recommended.
By pulsing the common switch line at a rate lower than the whole bounce period (15 msec. max.), chances of misfunction are reduced.
Pulsing can be provided by a unijunction transistor relaxation oscillator or by a switching transistor driven by the vertical deflection flyback signal or others. The pulse width can vary between few hundred µsec. and few milliseconds.

FIGURE 2 – BOUNCE IMMUNE APPLICATION



APPLICATION INFORMATION

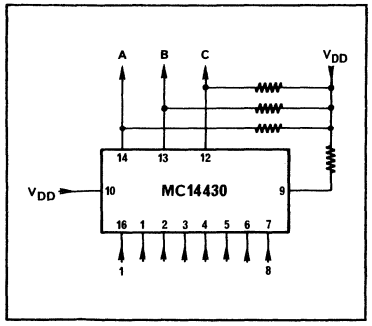


FIGURE 3 – 8 CHANNELS SINGLE KEYING

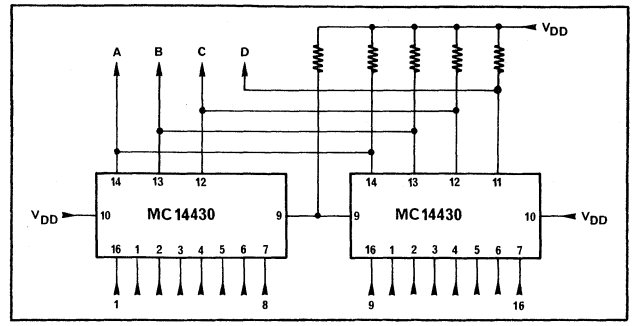


FIGURE 4 – 16 CHANNELS SINGLE KEYING

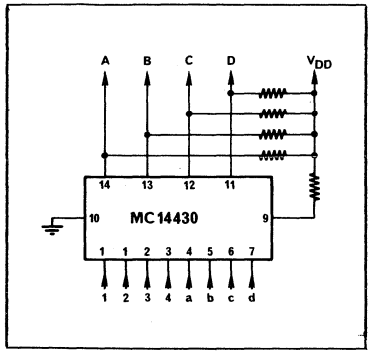


FIGURE 5 – 16 CHANNELS DOUBLE KEYING

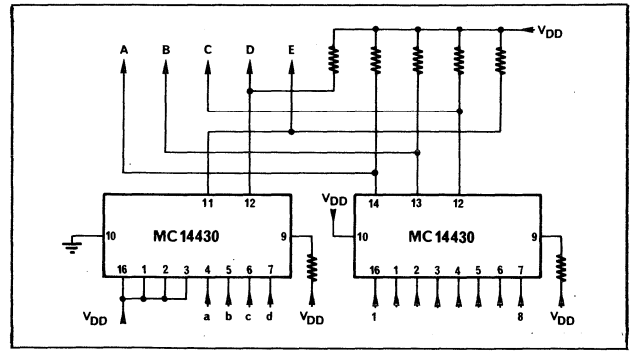
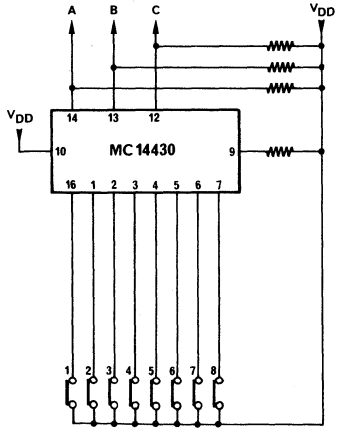
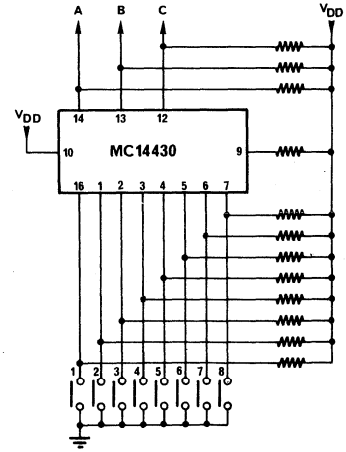


FIGURE 6 – 32 CHANNELS DOUBLE KEYING



ALL SWITCHES NORMALLY CLOSED



ALL SWITCHES NORMALLY OPEN

FIGURE 7 – PUSH BUTTON ELECTRICAL DIAGRAM

INPUT/OUTPUT FUNCTIONS

SINGLE/DOUBLE KEYING – Single Keying Mode (SKM) is selected by connecting pin 10 to V_{DD}. Double Keying Mode (DKM) is obtained by connecting pin 10 to ground.
In SKM, input pins: 16, 1, 2, 3, 4, 5, 6, 7 select programs 1 to 8 respectively. The corresponding binary coded output (000 for program 1) will appear on lines A, B, C. Output D (pin 11) is a chip select output and will remain activated (at V_{SS}) as long as the chip is selected. Refer to application information.
In DKM, keys are divided into two groups: keys 1, 2, 3, 4 (pin 16, 1, 2, 3) and keys a, b, c, d, (pin 4, 5, 6, 7) which affect output lines A, B, and C, D respectively (see application information).
Keying sequence is important since output lines A and B are reset every time a, b, c, d are actuated.
For example: program b3 is selected by keying b first, then 3. If key d is then actuated, program d1 is selected.

POWER ON RESET – When power is switched on, channel 1 (or channel 1a in DKM) will be automatically selected.

PRIORITY ENCODER – When two or more keys belonging to the same chip are activated simultaneously, the key having the lowest number will have priority and the corresponding code will be selected.
In Double Keying Mode, key 1 has priority over keys 2,3 and 4, key a has priority over keys b, c and d.

MULTI CHIP SYSTEM – As long as one key is activated the chip select pin 9 of the corresponding chip is pulled to ground.
That chip is now selected and any other chip connected in parallel will be disabled.
If two or more keys belonging to different chips are acutated at the same time, the chip corresponding to the first actuated key will be selected. When releasing the keys, the chip corresponding to the last released key will remain selected.

BINARY CODED OUTPUT – In SKM, binary coded program number minus one is present on lines A, B, C (pin 14, 13, 12).
Output D (pin 11) goes low when the corresponding chip is selected. In DKM the binary code output is present on lines A, B, C, D.

Circuit diagrams utilizing Motorola products are incuded as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14433

3½ DIGIT A/D CONVERTER

The MC14433 is a high performance, low power, 3½ digit A/D converter combining both linear CMOS and digital CMOS circuits on a single monolithic IC. The MC14433 is designed to minimize use of external components. With two external resistors and two external capacitors, the system forms a dual slope A/D converter with automatic zero correction and automatic polarity.

The MC14433 is ratiometric and may be used over a full-scale range from 1.999 volts to 199.9 millivolts. Systems using the MC14433 may operate over a wide range of power supply voltages for ease of use with batteries, or with standard 5 volt supplies. The output drive conforms with standard B-Series CMOS specifications and can drive a low-power Schottky TTL load.

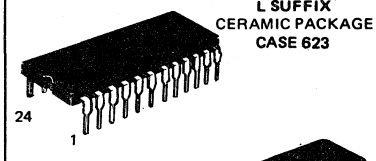
The high impedance MOS inputs allow applications in current and resistance meters as well as voltmeters. In addition to DVM/DPM applications, the MC14433 finds use in digital thermometers, digital scales, remote A/D, A/D control systems, and in MPU systems.

- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions/s
- Z_{in} > 1000 M ohm
- Auto-Polarity and Auto-Zero
- Single Positive Voltage Reference
- Standard B-Series CMOS Outputs—Drives One Low Power Schottky Load
- Uses On-Chip System Clock, or External Clock
- Low Power Consumption: 8.0 mW typical @ ±5.0 V
- Wide Supply Range: e.g., ±4.5 V to ±8.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Operates with LED and LCD Displays
- Low External Component Count

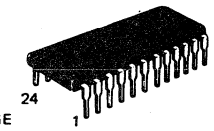
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

3½ DIGIT A/D CONVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 623

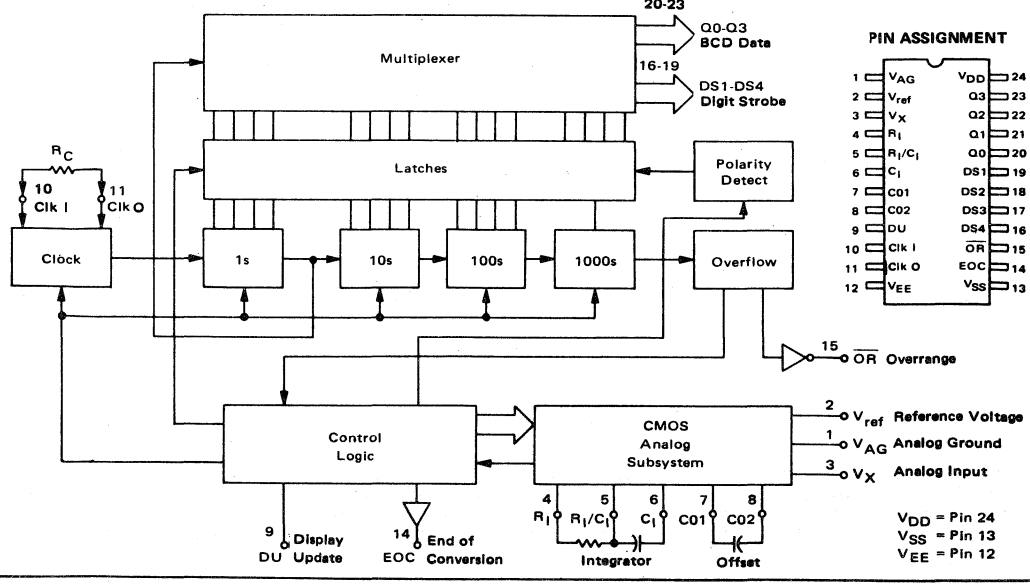


P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



PIN ASSIGNMENT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} to V_{EE}	-0.5 to +18	Vdc
Voltage, any pin, referenced to V_{EE}	V	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 or V_{EE})

Parameter	Symbol	Value	Unit
DC Supply Voltage — V_{DD} to Analog Ground V_{EE} to Analog Ground	V_{DD} V_{EE}	+5.0 to +8.0 -2.8 to -8.0	Vdc
Clock Frequency	f_{Clk}	32 to 400	kHz
Zero Offset Correction Capacitor	C_o	0.1 ± 20%	μF

ELECTRICAL CHARACTERISTICS (C_I = 0.1 μF mylar, R_I = 470 kΩ @ V_{ref} = 2.000 V, R_I = 27 kΩ @ V_{ref} = 200.0 mV, C_o = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1.)

Characteristic	Symbol	V_{DD} Vdc	V_{EE} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
Linearity-Output Reading (Note 1)	–										%rdg
(V_{ref} = 2.000 V)		5.0	-5.0	–	–	-0.05 -Count	±0.05	+0.05 +Count	–	–	
(V_{ref} = 200.0 mV)		5.0	-5.0	–	–	–	±0.05	–	–	–	
Stability-Output Reading (Note 2)	–										LSD
(V_X = 1.990 V, V_{ref} = 2.000 V)		5.0	-5.0	–	–	–	–	2	–	–	
(V_X = 199.0 mV, V_{ref} = 200.0 mV)		5.0	-5.0	–	–	–	–	3	–	–	
Zero-Output Reading (V_X = 0 V, V_{ref} = 2.000 V)	–	5.0	-5.0	–	–	–	0	0	–	–	LSD
Bias Current — Analog Input	–	5.0	-5.0	–	–	–	±20	±100	–	–	pAdc
Reference Input		5.0	-5.0	–	–	–	±20	±100	–	–	
Analog Ground		5.0	-5.0	–	–	–	±20	±500	–	–	
Common Mode Rejection (V_X = 1.4 V, V_{ref} = 2.000 V, f_{oc} = 32 kHz)	–	5.0	-5.0	–	–	–	65	–	–	–	dB
Output Voltage — Pins 14 to 23											Vdc
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	-5.0	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	-5.0	4.95	–	4.95	5.0	–	4.95	–	
(V_{SS} = -5.0 V) "0" Level	V_{OL}	5.0	-5.0	–	4.95	–	-5.0	-4.95	–	-4.95	
"1" Level	V_{OH}	5.0	-5.0	4.95	–	4.95	5.0	–	4.95	–	
Output Current — Pins 14 to 23											mAdc
(V_{SS} = 0 V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	-5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	-5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{SS} = -5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	-5.0	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OL} = -4.5 V) Sink	I_{OL}	5.0	-5.0	1.6	–	1.3	2.25	–	0.9	–	
Clock Frequency (R_C = 300 kΩ)	f_{Clk}	5.0	-5.0	–	–	–	66	–	–	–	kHz
Input Current — DU	I_{DU}	5.0	-5.0	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Quiescent Current	I_Q	5.0	-5.0	–	3.7	–	0.9	2.0	–	1.6	mAdc
(V_{DD} to V_{EE}, I_{SS} = 0)		8.0	-8.0	–	7.4	–	1.8	4.0	–	3.2	
DC Supply Rejection (V_{DD} to V_{EE}, I_{SS} = 0, V_{ref} = 2.000V)	–	5.0	-5.0	–	–	–	0.5	–	–	–	mV/V

Note 1: Accuracy — The accuracy of the meter at full scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full scale and zero is defined as the linearity specification.

Note 2: 3 LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.

TYPICAL CHARACTERISTICS

FIGURE 1 – TYPICAL ROLLOVER ERROR versus POWER SUPPLY SKEW

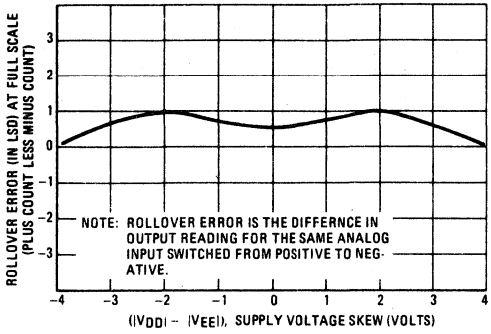


FIGURE 2 – TYPICAL QUIESCENT POWER SUPPLY CURRENT versus TEMPERATURE

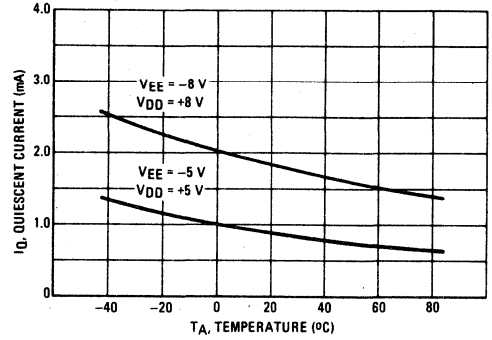


FIGURE 3 – TYPICAL N-CHANNEL SINK CURRENT AT VDD–VSS = 5 VOLTS

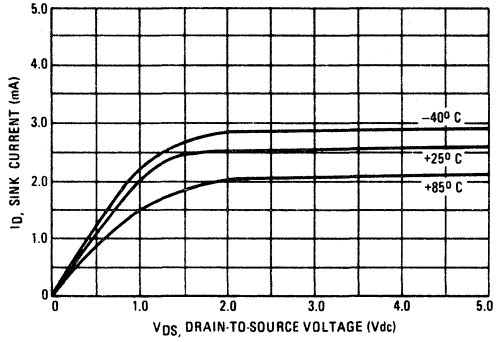


FIGURE 4 – TYPICAL P-CHANNEL SOURCE CURRENT AT VDD–VSS = 5 VOLTS

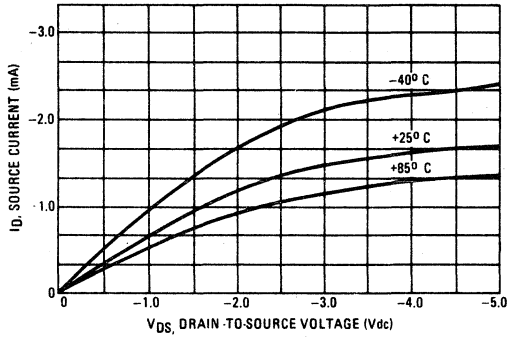


FIGURE 5 – TYPICAL CLOCK FREQUENCY versus RESISTOR (R_C)

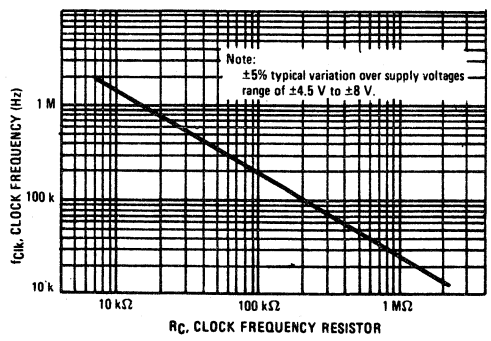
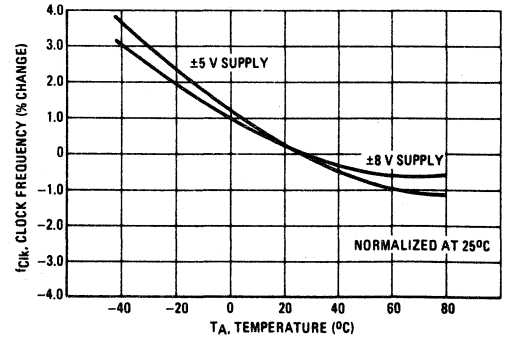


FIGURE 6 – TYPICAL % CHANGE OF CLOCK FREQUENCY versus TEMPERATURE



CONVERSION RATE = $\frac{\text{CLOCK FREQUENCY}}{16{,}400} \pm 1.5\%$
MULTIPLEX RATE = $\frac{\text{CLOCK FREQUENCY}}{80}$

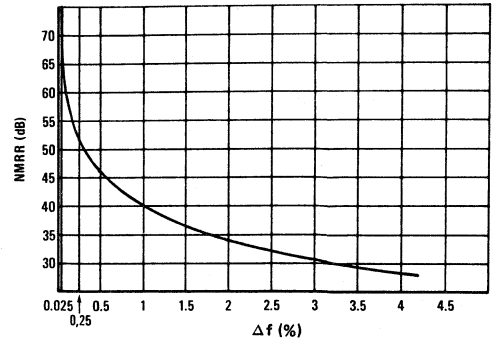
TYPICAL CHARACTERISTICS

FIGURE (Table) 7 – FOR BEST 50 Hz NMRR (Normal Mode Rejection Ratio) AT DIFFERENT CLOCK FREQUENCIES

Clock frequency (KHz)	Integration time (msec)	Conversion rate (~ Hz)
200	20	12.5
100	40	6.25
66.6	60	4.16
50	80	3.12
40	100	2.5

The NMRR depends on the difference Δf (%) between a multiple of the power line frequency and the clock frequency.

FIGURE 8 – NMRR (dB) vs Δf (%)



DEVICE OPERATION

ANALOG GROUND (V_{AG}, Pin 1)

Analog ground at this pin is the input reference level for the unknown input voltage (V_X) and reference voltage (V_{ref}). This pin is a high impedance input.

REFERENCE VOLTAGE (V_{ref}, Pin 2)
UNKNOWN INPUT VOLTAGE (V_X, Pin 3)

This A/D system performs a ratiometric A/D conversion; that is, the unknown input voltage, V_X, is measured as a ratio of the reference voltage, V_{ref}. The full scale voltage is equal to that voltage applied to V_{ref}. Therefore, a full scale voltage of 1.999 V requires a reference voltage of 2.000 V while full scale voltage of 199.9 mV requires a reference voltage of 200 mV. Both V_X and V_{ref} are high impedance inputs. In addition to being a reference input, pin 2 functions as a reset for the A/D converter. When pin 2 is switched to V_{EE} for at least 5 clock cycles, the system is reset to the beginning of a conversion cycle.

EXTERNAL COMPONENTS (R_I, R_I/C_I, C_I; Pins 4, 5, 6)

These pins are for external components for the integration used in the dual ramp A/D conversion. A typical value for the capacitor is 0.1 μF (mylar) while the resistor should be 470 kΩ for 2.0 V full scale operation and 27 kΩ for 200 mV full scale operation. These values are for a 66 kHz clock frequency which will produce a conversion time of approximately 250 ms. The equations governing the calculation for the values for integrator components are as follows:

$$R_I = \frac{V_X(max)}{C_I} \times \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X(max) - 0.5$$

$$T = 4000 \times \frac{1}{f_{Clk}}$$

where:

R_I is in kΩ
V_{DD} is the voltage at pin 24 referenced to V_{AG}
V_X is the voltage at pin 3 referenced to V_{AG}
f_{Clk} is the clock frequency at pin 10 in kHz

Example:

C_I = 0.1 μF
V_{DD} = 5.0 volts
f_{Clk} = 66 kHz
For $V_X(max)$ = 2.0 volts
R_I = 480 kΩ (use 470 kΩ ± 5%)
For $V_X(max)$ = 200 mV
R_I = 28 kΩ (use 27 kΩ ± 5%)

Note that for worst case conditions, the minimum allowable value for R_I is a function of C_I min, V_{DD} min, and f_{Clk} max. The worst-case condition does not allow $V + V_X$ to exceed V_{DD}. The 0.5 V factor in the above equation for ΔV is for safety margin.

OFFSET CAPACITOR (CO1, CO2; Pins 7, 8)

These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF.

DISPLAY UPDATE INPUT (DU, Pin 9)

If a positive edge is received on this input prior to the ramp-down cycle, new data will be strobed into the output latches during that conversion cycle. When this pin is wired directly to the EOC output (pin 14), every conversion will be displayed. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.

CLOCK (Clk I, Clk O, Pins 10, 11)

The MC14433 device contains its own oscillator system clock. A single resistor connected between pins 10 and 11 sets the clock frequency. If increased stability is desired, these pins will support a crystal or LC circuit. The clock input, pin 10, may also be driven from an external clock source which need have only standard CMOS output drive. For external clock inputs this pin is referenced to V_{EE}. A 300 kΩ resistor results in clock frequency of about 66 kHz. (See the typical characteristic curves.) For alternate circuits see Figure 7.

NEGATIVE POWER SUPPLY (V_{EE}, Pin 12)

This is the connection for the most negative power supply voltage. The typical current is 0.8 mA. Note the current for the output drive circuit is not returned through this pin, but through pin 13.

NEGATIVE POWER SUPPLY FOR OUTPUT CIRCUITRY (V_{SS}, Pin 13)

This is the low voltage level for the output pins of the MC14433 (BCD, Digit Selects, EOC, $\overline{OR}$). When this pin is connected to analog ground, the output voltage is from analog ground to V_{DD}. When connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The allowable operating range for V_{SS} is between V_{DD} – 3.0 volts and V_{EE}.

END OF CONVERSION (EOC, Pin 14)

The EOC output produces a pulse at the end of each conversion cycle. This pulse width is equivalent to one half the period of the system clock (pin 11).

OVERRANGE ($\overline{OR}$, Pin 15)

The $\overline{OR}$ pin is low when V_X exceeds V_{ref}. Normally it is high.

DIGIT SELECT (DS4, DS3, DS2, DS1; Pins 16, 17, 18, 19)

The digit select output is high when the respective

digit is selected. The most significant digit (½ digit) turns on immediately after an EOC pulse followed by the remaining digits, sequencing from MSD to LSD. An interdigit blanking time of two clock periods is included to ensure that the BCD data has settled. The multiplex rate is equal to the clock frequency divided by 80. Thus, with a system clock rate of 66 kHz, the multiplex rate would be 0.8 kHz. Relative timing among digital select ouptut and EOC signals is shown in the Digit Select Timing Diagram, Figure 8.

BCD DATA OUTPUTS (Q0, Q1, Q2, Q3, Pins 20, 21, 22, 23)

Multiplexed BCD outputs contain 3 full digits of information during DS2, 3, 4, while during DS1, the ½ digit, overrange, underrange and polarity are available. The adjacent truth table shows the formats of the information during DS1.

POSITIVE POWER SUPPLY (V_{DD}, Pin 24)

The most positive supply voltage pin.

TRUTH TABLE

Coded Condition of MSD	Q3	Q2	Q1	Q0	BCD to 7 Segment Decoding
+0	1	1	1	0	Blank
−0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
−0 UR	1	0	1	1	Blank
+1	0	1	0	0	4 → 1 } Hook up
−1	0	0	0	0	0 → 1 } only seg b
+1 OR	0	1	1	1	7 → 1 } and c to
−1 OR	0	0	1	1	3 → 1 } MSD

Notes for Truth Table
Q3 – ½ digit, low for "1", high for "0"
Q2 – Polarity: "1" = positive, "0" = negative
Q0 – Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 → OR or Q3 = 1 → UR.

When only segment b and c of the decoder are connected to the ½ digit of the display, 4, 0, 7 and 3 appear as 1.

The overrange indication (Q3 = 0 and Q0 = 1) occurs when the count is greater than 1999, e.g., 1.999 V for a reference of 2.000 V. The underrange indication, useful for autoranging circuits, occurs when the count is less than 180, e.g., 0.180 V for a reference of 2.000 V.

Caution: If the most significant digit is connected to a display other than a "1" only; such as a full digit display, segments other than b and c must be disconnected. The BCD to seven segment decoder must blank on BCD inputs 1010 to 1111.

FIGURE 7 – ALTERNATE OSCILLATOR CIRCUITS

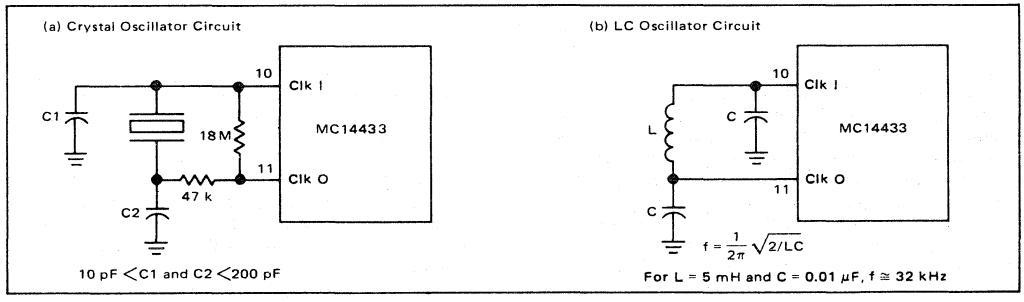


FIGURE 8 – DIGIT SELECT TIMING DIAGRAM

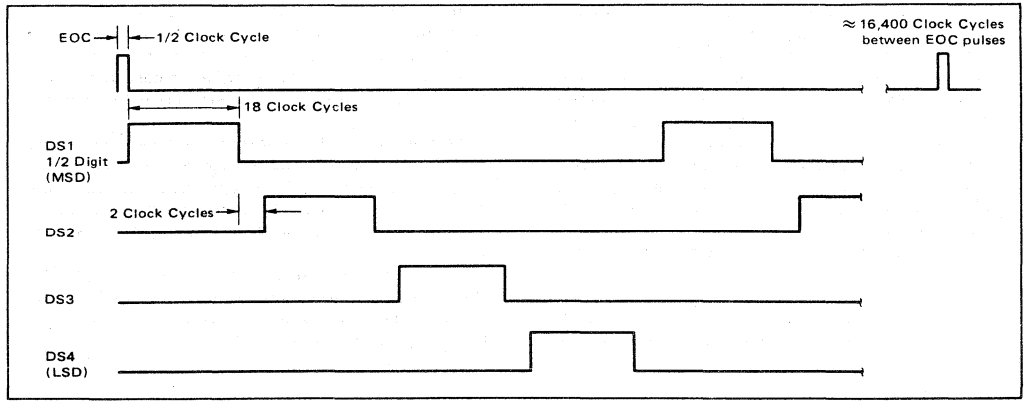


FIGURE 9 – INTEGRATOR WAVEFORMS AT PIN 6

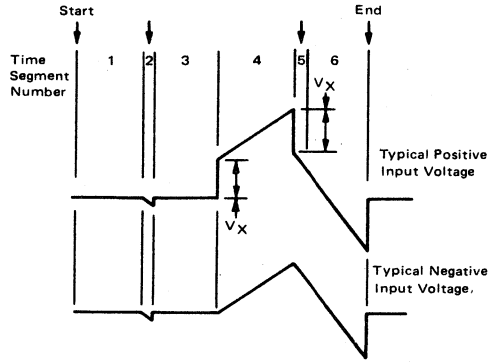
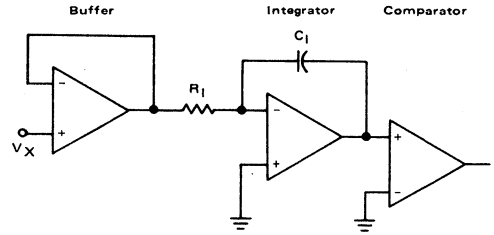


FIGURE 10 – EQUIVALENT CIRCUIT DIAGRAMS OF THE ANALOG SECTION DURING SEGMENT 4 OF THE TIMING CYCLE



CIRCUIT OPERATION

The MC14433 CMOS integrated circuit, together with a minimum number of external components, forms a modified dual ramp A/D converter. The device contains the customary CMOS digital logic providing counters, latches, and multiplexing circuitry as well as the CMOS analog circuitry providing operational amplifiers and comparators required to implement a complete single chip A/D. Autozero, high input impedances, and autopolarity are features of this system. Using CMOS technology, an A/D with a wide range of power supply voltage and low power consumption is now available with the MC14433.

During each conversion, the offset voltages of the internal amplifiers and comparators are compensated for by the system's autozero operation. Also each conversion 'ratiometrically' measures the unknown input voltage. In other words, the output reading is the ratio of the unknown voltage to the reference voltage with a ratio of 1 equal to the maximum count 1999. The entire conversion cycle requires slightly more than 16000 clock periods and may be divided into six different segments. The waveforms showing the conversion cycle with a positive input and a negative input are shown in Figure 9. The six segments of these waveforms are described below.

Segment 1 – The offset capacitor (C_O), which compensates for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. Also, the integrator capacitor is shorted. This segment requires 4000 clock periods.

Segment 2 – The integrator output decreases to the comparator threshold voltage. At this time a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the autozero process. The time for this segment is variable, and less than 800 clock periods.

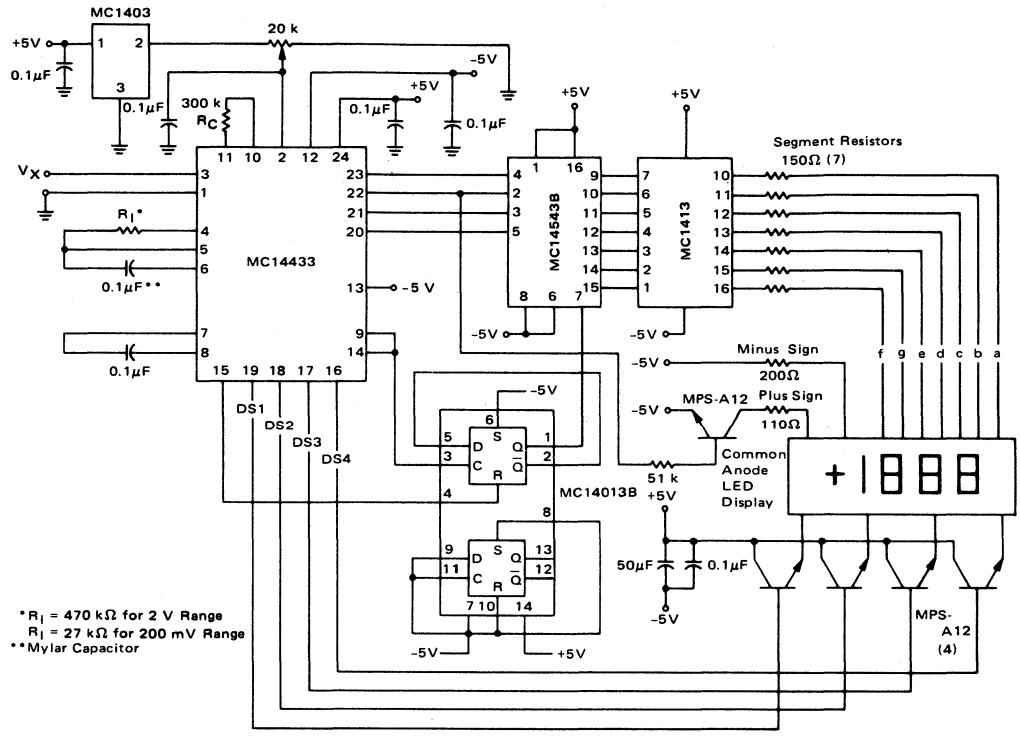
Segment 3 – This segment of the conversion cycle is the same as Segment 1.

Segment 4 – Segment 4 is an up-going ramp cycle with the unknown input voltage (V_X) as the input to the integrator. Figure 10 shows the equivalent configuration of the analog section of the MC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

Segment 5 – This segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 – This is an extension of Segment 5. The time period for this portion is 4000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

FIGURE 11 – 3-1/2 DIGIT VOLTMETER–COMMON ANODE DISPLAYS, FLASHING OVERRANGE



APPLICATIONS INFORMATION

3½ DIGIT VOLTMETER – COMMON ANODE DISPLAYS, FLASHING OVERRANGE

An example of a 3½ digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 11. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_I is also changed, as shown on the diagram.

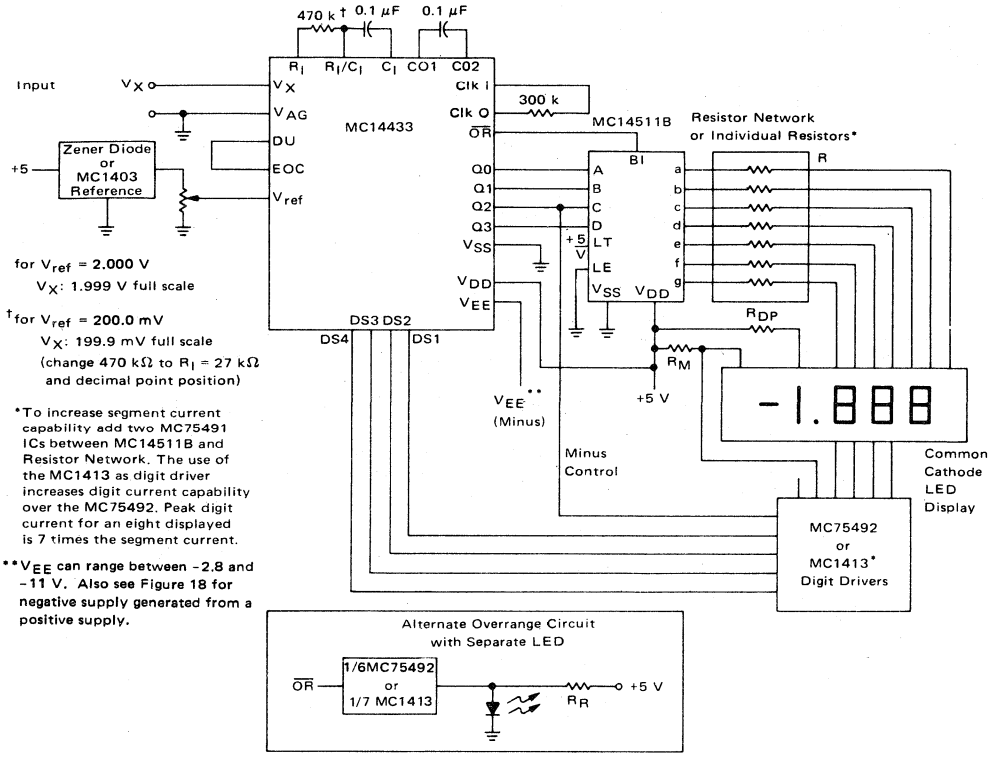
When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with ½ MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 darlington transistors operating in an emitter follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in the above figure.

The power supply for the system is shown as a dual ±5 V supply. However, the MC14433 will operate over a wide range of voltages, and balance between the +5 and –5 V supplies is *not* required. See the recommended operating conditions and Figure 1, on pages 2 and 3.

FIGURE 12 – 3½ DIGIT VOLTMETER WITH LOW COMPONENT COUNT



3½ DIGIT VOLTMETER WITH LOW COMPONENT COUNT USING COMMON CATHODE DISPLAYS

The 3½ digit voltmeter of Figure 12 is an example of the use of the MC14433 in a system with a minimum of components. This circuit uses only 11 components in addition to the MC14433 to operate the MC14433 and drive the LED displays.

In this circuit the MC14511B provides the segment drive for the 3½ digits. The MC75492 or MC1413 provides sink for digit current. (The MC75492 or MC1413 are devices with 6 or 7 darlingtons respectively with common emitters.) The worst case digit current is 7 times the segment current at ¼ duty cycle. The peak segment current is limited by the value of R. The current for the display flows from V_{DD} (+5 V) to ground and does not flow through the V_{EE} (negative) supply. The minus sign is controlled by one section of the MC75492 or MC1413 and is turned off by shunting the current through R_M to ground, bypassing the minus sign LED. The minus sign is derived from the Q2 output. The decimal point brightness is controlled by resistor R_{DP}. Since the brightness and the type and size of LED display are the choice of the designer, the values of resistors R, R_M, R_{DP}, and R_R that govern brightness are not given.

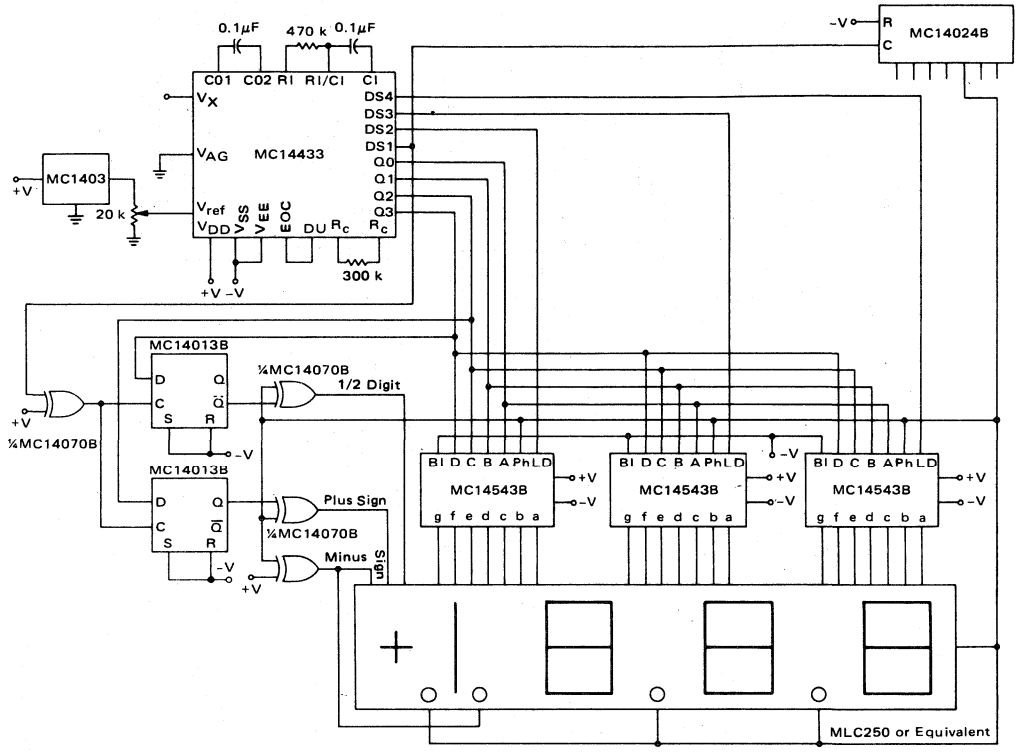
During an overrange condition the 3½ digit display is blanked at the BI pin on the MC14511B. The decimal point and minus sign will remain on during a negative overrange condition. In addition, an alternate overrange circuit with separate LED is shown. There are leftover sections in either the MC75492 or MC1413.

3½ DIGIT VOLTMETER WITH LCD DISPLAY

A circuit for a 3½ digit voltmeter with a liquid crystal display is shown in Figure 13. Three MC14543B LCD latch/decoder/display drivers are used to demultiplex, decode the three digits, and drive the LCD. The half digit and polarity are demultiplexed with the MC14013B dual D flip-flop.

Since the LCD is best driven by an ac signal across the LCD, the low-frequency square wave drive for the LCD is derived from the MC14024B binary counter which divides the digit select output from the A/D. This low frequency square wave is connected to the backplane of

FIGURE 13 – 3½ DIGIT VOLTMETER WITH LCD DISPLAY



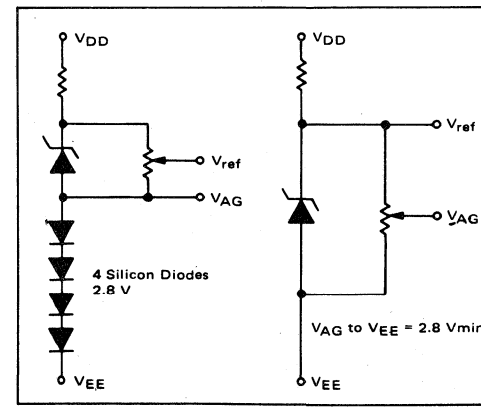
the LCD and to the individual segments through the combination of the output circuitry of the MC14543B and the exclusive OR gates at the outputs of the MC14013B. Alternatively the square wave can be derived from a 50/60 Hz input signal when available.

The minus sign and the decimal point to the right of the half digit are connected to the inverted low frequency square wave signal. Unused decimal points are tied directly to the low frequency square wave.

The system shown operates from two power supplies (plus and minus). Alternatively one supply can be used when V_{SS} is connected to V_{EE}. In this case a level must be set for analog ground, V_{AG}, which must be at least 2.8 V above V_{EE}. This circuit may be implemented with a resistor network, resistor/forward-biased diode network or resistor-zener diode network. For example, a 9 V supply can be used with 3 V between V_{AG} and V_{EE}, leaving 6 V for V_{DD} to V_{AG}. This system leaves a comfortable margin for battery degeneration (end of life). Two versions of this circuit for single supply operation is shown in Figure 14.

For panel meter operation from a single 5 V supply, a negative supply can be generated as shown in Figure 18.

FIGURE 14 – TWO CIRCUITS FOR GENERATION OF V_{ref} AND V_{AG} FROM A SINGLE SUPPLY



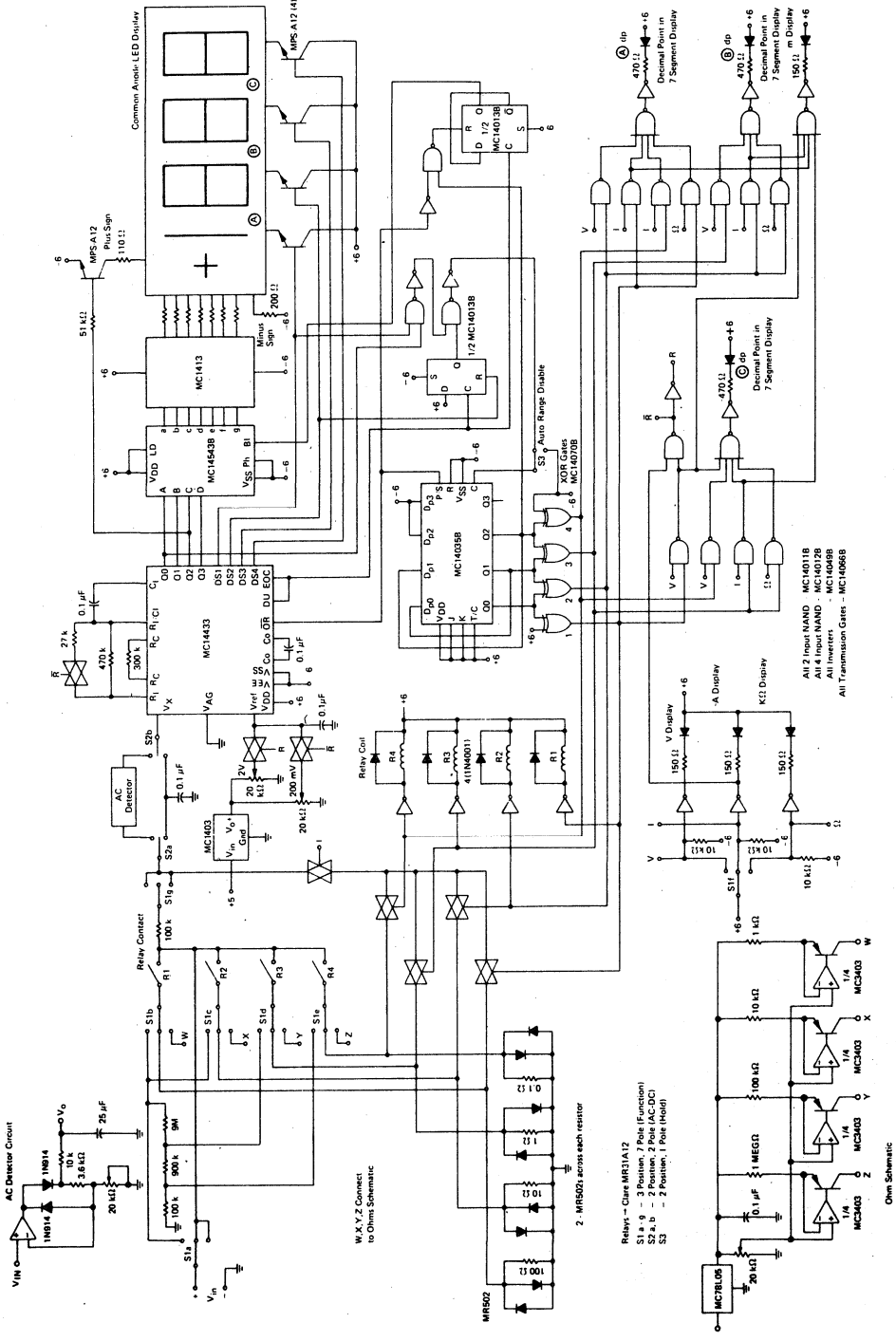


FIGURE 15 – 3½ DIGIT AUTORANGING MULTIMETER

3½ DIGIT AUTORANGING MULTIMETER

An autoranging multimeter including ac and dc voltage ranges from 200 mV to 200 V, ac and dc current from 2 mA to 2 A fullscale and resistance ranges from 2 kΩ to 2 MΩ fullscale is shown in Figure 15. In this multimeter only two input jacks are required for all ranges and functions, eliminating the need for changing leads on the instrument when changing ranges or functions. Although only four ranges are provided for each function, the technique used may be expanded to more ranges if desired. Range switching uses mechanical relays. However, the relays may be replaced with solid state analog switches.

The MC14433 provides the overrange and underrange control signals for the automatic ranging circuits. For additional information, see Motorola Application Note AN-769, "Autoranging Digital Multimeter Using the MC14433 CMOS A/D Converter."

PARALLEL BCD DATA OUTPUT CIRCUIT

The output of the MC14433 may be demultiplexed to produce parallel BCD data as shown in Figure 16. Two levels of latches are required for a complete demultiplexing of the data since the outputs of the MC14042B latches change sequentially with the DS1 to DS4 strobe pulses. To key output validity to one leading edge, i.e., that of the EOC signal of the MC14433, information is transferred to the second set of latches (MC14175B latches). A single set of latches can be used when reading of output is restricted to within 12,000 clock pulses after EOC. This requires synchronous system operation with respect to the BCD data bus.

In this system the output ground level is V_{SS}. In most cases, a two supply system with V_{SS} connected to V_{AG} is recommended. This allows connecting analog ground and digital ground together without destroying a power supply. This circuit works well with that of Figure 12.

FIGURE 16 – DEMULTIPLEXING FOR MC14433 BCD DATA

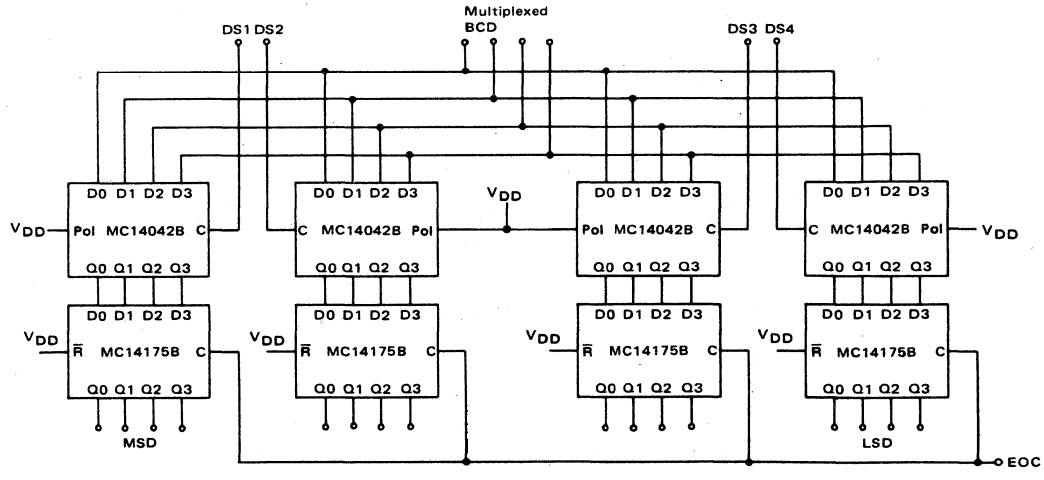
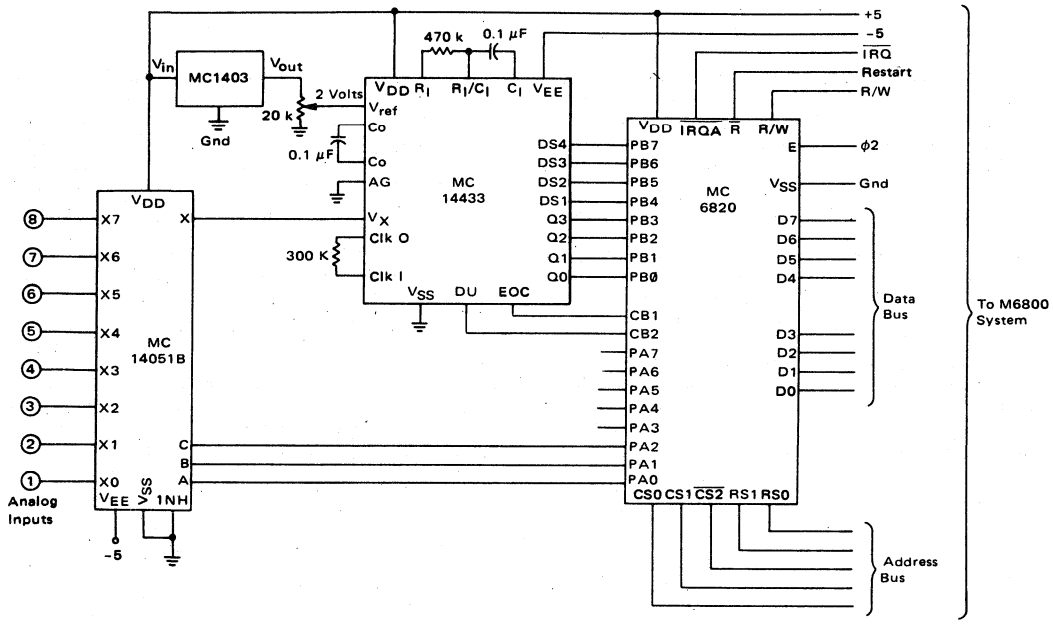


FIGURE 17 – CHANNEL DATA ACQUISITION HARDWARE

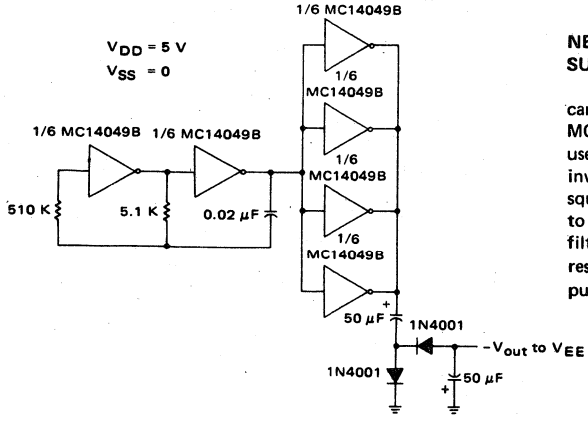


8 CHANNEL DATA ACQUISITION NETWORK

Figure 17 shows an 8 channel data acquisition network using the MC14433 and an M6800 microprocessor system. The interface between the microprocessor data bus and the A/D system is done with an MC6820 PIA. One half of the PIA is used with the BCD and digit select outputs of the MC14433, while the second half of the PIA selects the channel to be measured via the MC14051B analog multiplexer. Control lines CB1 and CB2 are used for data flow control and are connected to DU and EOC of the MC14433.

A more detailed explanation of this system including the actual software required for the M6800 microprocessor may be found in Motorola Application Note AN-770, "Data Acquisition Networks With NMOS and CMOS."

FIGURE 18 – NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY



NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY

When only +5 V is available, a negative supply voltage can be generated with the circuit of Figure 18 using one MC14049B. Two inverters from CMOS hex inverter are used as an oscillator (≈ 3 kHz) with the remaining inverters used as buffers for higher current output. The square wave output from the oscillator is level-translated to a negative going signal. This signal is rectified and filtered. A V_{DD} voltage of +5 V for the hex buffer will result in a -4.3 V no load output voltage while the output with a 2 mA load is ≈ 3.4 V.

MOTOROLA

MC14435

Advance Information

3-1/2 DIGIT A/D LOGIC SUBSYSTEM

The MC14435 A/D Logic is designed specifically for use in a dual-slope integration A/D converter system.

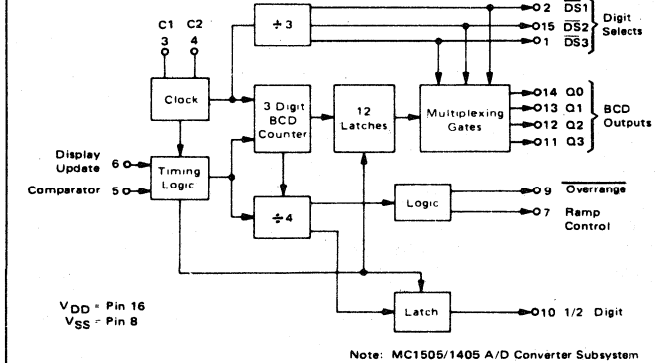
The device consists of 3-1/2 digits of BCD counters, 13 memory latches, and output multiplexing circuitry. An internal clock oscillator is provided to generate system timing and to set the output multiplexing rate. A single capacitor is required to set the oscillator frequency.

- On-Chip Clock to Control Digit Select, Multiplexing, and BCD Counters Simultaneously
- Multiplexed BCD Output
- Built-In 100-Count Delay for Accurate System Conversion of Low-Level Inputs
- System Over-Range Output
- Linear Companion Device Available From Motorola (MC1405L/1505L)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14435EFL/FL/FP)
  = 3.0 Vdc to 6.0 Vdc (MC14435EVL/VL/VP)

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage – MC14435EFL/FL/FP – MC14435EVL/VL/VP	V_{DD}	 +18 to -0.5 +6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range MC14435EFL/EVL MC14435FL/FP/VL/VP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



Note: MC1505/1405 A/D Converter Subsystem recommended for linear front end.

This is advance information and specifications are subject to change without notice.

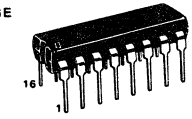
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

3-1/2 DIGIT A/D LOGIC SUBSYSTEM

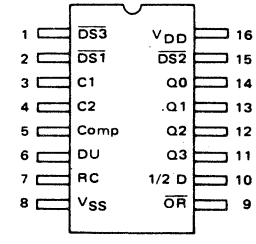


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



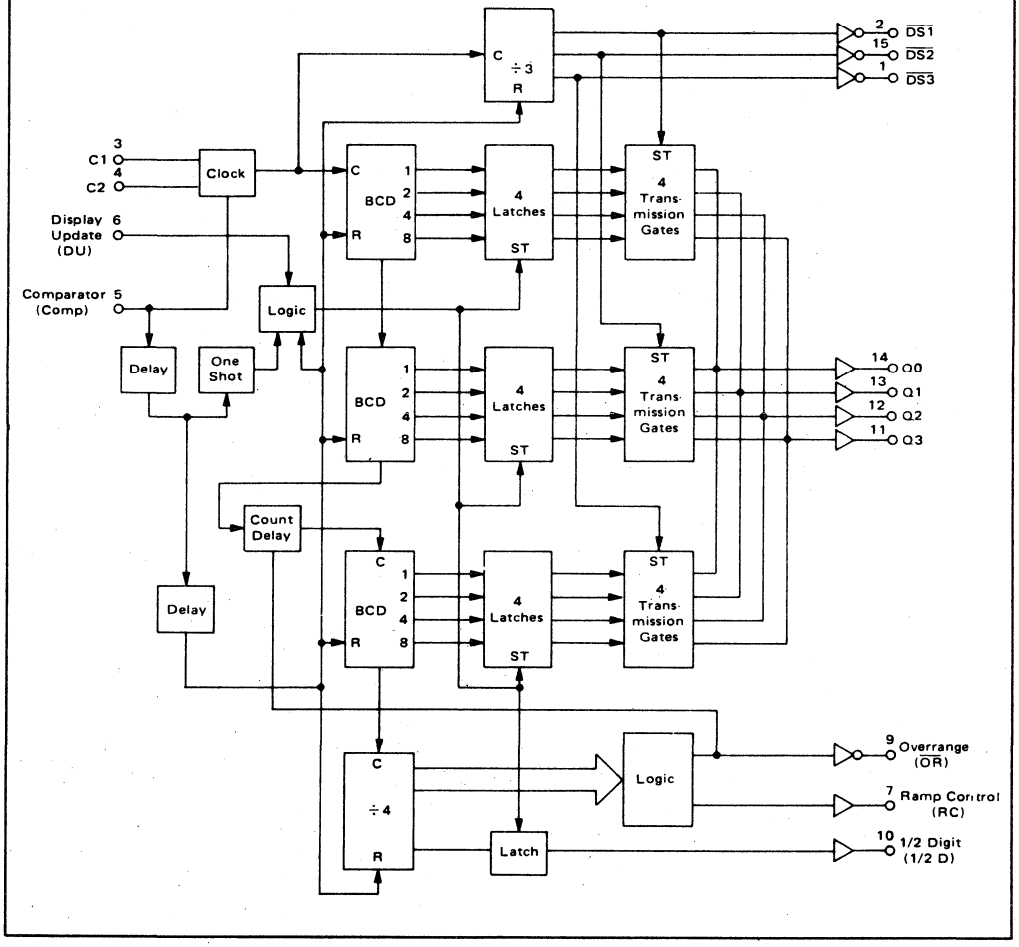
ORDERING INFORMATION

MC14435 — Suffix — Denotes

Suffix	Denotes
L	Ceramic Package
P	Plastic Package
F	*Extended Operating Voltage Range
V	*Limited Operating Voltage Range
Blank	**Standard Operating Temperature Range
E	**Extended Operating Temperature Range

*See Features (above, left)
**See Maximum Ratings

FUNCTIONAL DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}** Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.10	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.90	–	
Noise Immunity	V_{NL}									Vdc
($\Delta V_{out} \leq 1.5$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 3.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 4.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 1.5$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 3.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 4.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current	I_{OH}									mAdc
Source – All outputs										
(V_{OH} = 2.5 Vdc)		5.0	-0.23	–	-0.20	-1.35	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.64	–	-0.14	–	
(V_{OH} = 13.5 Vdc)		15	-0.23	–	-0.20	-2.35	–	-0.14	–	
Sink – $\overline{DS1}$, $\overline{DS2}$, $\overline{DS3}$	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		5.0	1.60	–	1.60	3.45	–	1.12	–	
(V_{OL} = 0.5 Vdc)		10	2.55	–	2.15	6.50	–	1.50	–	
(V_{OL} = 1.5 Vdc)		15	8.35	–	7.0	21.0	–	4.90	–	
Sink – Q0, Q1, Q2, Q3	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		5.0	1.60	–	1.60	2.55	–	1.12	–	
(V_{OL} = 0.5 Vdc)		10	2.25	–	1.90	5.80	–	1.35	–	
(V_{OL} = 1.5 Vdc)		15	7.20	–	6.0	18.5	–	4.20	–	
Sink – 1/2D, RC, $\overline{OR}$	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		5.0	0.23	–	0.20	0.64	–	0.14	–	
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	1.57	–	0.35	–	
(V_{OL} = 1.5 Vdc)		15	2.15	–	1.8	5.5	–	1.25	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q									mW
(Comp Input Low)		5.0	–	2.15	–	0.40	1.75	–	1.75	
		10	–	8.50	–	1.60	6.85	–	6.85	
		15	–	19.50	–	3.6	15.75	–	15.75	
Dynamic Power Dissipation	P_D									mW
(Comp Input High)		5.0	–	12.4	–	2.0	10	–	10	
		10	–	62.0	–	16.7	50	–	50	
		15	–	248	–	66.7	200	–	200	

*T_{low} = -55°C for MC14435 EFL, EVL; -40°C for MC14435FL, FP, VL, VP.
T_{high} = +125°C for MC14435 EFL, EVL; +85°C for MC14435 FL, FP, VL, VP.
**Only 5 volt specifications apply to MC14435 EVL, VL, VP devices.

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Typical All Types	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	100 50 40	ns
Propagation Delay Time (Comp to all Outputs)	t_{PLH}, t_{PHL}	5.0 10 15	14 5.0 3.0	μs
Propagation Delay Time (Clock to RC)	t_{PLH}, t_{PHL}	5.0 10 15	2.4 1.0 0.75	μs
Propagation Delay Time (Clock to Digit Selects or Q outputs)	t_{PLH}, t_{PHL}	5.0 10 45	2.2 0.85 0.65	μs
Display Update Pulse Width	t_{WH}	5.0 10 15	230 90 65	ns
Comparator Pulse Width (Low State)	t_{WL}	5.0 10 15	11.5 4.5 2.5	μs

OPERATING CHARACTERISTICS

The MC14435 contains the clock, BCD counters, latches, BCD multiplexing, and control circuitry for a 3-1/2 digit A to D converter. In conjunction with the MC1505 analog subsystem a multiplexed A to D can be implemented in three 16-pin packages as shown in Figure 5.

Two connections are required between the analog subsystem (MC1505) and the logic subsystem (MC14435). These two connections are the comparator input (Comp) and the ramp control output (RC) of the MC14435. The clock and counters operate whenever the comparator line is high. After 1000 counts from the clock, the RC output goes high, switching the integrator input from the unknown current to the reference current. When the integrator output falls below the threshold level the comparator line goes low, inhibiting the clock and ending the conversion cycle. The BCD content of the counters is then strobed into the latches, the counters reset, and the conversion cycle starts over.

After the RC line goes high, the next 100 pulses are subtracted, compensating for the offset produced by the analog subsystem. The three BCD latch outputs are multiplexed into a single 4-line output. The multiplex frequency

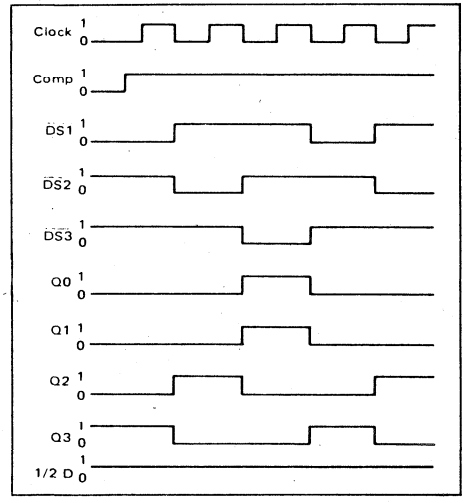
is the same as the clock frequency.

The internal oscillator requires a capacitor between pins 3 and 4. Figure 1 shows a curve of output frequency versus capacitance value for determining the desired system clock frequency. An external clock oscillator may be used by removing the clock capacitor and connecting the external signal to pin 3 (negative edge trigger), or pin 4 (positive edge trigger).

The Display Update input (DU) is used to control the rate of display of the BCD multiplexed outputs. If the DU input is held high, the system makes conversions continuously and strobes each conversion into the memory latches to be multiplexed out. If the DU input is held low, after one conversion has been entered into the latches, all other conversions will be blocked from entering. By synchronizing the DU input with the system clock, the rate of displayed output updating can be controlled.

The 3-digit multiplexed BCD pins 11, 12, 13, and 14 are low for a BCD word of "zero", while the digit select lines are normally high and go low for the individual digit selection. The half-digit output (pin 10) is in the logic "1" state whenever the input voltage is greater than 1.0 volt. When the input voltage is greater than 2.0 volts, pin 9 goes low after 2100 counts are reached during the ramp down portion of the conversion cycle, or 3100 total counts. The overrange ($\overline{OR}$) pin remains in this condition until the counters are reset and the next conversion cycle starts.

OUTPUT MULTIPLEX TIMING DIAGRAM



FUNCTIONAL TRUTH TABLE

INPUTS		FUNCTION
Comp	DU	
0	X	BCD Counter is held reset to "0". Digit Select Counter is held reset to $\overline{DS1}$. Previous count is held in latches. Clock oscillator is inhibited, RC and $\overline{OR}$ are held reset.
⌐	X	Clock oscillator starts BCD counter begins counting clock. Digit Select counter runs, operating output multiplexing. Previous count is held in latches.
⌐	1	Clock oscillator is inhibited. New count is strobed from the first BCD Counter into latches. BCD counters are reset. Digit select counter is reset to $\overline{DS1}$. RC and $\overline{OR}$ are reset.
⌐	0	The first negative edge of Comp after DU is brought low produces the same results as if DU was high. On subsequent cycles of Comp the Clock oscillator, BCD counters, and Digit Select counter operate normally, but no further latch strobes occur. RC and $\overline{OR}$ are reset.

X = Don't Care

FIGURE 1 – TYPICAL OSCILLATOR FREQUENCY versus EXTERNAL CAPACITOR VALUE

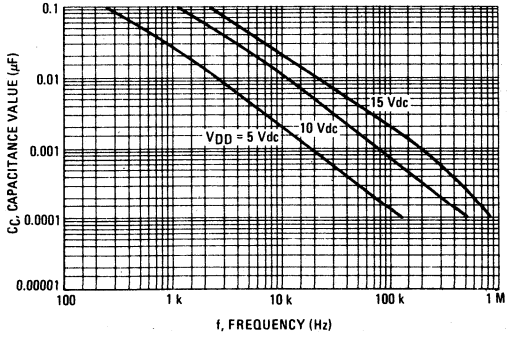
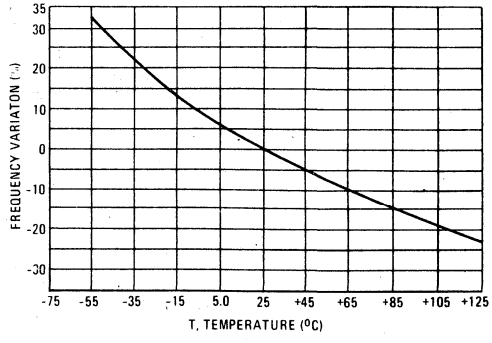


FIGURE 2 – TYPICAL OSCILLATOR FREQUENCY VARIATION versus TEMPERATURE



APPLICATION INFORMATION

The dual ramp A to D system is an integrating converter whose output is relatively independent of both clock frequency and integrator capacitor value. The timing diagram shows a typical conversion cycle for the dual ramp system. A block diagram of the basic system is shown in Figure 3 of the data sheet. The up ramp voltage is created by charging an integrator capacitor with a constant current whose value is proportional to the unknown input voltage. This time period (T1) lasts for a fixed number of clock pulses, which in the case of the MC14435 is 1000 clock pulses. The voltage on the output of the integrator at this point is proportional to the input voltage. After this fixed time period the ramp direction is reversed by switching the integrator capacitor input to a reference current which is the opposite polarity of the input current. The integrator capacitor is discharged until the output voltage reaches the comparator threshold value. This variable time period (T2) is proportional to the unknown input voltage. The unknown input voltage is the product of the reference voltage and the ratio of T2 to T1 or $T2 = T1 \frac{V_X}{V_R}$.

When the input voltage to the basic dual ramp system is zero or near zero the integrator current during the ramp up time period is zero or near zero. In this case the ramp down period would be very short. Thus any noise in the system could cause delay in the comparator line going low and cause instability in low voltage readings. The problem is eliminated by adding a fixed offset current to the unknown current and subtracting out the equivalent number of counts in the digital counters to compensate for the offset current. With this technique the A to D always has at least a minimum number of counts on the counters with a zero input voltage. In the case of the MC14435 the number of pulses subtracted out is 100 pulses; e.g., the down ramp is 100 pulses longer than T2.

For additional information consult the MC1505 (Analog Subsystem) data sheet.

FIGURE 3 – BASIC DUAL RAMP SYSTEM

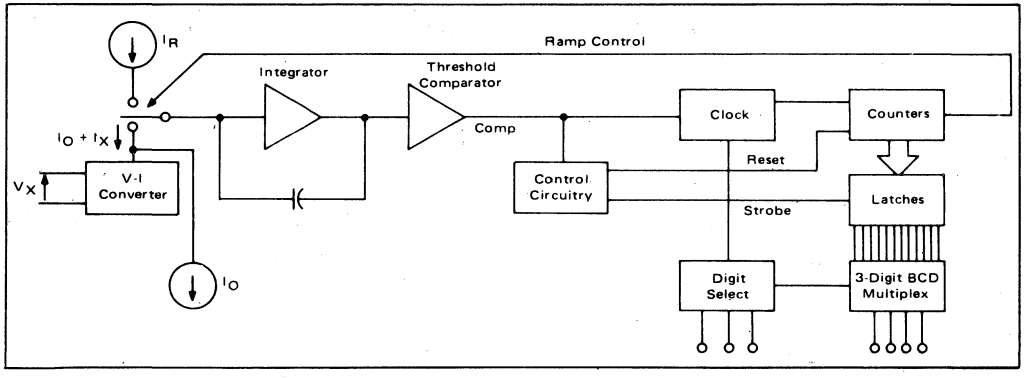


FIGURE 4 – DUAL SLOPE A/D CONVERTER SYSTEM TIMING DIAGRAM

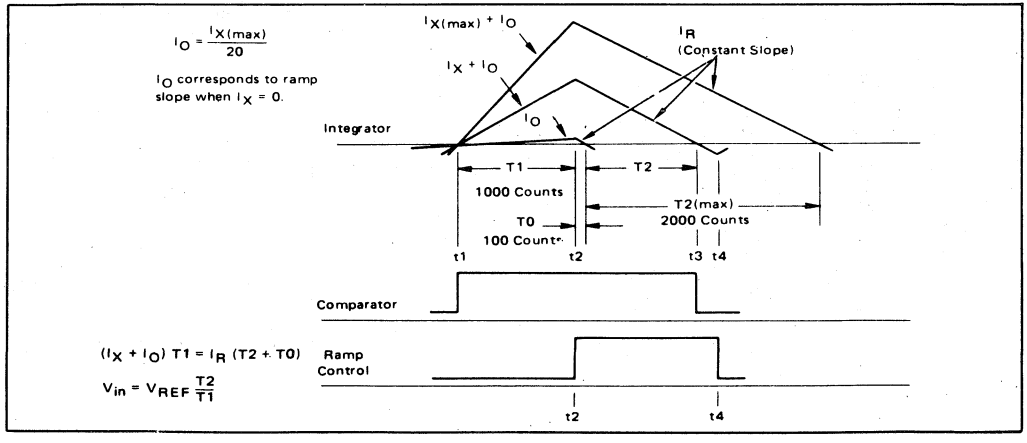
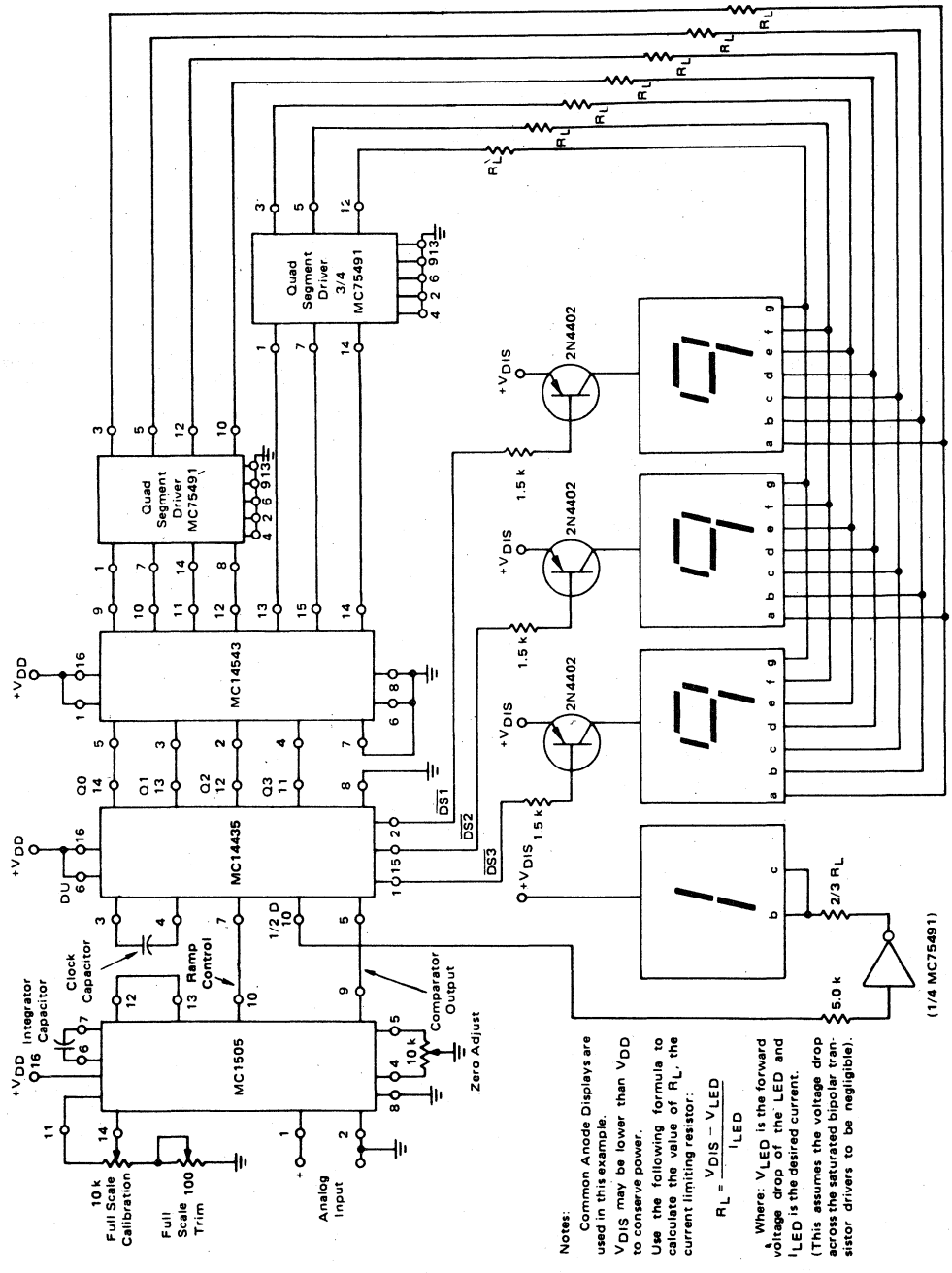


FIGURE 5 – TYPICAL A/D SYSTEM INCLUDING DRIVERS AND LED DISPLAYS



Notes:
Common Anode Displays are used in this example.
V_{DIS} may be lower than V_{DD} to conserve power.
Use the following formula to calculate the value of R_L, the current limiting resistor:

$$R_L = \frac{V_{DIS} - V_{LED}}{I_{LED}}$$

Where: V_{LED} is the forward voltage drop of the LED and I_{LED} is the desired current.
(This assumes the voltage drop across the saturated bipolar transistor drivers to be negligible).

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14443
MC14447

Advance Information

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

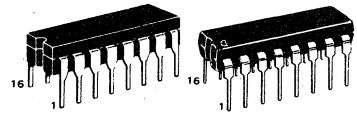
MICROPROCESSOR BASED
ANALOG TO DIGITAL CONVERTER

ANALOG TO DIGITAL CONVERTER LINEAR SUBSYSTEM

The MC14443 and the MC14447 devices are 6 channel, single slope, 8–10 bit analog to digital converter linear subsystems for microprocessor based data and control, systems. Contained in both devices are a one of 8 decoder, an 8 channel analog multiplexer, a buffer amplifier, a precision voltage to current converter, a ramp start circuit, and a comparator. The output driver of the MC14443 comparator is an open-drain N-channel capable of sinking up to 5 mA of current. The output of the MC14447 comparator has a standard B-Series P-channel, N-channel pair.

A processor system (such as the MC6800, MC141000 or MC3870) provides the addressing, timing, counting, and arithmetic operations required for implementing a full analog to digital converter system. A system made up of a processor and the linear subsystem has features such as automatic zeroing and variable scaling (weighting) of six separate analog channels.

- Quiescent Current 0.8 mA Typical at V_{DD} = 5 V
- Single Supply Operation +4.5 to +18 Volts
- MPU Compatible
- Typical Resolution — 8 Bits
- Typical Conversion Cycle as Fast as 300 μs
- Ratio Metric Conversion Minimizes Error



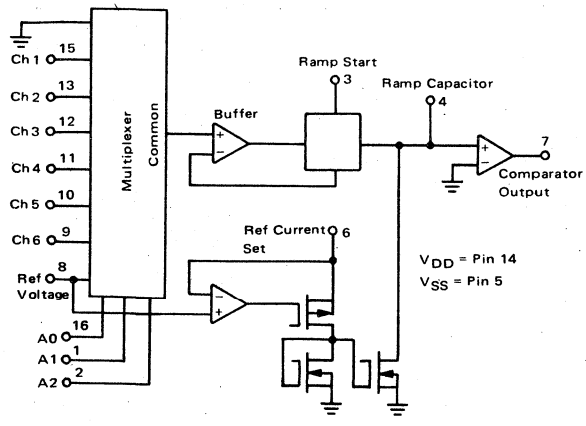
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

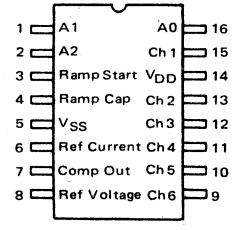
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



PIN ASSIGNMENT



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	T_{low}		25°C			T_{high}		Unit
		Vdc	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage—Comparator "0" Level	V_{OL}	5.0	–	0.05	–	0.01	0.05	–	0.05	Vdc
V_{in} @ Pin 4 = 0 V		10	–	0.05	–	0.01	0.05	–	0.05	
		15	–	0.05	–	0.01	0.05	–	0.05	
V_{in} @ Pin 4 = 1.0 V "1" Level	V_{OH}	5.0	4.95	–	4.95	4.99	–	4.95	–	Vdc
(R_L = 10 k, MC14447 only)		10	9.95	–	9.95	9.99	–	9.95	–	
		15	14.95	–	14.95	14.99	–	14.95	–	
Input Voltage-Address, Ramp Start "0 Level"	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current—Comparator	I_{OH}									mAdc
V_{in} @ Pin 4 = 1.0 V (MC14447 only)										
(V_{OH} = 2.5 Vdc)		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
V_{in} @ Pin 4 = 0 V	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current—Address, Ramp Start	I_{in}	15	–	±0.3	–	–	±0.3	–	±1.0	μAdc
Input Current—Analog Inputs	I_{in}	15	–	–	–	±0.1	±10	–	–	nAdc
Input Capacitance—Address, Ramp Start V_{in} = 0 V	C_{in}	15	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5	–	–	–	0.8	–	–	–	mAdc
		10	–	–	–	1.5	–	–	–	
		15	–	–	–	1.7	–	–	–	
Crosstalk Between Any Two Input Channels	V_{Cr}	–	–	–	–	0	4.0	–	–	mVdc
Reference Current Range	I_R	–	–	–	10	–	50	–	–	μAdc
Common Mode Input Voltage	V_{CM}	5	–	–	0	–	2.5	–	–	Vdx
		10	–	–	0	–	7.0	–	–	
		15	–	–	0	–	12	–	–	
Buffer Amplifier Output Offset	V_{BO}	5	–	–	–	0.285	–	–	–	Vdc
		10	–	–	–	0.400	–	–	–	
		15	–	–	–	0.420	–	–	–	
Comparator Threshold	V_{TC}	5	–	–	–	0.195	V_{BO}	–	–	Vdc
		10	–	–	–	0.275	V_{BO}	–	–	
		15	–	–	–	0.290	V_{BO}	–	–	
Reference Voltage Range	V_R	5	–	–	2.0	–	2.5	–	–	Vdc
		10	–	–	2.0	–	7	–	–	
		15	–	–	2.0	–	12	–	–	
Conversion Linearity V_{in} = V_{DD} – 3 V for C > 100 pF	L_C	–	–	–	–	0.15	0.3	–	–	% Full Scale

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Sumbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time—Comparator (MC14447 only)	t_{TLH}	5.0	–	120	240	ns
		10	–	75	150	
		15	–	65	130	
Output Fall Time—Comparator	t_{THL}	5.0	–	250	500	ns
		10	–	350	700	
		15	–	650	1300	
Propagation Delay Time—Comparator MC14443 (R_L = 10 k to V_{DD})	t_{PLH}	5.0	–	550	1100	ns
		10	–	500	1000	
		15	–	550	1100	
	t_{PHL}	5.0	–	350	700	ns
		10	–	300	600	
		15	–	300	600	
MC14447	t_{PLH}	5.0	–	600	1200	ns
		10	–	475	950	
		15	–	500	1000	
	t_{PHL}	5.0	–	450	980	ns
		10	–	540	1080	
		15	–	750	1500	
Multiplexer Propagation Delay	t_M	5.0	–	180	360	ns
		10	–	125	250	
		15	–	110	220	
Ramp Start Delay Time	t_{TS}	5.0	–	40	80	ns
		10	–	25	50	
		15	–	20	40	
Acquisition Time* C = 1000 pF R = 100 kΩ	t_A	5.0	–	30	60	μs
		10	–	15	30	
		15	–	14	28	

* Acquisition Time includes multiplexer propagation delay, ramp start propagation delay and the time required to charge ramp capacitor to the selected input voltage.

DEVICE OPERATION

ADDRESS INPUTS SELECT (A0, A1, A2, Pins 1, 2, 16) The input voltage source to be presented to the measurement system according to the Truth Table shown in Figure 3.

RAMP START (Ramp Start, Pin 3) When the Ramp Start is low, the ramp capacitor is charged to a voltage associated with the selected input channel. When the Ramp Start is brought high,the connection to the input channel is broken and the capacitor begins to ramp toward V_{SS}.

RAMP CAPACITOR (Ramp Cap, Pin 4) The ramp capacitor is used to generate a time period when discharged from a selected voltage via a precise reference current.

NEGATIVE POWER SUPPLY (V_{SS}, Pin 5) This pin is system ground.

REFERENCE CURRENT (Ref Current, Pin 6) To discharge the ramp capacitor, the reference current is fixed via a resistor (R_{Ref}) to a positive supply from pin 6. Typical current is equal to $(V_{DD} - V_{Ref})/R_{Ref}$.

COMPARATOR OUTPUT (Comp Out, Pin 7) This output is low when the capacitor has reached the discharged voltage and is high otherwise.

REFERENCE VOLTAGE (Ref Voltage, Pin 8) This voltage can be set to a voltage between V_{SS} + 2 V and V_{DD} – 2 V. This is the known voltage to which the unknown is compared.

INPUT CHANNELS (Pins 9, 10, 11, 12, 13, 15) Input channels 1 through 6 are used to monitor up to six separate unknown voltages. Selection is via the address inputs.

POSITIVE POWER SUPPLY (V_{DD}, Pin 14) This pin is the package positive power supply pin.

FIGURE 1 – VOLTAGE TO PULSE WIDTH CONVERSION

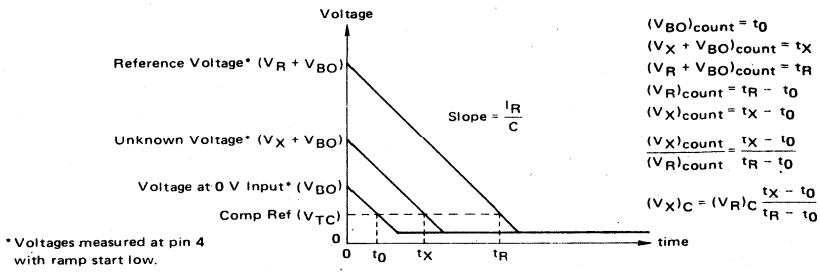
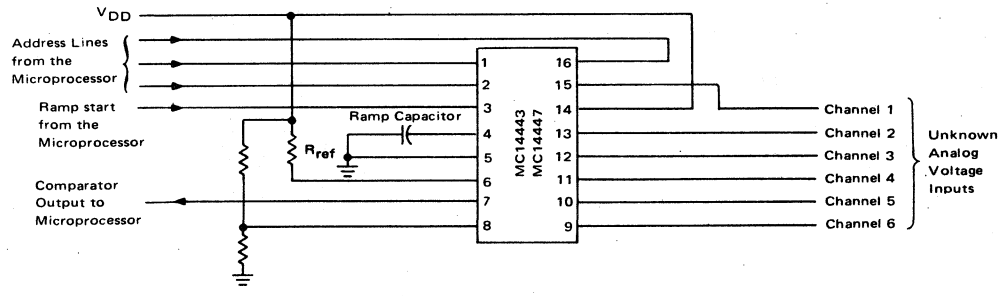


FIGURE 2 – TRUTH TABLE

A2	A1	A0	Input Selected	
0	0	0	V_{SS}	Channel 0 (ground)
0	0	1	Ch1	Channel 1
0	1	0	Ch2	Channel 2
0	1	1	Ch3	Channel 3
1	0	0	Ch4	Channel 4
1	0	1	Ch5	Channel 5
1	1	0	Ch6	Channel 6
1	1	1	V_{Ref}	Channel 7 (External Reference)

FIGURE 3 – TYPICAL APPLICATIONS CIRCUIT



CONVERSION SEQUENCE

Step No.	A2	A1	A3	Ramp Start	Comment
1.	1	1	1	0	Channel 7 Selected (Reference Voltage)
2.	1	1	1	1	Record time until Pin 7 goes low
3.	0	0	0	0	Channel 0 Selected (Ground)
4.	0	0	0	1	Record time until Pin 7 goes low
5.	0	0	1	0	Channel 1 Selected
6.	0	0	1	1	Record time until Pin 7 goes low
Calculate $t_{Ch7} - t_{Ch0} = t_{Ch7}'$ Step 2–Step 4					
Calculate $t_{Ch1} - t_{Ch0} = t_{Ch1}'$ Step 6–Step 4					
Calculate $V_{unknown} = V_{Ch7}(t_{Ch1}'/t_{Ch7}')$					
7.	0			0	Channel 2 Selected
8.	0			1	Record time until Pin 7 goes low
Calculate $t_{Ch2} - t_{Ch0} = t_{Ch2}'$					
Calculate $V_{unknown} = V_{Ch7}(t_{Ch2}'/t_{Ch7}')$					
etc.					

MOTOROLA

MC14450

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

OSCILLATOR/2^{16} DIVIDER/BUFFER

OSCILLATOR/2^{16} DIVIDER/BUFFER
with Integrated Feedback Capacitor

The MC14450 consists of an oscillator, 16-stage divider, and two buffers in a single monolithic structure. This circuit employs complementary MOS devices for low-voltage operation and extremely low power dissipation. It finds primary use in crystal controlled timing circuitry, and is particularly suited for wristwatch and low-voltage clock operation.

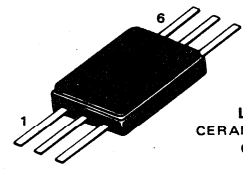
The oscillator section has an output capacitor integrated on the chip. The addition of a crystal, an input capacitor, and a feedback resistor is all that is necessary to complete the oscillator circuit.

The divider section consists of a 16-stage binary divider. Two outputs are provided, 180 degrees out of phase. The outputs of the last six stages of the divider are used to gate the output pulses, providing narrow output pulse widths. Both outputs are buffered to provide fast rise and fall times, and to maximize energy transfer to the load for the pulse duration.

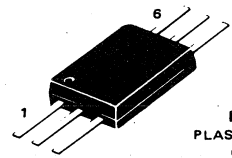
The MC14450 utilizes a 1.58 volt silver oxide battery, and provides peak output pulse voltages of more than 1.20 volts with a 5.2 kilohm load.

This device provides a divide-by-65,536 function and can be operated at frequencies to 1.0 MHz. When operated at 32.768 kHz, it provides 0.5 Hz, 1.563% duty cycle alternating output pulses.

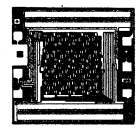
- Extremely Low Operating Current Consumption: 4.0 μA Typical
- Typical Power Supply = 1.58 V
- Inverting Amplifier with Integrated Feedback Capacitor
- Gated and Buffered Outputs
- Diode Protection on Input
- High Output Drive at Low Voltage



L SUFFIX
CERAMIC PACKAGE
CASE 688

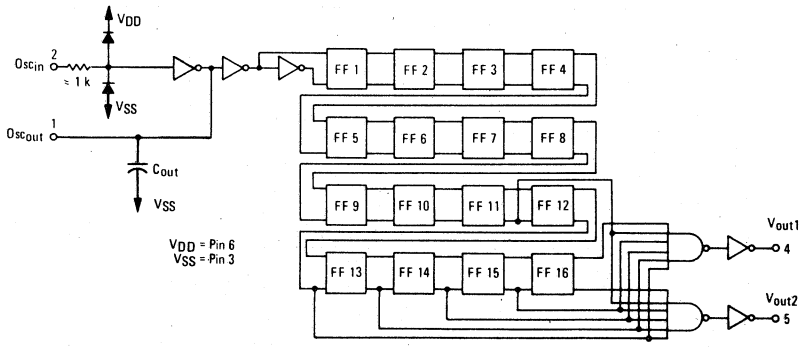


P SUFFIX
PLASTIC PACKAGE
CASE 704



MCC PREFIX
CHIP

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 3.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+3.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	0 to +50	°C
Storage Temperature Range	T_{stg}	-30 to +85	°C

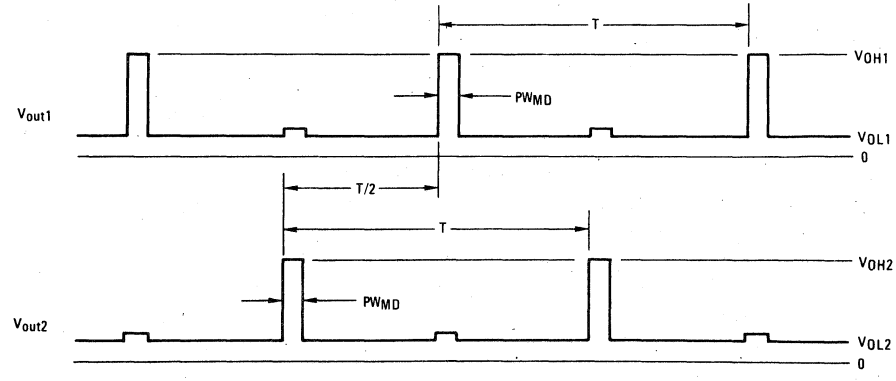
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (V_{DD} = 1.58 Vdc, V_{SS} = 0, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Operating Range	V_{DD}	1.3	1.5	3.0	Vdc
Output Voltage (No Load)	V_{OH}	1.4	1.5	–	Vdc
	V_{OL}	–	0.0	0.1	Vdc
Output Drive Current					
(V_{OH} = 1.3 Vdc)	I_{OH}	700	–	–	μAdc
(V_{OL} = 0.2 Vdc)	I_{OL}	1000	–	–	μAdc
Input Current	I_{in}	–	0.00001	–	μAdc
Quiescent Device Current	I_Q	–	–	1.0	μAdc
Dynamic Device Current	I_{DD}				μAdc
(f = 32.768 kHz, No Output Load) Square Wave, Pin 2		–	2.6	7.0	
MTQ32A Crystal		–	4.0	–	
Minimum Voltage Required for Oscillator Start	V_{DDS}	–	1.4	1.5	Vdc
Feedback Oscillator Capacitance	C_{out}	–	20	–	pF

FIGURE 1 – OUTPUT WAVEFORMS



PW_{MD}, MOTOR DRIVE PULSE WIDTH = 0.01563 T

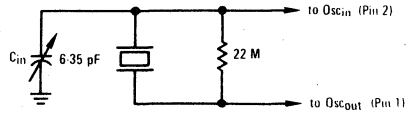
OUTPUT PERIOD, $T = \frac{65536}{\text{INPUT FREQUENCY}}$

$V_{on1} = V_{OH1} = V_{OL2}$

$V_{on2} = V_{OH2} = V_{OL1}$

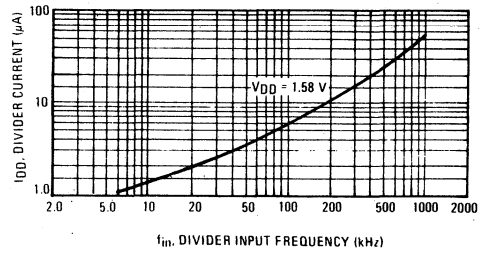
Note: Refer to Figure 4 for connection diagram.

FIGURE 2 – TYPICAL 32-kHz OSCILLATOR CIRCUIT



MOTOROLA MTQ32A CRYSTAL
$f_{A(C_L)}$ = 32.768 kHz
R_S = 30 kΩ
C_0 = 1.9 pF Typical
C_1 = 0.0056 pF Typical

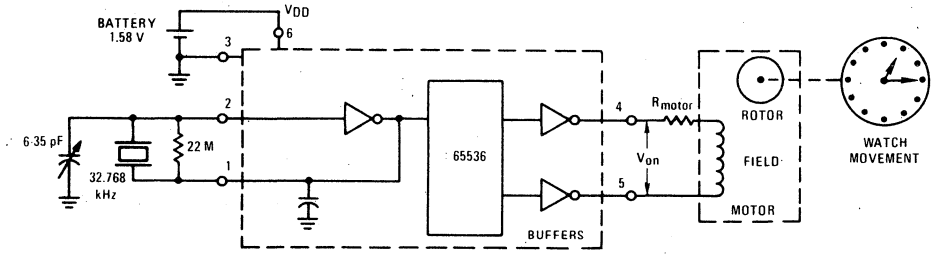
FIGURE 3 – TYPICAL CURRENT DRAIN versus FREQUENCY (No Output Load)



APPLICATIONS INFORMATION

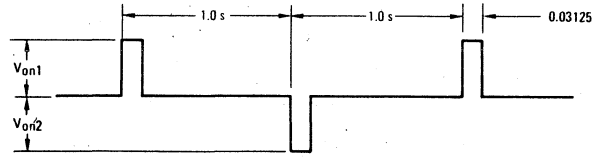
Figure 4 illustrates a typical wristwatch system. The MC14450 drives a rotary motor which rotates 180° with each input pulse.

FIGURE 4 – TYPICAL WRISTWATCH SYSTEM



V_{on} = Voltage at pin 4 minus voltage at pin 5.
R_{motor} = 5.2 kΩ minimum

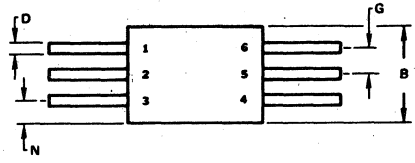
OUTPUT WAVEFORM ACROSS MOTOR



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

PACKAGE DIMENSIONS

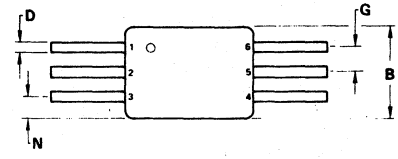
CASE 688-05



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	7.11	0.235	0.280
B	4.32	5.72	0.170	0.225
C	1.17	1.91	0.046	0.075
D	0.25	0.51	0.010	0.020
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.13	0.89	0.005	0.035
K	1.90	3.05	0.075	0.120
N	0.89	1.52	0.035	0.060

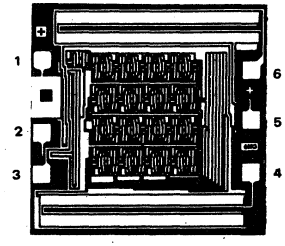
NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.13 mm (0.005) RADIUS TO DIM "A" & "B" AT MAXIMUM MATERIAL CONDITION.

CASE 704-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.69	6.35	0.224	0.250
B	4.06	5.08	0.160	0.200
C	1.17	1.90	0.046	0.075
D	0.38	0.51	0.015	0.020
F	0.20	0.30	0.008	0.012
G	1.22	1.32	0.048	0.052
H	0.13	0.89	0.005	0.035
K	2.34	2.84	0.092	0.112
N	0.89	1.14	0.035	0.045

MCC14450 BONDING PADS



Chip geometry subject to change without notice as modifications are made.

Due to die cleavage angles, the actual size of the chip could be up to 7.0 mils (0.17 mm) larger than indicated in both dimensions.

Die Size: 64 x 68 mils

MOTOROLA

MC14451

OSCILLATOR/2^{11} to 2^{19} DIVIDER/BUFFERED DUTY CYCLE CONTROL

The MC14451 consists of three sections: an oscillator, an 18-stage divider, and a buffered flip-flop for pulse width control and current sink drive. These circuits employ metal-gate complementary MOS devices for low-voltage operation and extremely low power dissipation.

A wide variety of output pulse widths and frequencies can be obtained using the pulse-width-control flip-flop. The number of combinations can be further increased by the variety of crystal frequencies or R-C networks used with the oscillator section.

The buffered output of the duty-cycle-control flip-flop consists of an N-channel MOSFET for maximum current sinking capability and a P-channel active pullup device. Outputs from the 18-stage divider section provide a negative logic binary count.

Applications of the MC14451 include power-off timers, low-power-consumption timers especially suited for battery applications, elapsed timers, wall clocks, auto-timers for feeding systems, fuse timers, incubator timers, weather measurement equipment, and many other battery or low-power applications.

- On-Chip Duty Cycle Control
- Buffered Duty Cycle Control Output
- On-Chip Oscillator
- Low Power Consumption — 20 μW typical @ 1.5 Vdc and f = 262 kHz
- Operating Supply Voltage Range = 1.3 to 3.0 Vdc
- Diode Protection on Inputs

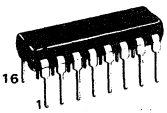
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

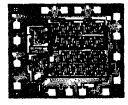
OSCILLATOR/2^{11} to 2^{19} DIVIDER/ BUFFERED DUTY CYCLE CONTROL



L SUFFIX
CERAMIC PACKAGE
CASE 620

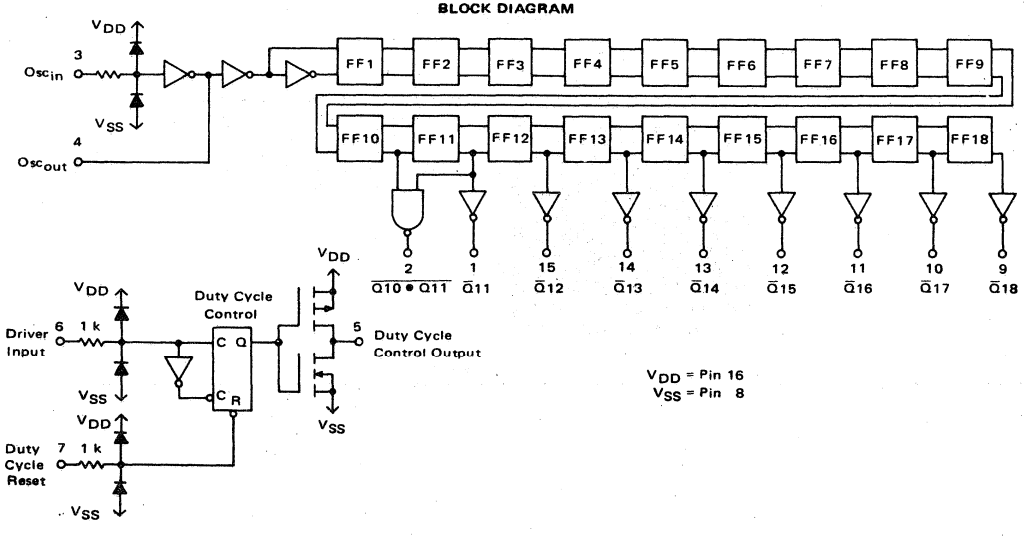


P SUFFIX
PLASTIC PACKAGE
CASE 648



MCC PREFIX
CHIP

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{DD}	+3.0 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	−10 to +60	°C
Storage Temperature Range	T_{stg}	−30 to +85	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (V_{DD} = 1.58 Vdc, V_{SS} = 0, T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Power Supply Operating Range		V_{DD}	1.3	1.5	3.0	Vdc
Output Voltage		V_{OH}	1.38	1.5	–	Vdc
		V_{OL}	–	0.0	0.2	Vdc
Output Drive Current		I_{OH}				μAdc
(V_{OH} = 1.3 Vdc)	Divider Outputs		-8.0	-25	–	
	Duty Cycle Control Output		-8.0	-25	–	
(V_{OL} = 0.2 Vdc)	Divider Outputs	I_{OL}	15	50	–	μAdc
	Duty Cycle Control Output		400	1200	–	
Input Current		I_{in}	–	0.00001	–	μAdc
Quiescent Device Current		I_Q	–	1.0	15	μAdc
Dynamic Device Current (f = 262.144 kHz, no output load)		I_{DD}	–	20	200	μAdc
Minimum Voltage Required for Oscillator Start		V_{DDS}	–	1.2	1.5	Vdc

TYPICAL OSCILLATOR CIRCUITS

FIGURE 1 – 262-kHz CIRCUIT

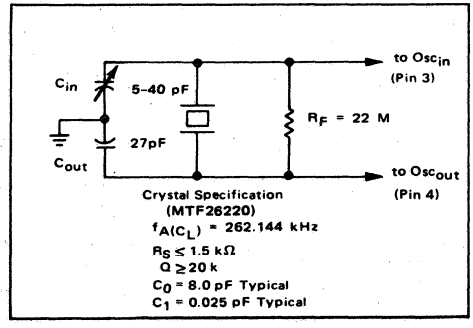


FIGURE 2 – 32.768 kHz CIRCUIT

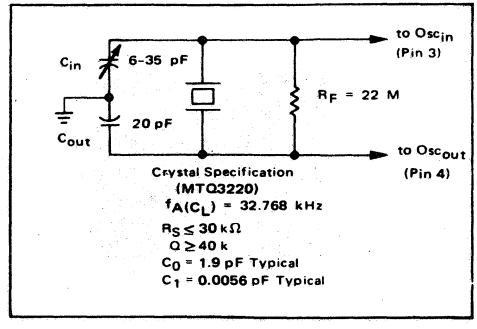
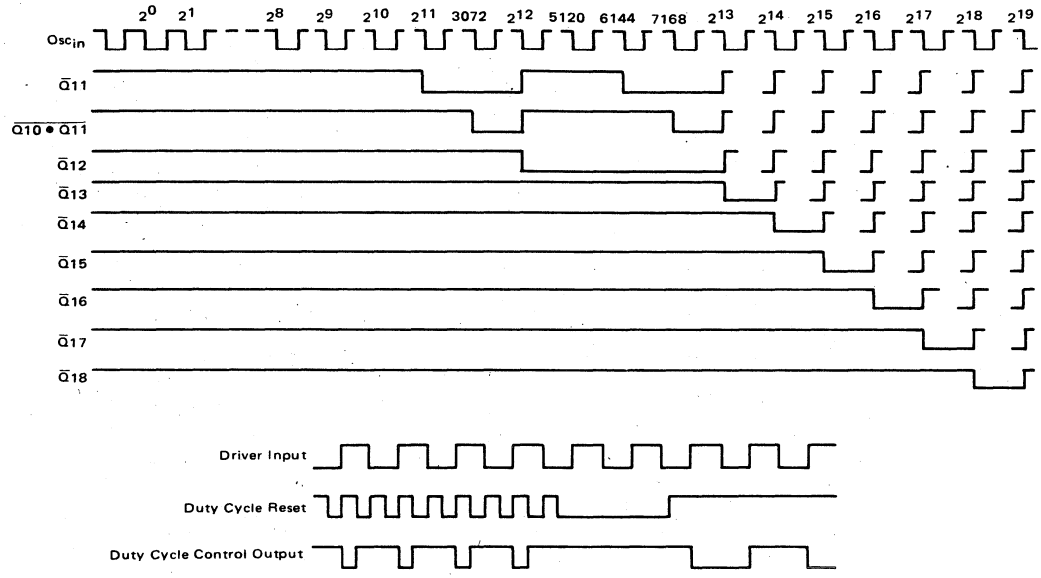
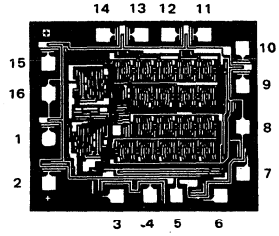


FIGURE 3 – TIMING DIAGRAM



MCC14451 BONDING PADS



Die Size: 67 x 69 mils

Chip geometry subject to change without notice as modifications are made.

Due to die cleavage angles, the actual size of the chip could be up to 7.0 mils (0.17 mm) larger than indicated in both dimensions.

FIGURE 4 – FUNCTIONAL MATRIX

Crystal Frequency = 262.144 kHz

Pin 6 (Driver Input) Connected To:	Characteristic	Pin 7 (Duty Cycle Reset) Connected To:								
		Pin 1 $\bar{Q}11$	Pin 2 $\overline{Q10 \bullet Q11}$	Pin 15 $\bar{Q}12$	Pin 14 $\bar{Q}13$	Pin 13 $\bar{Q}14$	Pin 12 $\bar{Q}15$	Pin 11 $\bar{Q}16$	Pin 10 $\bar{Q}17$	Pin 9 $\bar{Q}18$
Pin 9 $\bar{Q}18$	Pulse Width	3.9 ms	5.85 ms	7.8 ms	15.62 ms	31.25 ms	62.5 ms	125 ms	250 ms	500 ms
	f_{out}	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz
Pin 10 $\bar{Q}17$	Pulse Width	3.9 ms	5.85 ms	7.8 ms	15.62 ms	31.25 ms	62.5 ms	125 ms	250 ms	
	f_{out}	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz	
Pin 11 $\bar{Q}16$	Pulse Width	3.9 ms	5.85 ms	7.8 ms	15.62 ms	31.25 ms	62.5 ms	125 ms		
	f_{out}	4 Hz	4 Hz	4 Hz	4 Hz	4 Hz	4 Hz	4 Hz		
Pin 12 $\bar{Q}15$	Pulse Width	3.9 ms	5.85 ms	7.8 ms	15.62 ms	31.25 ms	62.5 ms			
	f_{out}	8 Hz	8 Hz	8 Hz	8 Hz	8 Hz	8 Hz			
Pin 13 $\bar{Q}14$	Pulse Width	3.9 ms	5.85 ms	7.8 ms	15.62 ms	31.25 ms				
	f_{out}	16 Hz	16 Hz	16 Hz	16 Hz	16 Hz				
Pin 14 $\bar{Q}13$	Pulse Width	3.9 ms	5.85 ms	7.8 ms	15.62 ms					
	f_{out}	32 Hz	32 Hz	32 Hz	32 Hz					
Pin 15 $\bar{Q}12$	Pulse Width	3.9 ms	5.85 ms	7.8 ms						
	f_{out}	64 Hz	64 Hz	64 Hz						
Pin 1 $\bar{Q}11$	Pulse Width	3.9 ms								
	f_{out}	128 Hz								

Crystal Frequency = 32.768 kHz

Pin 6 (Driver Input) Connected To:	Characteristic	Pin 7 (Duty Cycle Reset) Connected To:								
		Pin 1 $\bar{Q}11$	Pin 2 $\overline{Q10 \bullet Q11}$	Pin 15 $\bar{Q}12$	Pin 14 $\bar{Q}13$	Pin 13 $\bar{Q}14$	Pin 12 $\bar{Q}15$	Pin 11 $\bar{Q}16$	Pin 10 $\bar{Q}17$	Pin 9 $\bar{Q}18$
Pin 9 $\bar{Q}18$	Pulse Width	31.3 ms	46.8 ms	62.5 ms	125 ms	250 ms	500 ms	1000 ms	2000 ms	4000 ms
	f_{out}	0.125 Hz	0.125 Hz	0.125 Hz	0.125 Hz	0.125 Hz	0.125 Hz	0.125 Hz	0.125 Hz	0.125 Hz
Pin 10 $\bar{Q}17$	Pulse Width	31.3 ms	46.8 ms	62.5 ms	125 ms	250 ms	500 ms	1000 ms	2000 ms	
	f_{out}	0.25 Hz	0.25 Hz	0.25 Hz	0.25 Hz	0.25 Hz	0.25 Hz	0.25 Hz	0.25 Hz	
Pin 11 $\bar{Q}16$	Pulse Width	31.3 ms	46.8 ms	62.5 ms	125 ms	250 ms	500 ms	1000 ms		
	f_{out}	0.5 Hz	0.5 Hz	0.5 Hz	0.5 Hz	0.5 Hz	0.5 Hz	0.5 Hz		
Pin 12 $\bar{Q}15$	Pulse Width	31.3 ms	46.8 ms	62.5 ms	125 ms	250 ms	500 ms			
	f_{out}	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz			
Pin 13 $\bar{Q}14$	Pulse Width	31.3 ms	46.8 ms	62.5 ms	125 ms	250 ms				
	f_{out}	2 Hz	2 Hz	2 Hz	2 Hz	2 Hz				
Pin 14 $\bar{Q}13$	Pulse Width	31.3 ms	46.8 ms	62.5 ms	125 ms					
	f_{out}	4 Hz	4 Hz	4 Hz	4 Hz					
Pin 15 $\bar{Q}12$	Pulse Width	31.3 ms	46.8 ms	62.5 ms						
	f_{out}	8 Hz	8 Hz	8 Hz						
Pin 1 $\bar{Q}11$	Pulse Width	31.3 ns								
	f_{out}	16 Hz								

MOTOROLA

MC14457
MC14458

CMOS MSI/LSI

(LOW-POWER COMPLEMENTARY MOS)

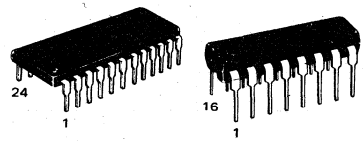
TRANSMITTER
RECEIVER

MC14457 TRANSMITTER
MC14458 RECEIVER

The MC14457 and MC14458 are a transmitter and receiver pair of integrated circuits constructed in CMOS monolithic technology. These units are designed for ultrasonic or infrared remote control of TV receivers, converters, communication receivers, and games. Channel selection up to 16 channels can be done single entry; or, up to 256 channels can be done double entry.

FEATURES:

- Low External Component Count
- High Noise Immunity
- Error Free Operation
- One Analog Output From Receiver
- On-Signal Provision
- Low Power



Receiver
P SUFFIX
PLASTIC PACKAGE
CASE 709

Transmitter
P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

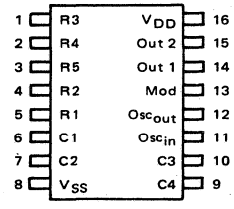
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

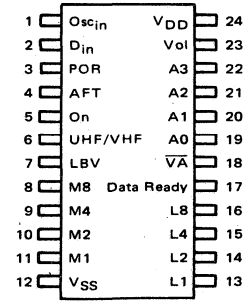
Rating		Symbol	Value	Unit
DC Supply Voltage	MC14457 MC14458	V_{DD}	−0.5 to +12 −0.5 to +6.0	Vdc
Input Voltage, All Inputs		V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin		I	10	−mAdc
Operating Temperature Range		T_A	−40 to +85	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

PIN ASSIGNMENTS

MC14457
TRANSMITTER



MC14458
RECEIVER



TRANSMITTER MC14457

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
Input Voltage # "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
Output Drive Current – Pins 14, 15 (Out 1, 2)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-6.0	–	-5.0	-9.0	–	-3.5	–	
(V_{OH} = 9.5 Vdc)		10	-3.2	–	-2.6	-4.5	–	-1.8	–	
(V_{OL} = 2.5 Vdc) Sink	I_{OL}	5.0	6.0	–	5.0	9.0	–	3.5	–	mAdc
(V_{OL} = 0.5 Vdc)		10	3.2	–	2.6	4.5	–	1.8	–	
Output Drive Current – Pin 13 (Mod)	I_{OH}									mAdc
(V_{OH} = 4.6 Vdc) Source		5.0	-0.26	–	-0.22	-0.44	–	-0.18	–	
(V_{OH} = 9.5 Vdc)		10	-0.6	–	-0.55	-1.12	–	-0.45	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.26	–	0.22	0.44	–	0.18	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.6	–	0.55	1.12	–	0.45	–	
Input Current – Pull-ups	I_{in}	10	–	–	50	500	1000	–	–	μAdc
Input Current – Pin 11 (Osc_{in})	I_{in}	10	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current – Per Package	I_{DD}	5.0	–	50	–	0.008	50	–	375	μAdc
(Osc_{in} = Low)		10	–	100	–	0.016	100	–	750	
**Total Supply Current at an External Load Capacitance (C_L) of Figure 4. f = 500 kHz (with any Analog command)	I_T	5.0	–	–	–	5.0	–	–	–	μAdc
		10	–	–	–	10	–	–	–	

RECEIVER – MC14458

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0										
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}										
Input Voltage # "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.5	–	-0.5	-1.7	–	-0.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.45	–	0.4	0.78	–	0.34	–	mAdc
Input Current (Osc_{in}, D_{in})	I_{in}	5.0	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Current ($\overline{POR}$)	I_{in}	5.0	–	–	10	50	400	–	–	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	250	1000	–	–	μAdc
Data Input Hysteresis	V_{Hys}	5.0	–	–	–	0.25	–	–	–	μAdc
**Total Supply Current at an External Load Capacitance (C_L) of Figure 6 f = 500 kHz	I_T	5.0	–	–	–	400	–	–	–	μAdc

*T_{low} = -40°C
T_{high} = +85°C
**The formulas given are for the typical characteristics only at 25°C

#Noise immunity specified for worst-case input combination
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc

SWITCHING CHARACTERISTICS (MC14457 – Transmitter V_{DD} = 5 to 15 V, MC14458 – Receiver V_{DD} = 5 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Rise and Fall Time – Receiver C_L = 100 pF	^tTLH, ^tTHL	–	0.3	1.0	μs
Oscillator Start-Up Time – Transmitter	t_{on}	–	8.0	–	μs
Clock Pulse Frequency	PRF	–	500	600	kHz

MC14457 – Transmitter

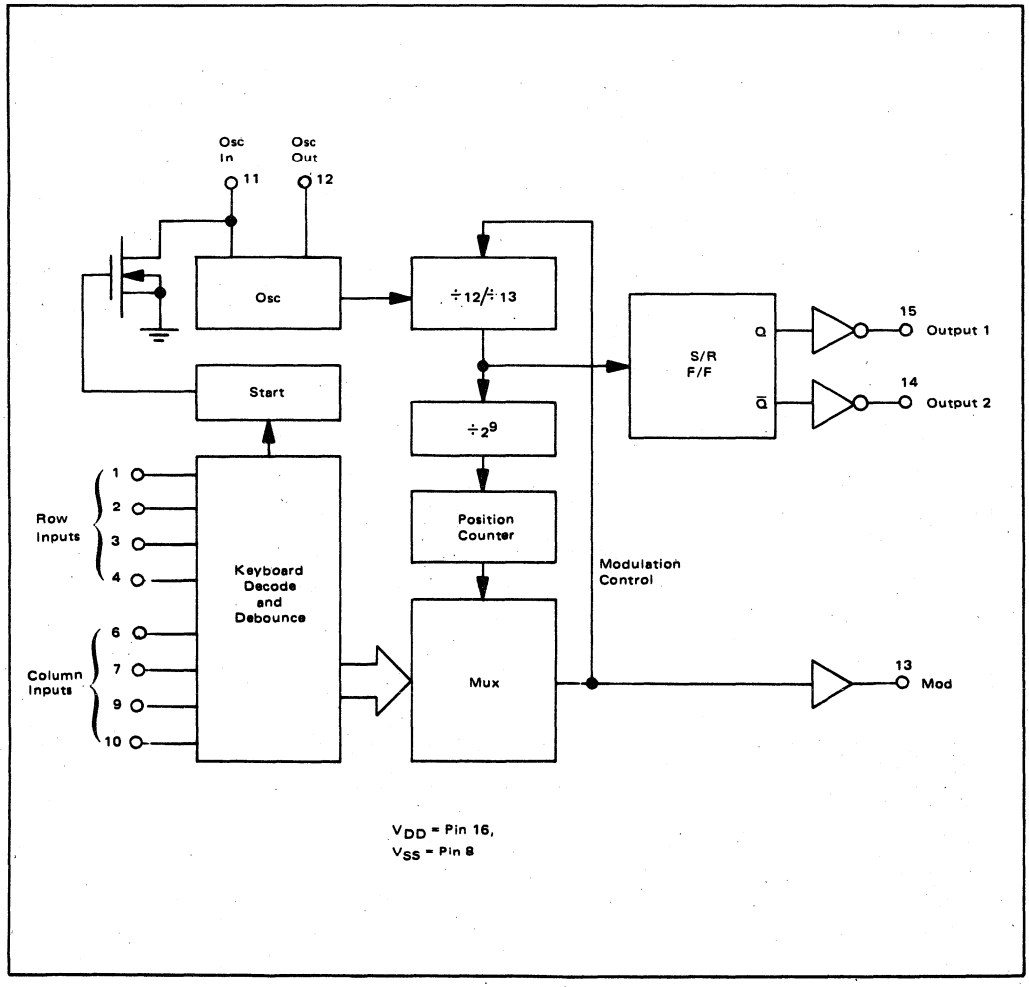


FIGURE 1 – Example of Transmitted Word

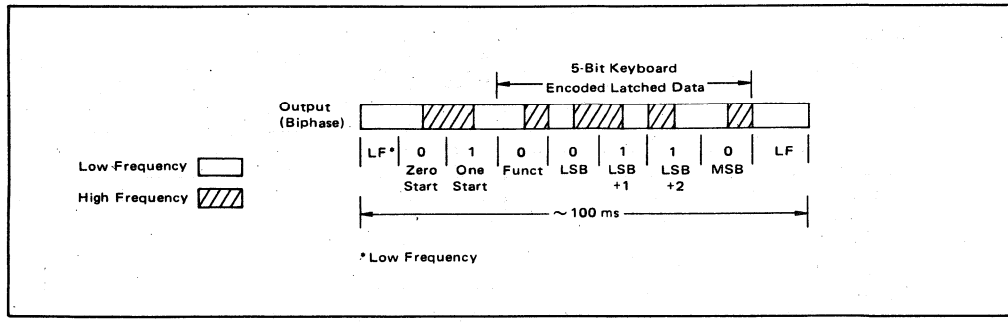
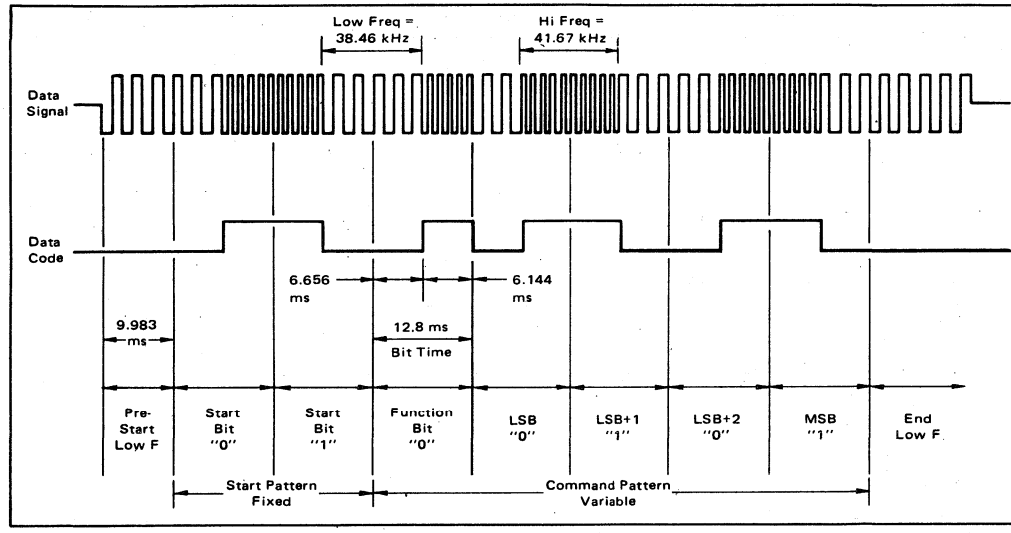


FIGURE 2 – Data Signal



INPUT/OUTPUT FUNCTIONS – MC14457; TRANSMITTER

Row Inputs (R1, R2, R3, R4, R5; Pins 1, 2, 3, 4, 5)

These pins are the row inputs and are active in the low state.

Column Inputs (C1, C2, C3, C4; Pins 6, 7, 9, 10)

These pins are the column inputs and are active in the low state.

Output (Out 1, Out 2; Pins 14, 15)

These pins provide push-pull output and can be used with ceramic transducers or LEDs. In the non-operating condition, both outputs are at ground potential.

Oscillator (Osc_{in}, Osc_{out}; Pins 11, 12)

These pins are the input/output terminals of the oscillator. It can be used with ceramic resonator or crystal. The oscillator is automatically turned off after the data is transmitted for low current quiescent operation.

Modulation (Mod; Pin 13)

This pin is a data code output.

TABLE 1 – Data Code

Key Number	Operation	Row (Active Low)	Column (Active Low)	Transmitter Data & Receiver Output Address					$\overline{VA}$ Pulse	Notes
				MSB/A3	LSB+2/A2	LSB+1/A1	LSB/A0	Function		
1	Digit 0	R1	C1	0	0	0	0	0	–	1
2	Digit 1	R1	C2	0	0	0	1	0	–	1
3	Digit 2	R2	C1	0	0	1	0	0	–	1
4	Digit 3	R2	C2	0	0	1	1	0	–	1
5	Digit 4	R3	C1	0	1	0	0	0	–	1
6	Digit 5	R3	C2	0	1	0	1	0	–	1
7	Digit 6	R4	C1	0	1	1	0	0	–	1
8	Digit 7	R4	C2	0	1	1	1	0	–	1
9	Digit 8	R5	C1	1	0	0	0	0	–	1
10	Digit 9	R5	C2	1	0	0	1	0	–	1
11	Spare	R1	C3	0	0	0	0	1	√	2
12	Spare	R1	C4	0	0	0	1	1	√	2
13	Fine Tuning	R2	C3	0	0	1	0	1	√	3
14	Fine Tuning	R2	C4	0	0	1	1	1	√	3
15	Spare	R3	C3	0	1	0	0	1	√	3
16	Spare	R3	C4	0	1	0	1	1	√	3
17	Vol ↓	R4	C3	0	1	1	0	1	√	3
18	Vol ↑	R4	C4	0	1	1	1	1	√	3
19	Mute	R5	C3	1	0	0	0	1	√	2
20	Off	R5	C4	1	0	0	1	1	√	2
21	Digit 10	R2 + R5	C1	1	0	1	0	0	–	1
22	Digit 11	R2 + R5	C2	1	0	1	1	0	–	1
23	Digit 12	R3 + R5	C1	1	1	0	0	0	–	1
24	Digit 13	R3 + R5	C2	1	1	0	1	0	–	1
25	Digit 14	R2+R3+R5	C1	1	1	1	0	0	–	1
26	Digit 15	R2+R3+R5	C2	1	1	1	1	0	–	1
27	Spare	R2 + R5	C3	1	0	1	0	1	–	3
28	Spare	R2 + R5	C4	1	0	1	1	1	–	3
29	Spare	R3 + R5	C3	1	1	0	0	1	–	3
30	Spare	R3 + R5	C4	1	1	0	1	1	–	3
31	Spare	R2+R3+R5	C3	1	1	1	0	1	–	3
32	Spare	R2+R3+R5	C4	1	1	1	1	1	–	3

Notes

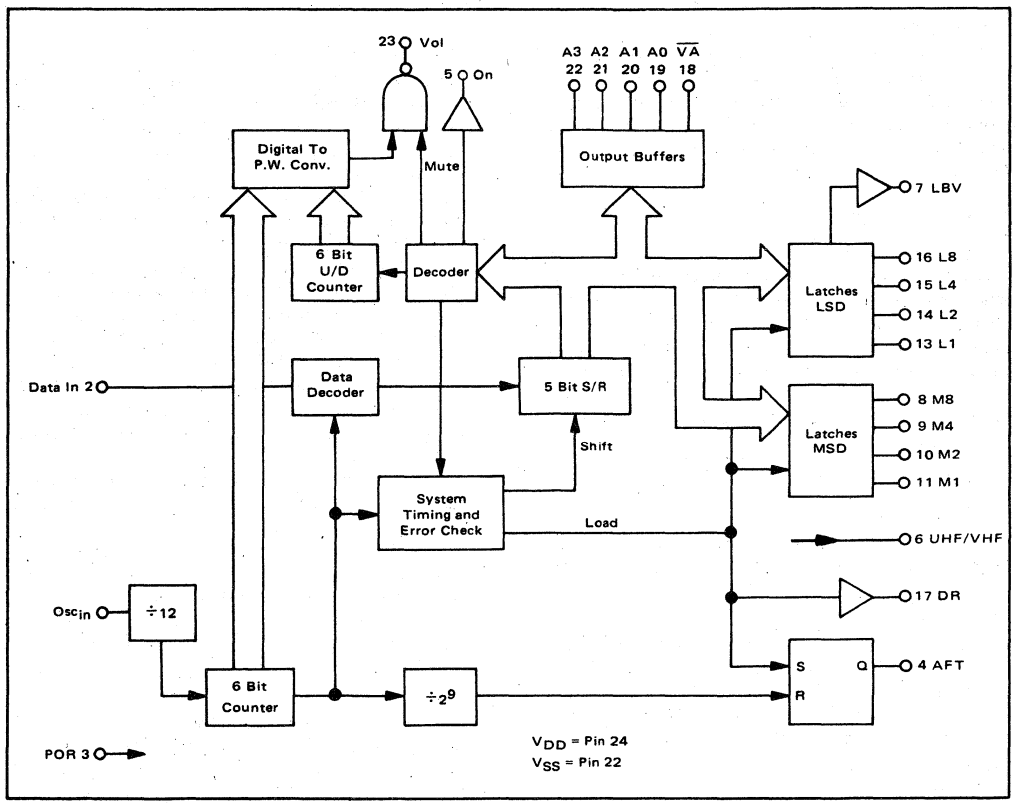
1. Channel Select Keys (Function Bit = 0). Data is transmitted once each time a key is activated.
2. Toggling type On/Off or counter advance type keys. Data is transmitted once each time a key is activated.
3. Analog Up/Down or On/Off keys, i.e., one key for Down or Off and another key for Up or On. Data transmission is repeated as long as the key is operated.

In Table 1 all channel select data is noted by the function bit equal to zero. For functions other than channel, the function bit equals one.

The four toggling or counter advance type keys that transmit data once each time a key is activated are Mute, Off, Channel Search Up, and Channel Search Down.

The twelve remaining analog keys (Vol, Tint, Color, etc.) transmit data as long as the key is activated. The keys' functions are arranged to provide the most typical application without grounding of multiple row or columns required.

MC14458 – Receiver



General Description

This transmitter integrated circuit is used for encoding keyboard position into frequency-modulated biphase data. This integrated circuit can function with a keyboard from 20 to 32 keys and provide either channel select/toggle information (single-word transmission) or analog information (continuous transmission of the data word for duration of key press).

When used in conjunction with the receiver, selection capability is: any single or two-digit channel select up to 256 channels with appropriate keyboard; a maximum of 12 analog control functions; 4 toggle type commands. At an operating voltage of 9.0 volts, the high output drivers provide 4 V_{PP} into a 1 kΩ load via an output bridge configuration. The chip features low standby power as all portions are shut off after data transmission, with the counter-chain held in the reset position.

Operation

As one example of operation, a free-running ceramic resonator oscillator (at 500 kHz), triggered by the depression of any key, is divided by 12 or 13 to provide frequencies of 41.67 kHz or 38.46 kHz. The transmitted data 'zero' consists of 256 periods of the lower frequency followed by an equal number of the higher frequency. Mark to space ratio is kept at 1:1 in each case. Data 'one' reverses the order of the two frequencies.

Row and column information from the keyboard is encoded into a 5-bit word and loaded onto data latches on the edge of transmit enable. This data, preceded by two bits, 0 and 1, is used in sequence to provide biphase control of the divider and, consequently, the bit pattern transmitted from the unit. Each 7-bit word begins and ends with a low frequency burst. Operation of a channel select key produces an output data stream for a duration of approximately 100 ms.

INPUT/OUTPUT FUNCTIONS — MC14458; RECEIVER

Data (D_{in}; Pin 2)

The amplified ultrasonic data signal—after amplification and limiting forms a square wave with a peak-to-peak value of V_{DD}—is applied to this input terminal. The input terminal is supplied with amplified and square-wave limited signal. A peak-to-peak value of V_{DD} should be furnished.

Oscillator (Osc_{in}; Pin 1)

The oscillator input pin of the receiver pin is connected to an oscillator providing, for example, a 500 kHz square-wave signal. A typical oscillator circuit is shown in Figure 5. Accuracy of 1% relative to the oscillator frequency in the transmitter is recommended for satisfactory performance in very high echo-producting environments.

Channel Outputs (L1, 2, 4, 8, M1, 2, 4, 8; Pins 13, 14, 15, 16, 11, 10, 9, 8)

The eight data output pins provide latched data corresponding to the channel selected on the transmitter keyboard. L1 through L8 are the least significant bits; M1 through M8 are the most significant bits. The data on these pins is accompanied by a Data Ready signal.

Data Ready (Pin 17)

A positive pulse with a duration of 768 μs appears at pin 17 of the transmitter approximately 0.1 second after a complete command is entered on the remote control transmitter keyboard. The negative going edge of this pulse may be used for triggering purposes.

NOTE: A complete command is one digit in the single entry mode or two digits in the double entry mode.

AFT Enable (AFT; Pin 4)

The voltage level at this pin is low for a time duration of 0.393 second following a change in selected channel to allow disabling the tuner AFT circuit. Also, miscellaneous commands 0000, 0001, 0010, and 0011 (Channel Search Up/Down, Fine Tuning Up/Down) will cause this disable feature.

Power-On Reset (POR; Pin 3)

This pin is low for power-on reset of the analog output to 0 pulse width and off/on output to 0. An internal pull-up device of 10 to 400 μA will charge an external capacitor. Reset occurs until the input voltage reaches 70% V_{DD}. All internal registers will also be reset.

Address (A0, 1, 2, 3; Pins 19, 20, 21, 22)

The Address outputs of the receiver identify selected analog and on/off commands for use in system expansion. The data on these lines is valid when accompanied by a Valid Address pulse.

Valid Address ($\overline{VA}$; Pin 18)

A negative going pulse with a duration of 768 μs appears at pin 18 approximately 0.1 second after an analog on/off key on the remote control transmitter keyboard is operated. Either edge of this pulse may be used for control of add-on circuits.

The Valid Address pulse is repeated every 102.4 ms for as long as a key is operated which provides repeated transmission of data when held down.

The Valid Address signal may be used in conjunction with the Address Outputs to drive memories to provide additional control functions such as color, tint, etc.

The Valid Address pulse may be used to provide a stepping clock for up/down counters in a memory. The least significant address line (A0) is used to identify the up or down mode and the remaining address lines (A1, A2, A3) are decoded to enable each individual control circuit.

By adding up/down counters to the Data Outputs, it is possible to use the Valid Address pulse and a decoded address for implementing a channel up/down stepping function from the remote control. Additional On/Off functions may be obtained by using the Valid Address pulse in combination with a decoded address for setting and resetting of latches. The Valid Address signal is disabled in the standby mode (On output at logical 0).

UHF/VHF (Pin 6)

This pin of the receiver provides a low level when the selected channel is a VHF channel (00 to 13, or 84 to 99).

A high level on pin 6 identifies selection of a UHF channel (14 to 83). This signal is provided to permit switching of VHF and UHF tuners.

On (Pin 5)

This pin of the receiver provides a low level following operation of the Off command (1001) on the remote-control transmitter. The signal on this pin changes to a high level when a channel is selected.

Analog Out (Vol; Pin 23)

An analog voltage in the range between 0 V and V_{DD} is obtained by integrating the signal at the Analog Out pin through a low pass filter. The analog voltage resolution has been chosen to be 64 steps. Its value can be incremented or decremented in steps of one by keys providing commands 0111 and 0110, respectively. (See Table 1.)

The analog voltage can be varied up or down at a speed of approximately 10 steps per second. The D/A conversion is performed with an underflow and an overflow limiting circuit. The Analog Out pin is normally used

for the control of volume. The first time power is applied to the remote-control receiver, the volume output is 0 volts.

The Analog Out signal may be increased after a channel has been selected by operating the key providing a command 0111. (Volume Up)

The Analog Out signal may be muted by operating a key on the transmitter providing command 1000. Return to the original output prior to muting may be achieved by operating the mute key a second time or by operating the volume-up key.

In the standby mode the analog level is memorized and cannot be varied by the up/down controls on the transmitter.

Low Band (LBV; Pin 7)

This pin will go HIGH whenever channels 02, 03, 04, 05, or 06 are selected. The output is LOW for channels 00, 01, and 07 through 99.

Single Digit Operation

The receiver can be placed in a single-digit mode of operation by connecting the M4 data output (pin 9) to V_{DD} and the UHF output (pin 6) to V_{SS}. In this mode, the L1 through L8 channel outputs will change immediately after the entry of a single digit on the transmitter keys. The M1 through M8 outputs are not used in this mode. (See Figure 6.)

TABLE 2 – Command Codes

Function Bit	MSB	MSB – 1	LSB + 1	LSB	Command
0	0	0	0	0	Channel Digit 0
0	0	0	0	1	Channel Digit 1
0	0	0	1	0	Channel Digit 2
0	0	0	1	1	Channel Digit 3
0	0	1	0	0	Channel Digit 4
0	0	1	0	1	Channel Digit 5
0	0	1	1	0	Channel Digit 6
0	0	1	1	1	Channel Digit 7
0	1	0	0	0	Channel Digit 8
0	1	0	0	1	Channel Digit 9
0	1	0	1	0	Channel Digit 10
0	1	0	1	1	Channel Digit 11
0	1	1	0	0	Channel Digit 12
0	1	1	0	1	Channel Digit 13
0	1	1	1	0	Channel Digit 14
0	1	1	1	1	Channel Digit 15
1	0	0	0	0	Channel Search Down
1	0	0	0	1	Channel Search Up
1	0	0	1	0	Fine Tuning Down
1	0	0	1	1	Fine Tuning Up
1	0	1	0	0	Miscellaneous Command Spare
1	0	1	0	1	Miscellaneous Command Spare
1	0	1	1	0	Volume Down
1	0	1	1	1	Volume Up
1	1	0	0	0	Mute On/Off
1	1	0	0	1	Set Off
1	1	0	1	0	Miscellaneous Command Spare
1	1	0	1	1	Miscellaneous Command Spare
1	1	1	0	0	Miscellaneous Command Spare
1	1	1	0	1	Miscellaneous Command Spare
1	1	1	1	0	Miscellaneous Command Spare
1	1	1	1	1	Miscellaneous Command Spare

FIGURE 3 – Typical Ultrasonic System

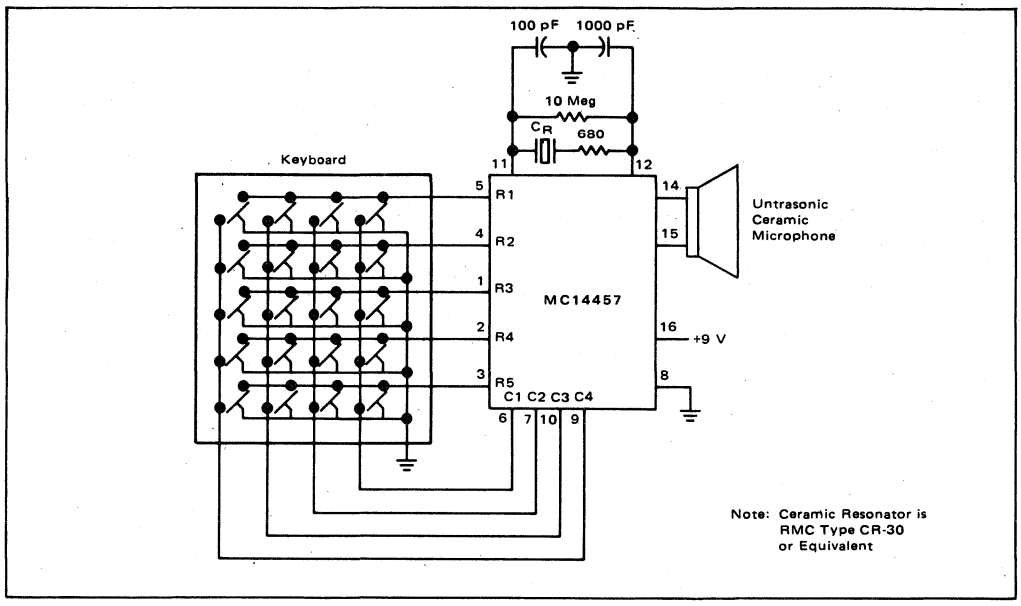


FIGURE 4 – Typical Infrared System

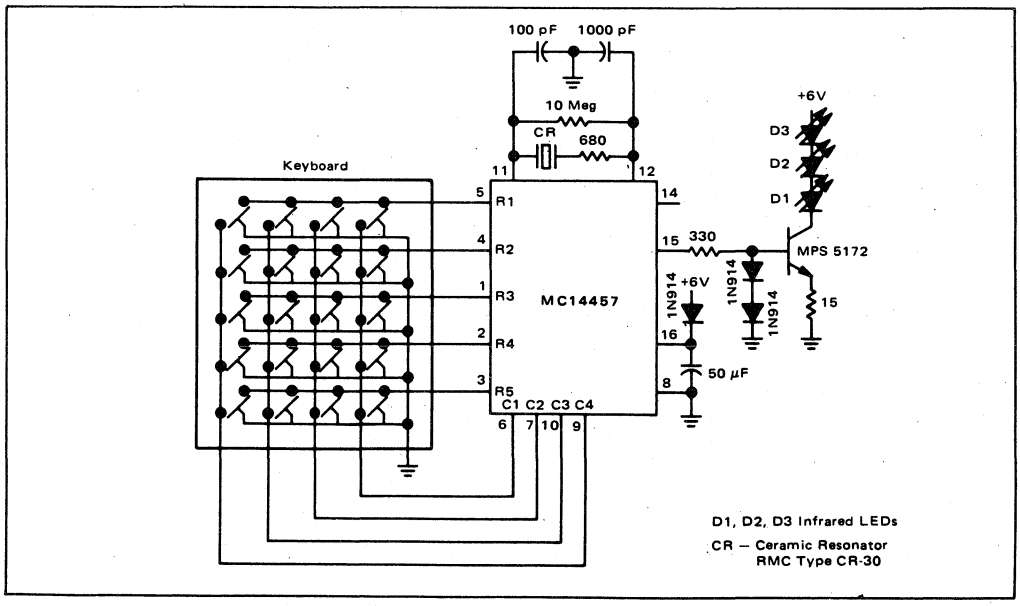
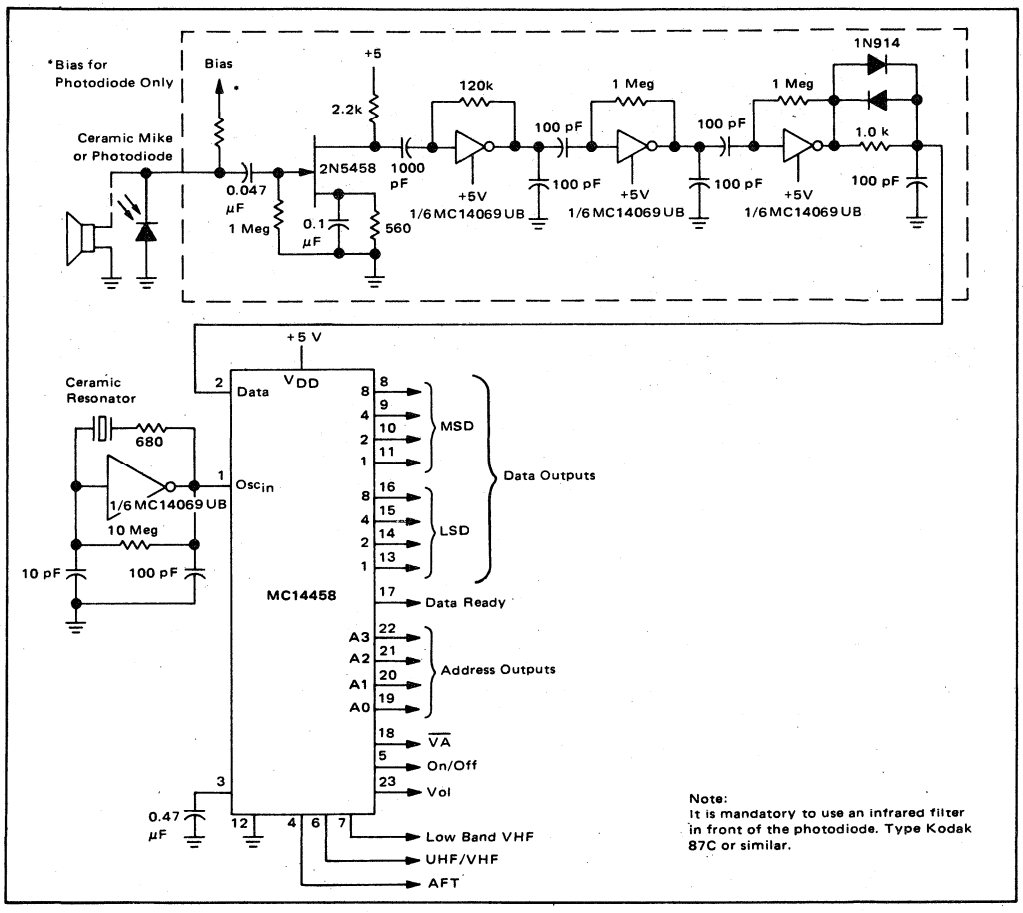


FIGURE 5 – Typical Remote Control Receiver Circuit Diagram



Application Information

Typical circuits for the transmitter and receiver chips are shown in Figure 3 through 8.

The transmitters, with the keyboard shown, transmit the first twenty codes from Table 1. The circuits of Figure 3 transmit via ultrasonic; whereas, the circuit of Figure 4 transmits infrared light. In Figure 3, push-pull output at pins 14 and 15 allows a balance drive to the ceramic microphone, which virtually doubles the transmitted power, compared to a single-ended output.

The diagram in Figure 5 shows an amplifier connected to a remote receiver. The bias resistor (photodiode) of the amplifier requires bias. The bias voltage is determined by the choice of photodiode and system considerations such as ambient light. Most of the required gain is realized using three of the four hex inverters in the MC14069UB package. A fourth inverter from the same package operates a 500 kHz oscillator circuit.

Figure 6 shows a block diagram of a PLL system. The receiver directly addresses a synthesizer. In this diagram, a complete command consists of two channel digits followed by an Enter code. The Enter code into the synthesizer is a 0101 in complementary logic. The transmitted code from the transmitter is 1010, which is Function 10 from Table 1.

A block diagram of a tuning address system is shown in Figure 7. This block diagram incorporates a one-chip microcomputer that would be programmed to the system's needs. The system can be expanded up to 256 channels.

FIGURE 6 – Block Diagram of a PLL System

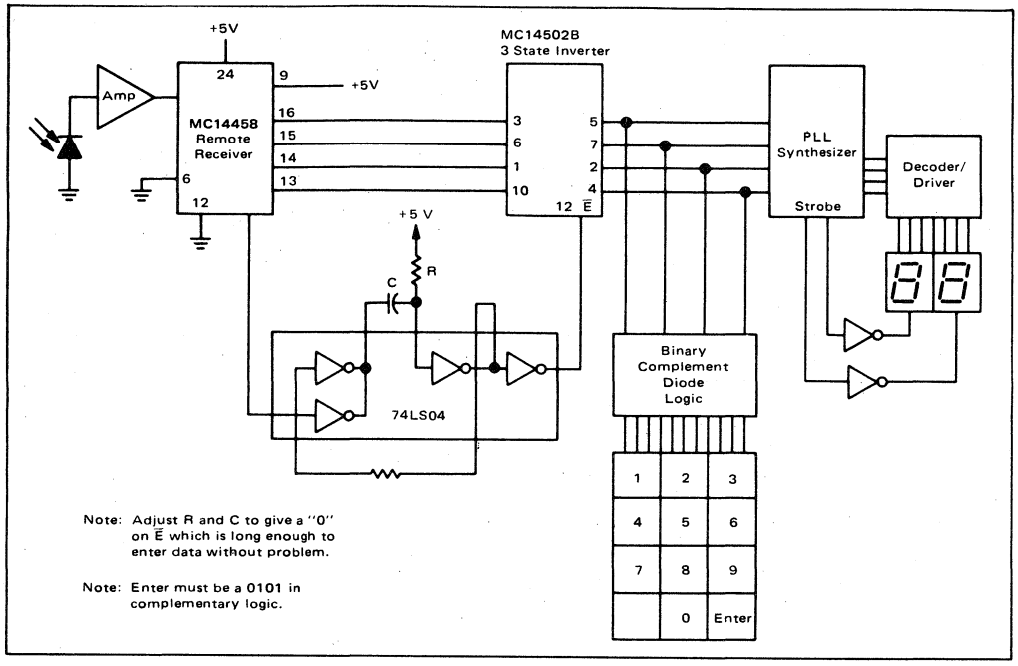
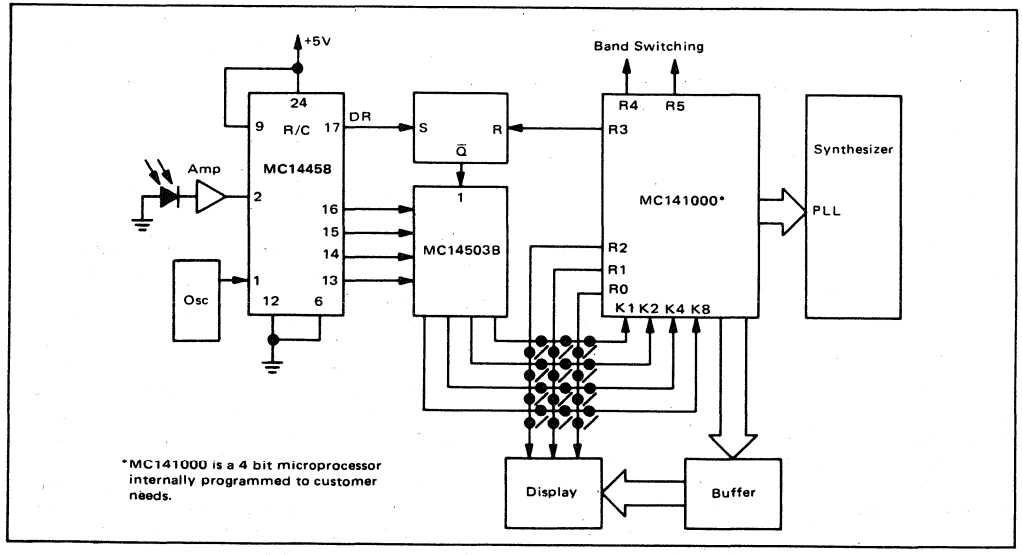


FIGURE 7 – Block Diagram of a Tuning Address System For Up To 256 Channels



MOTOROLA

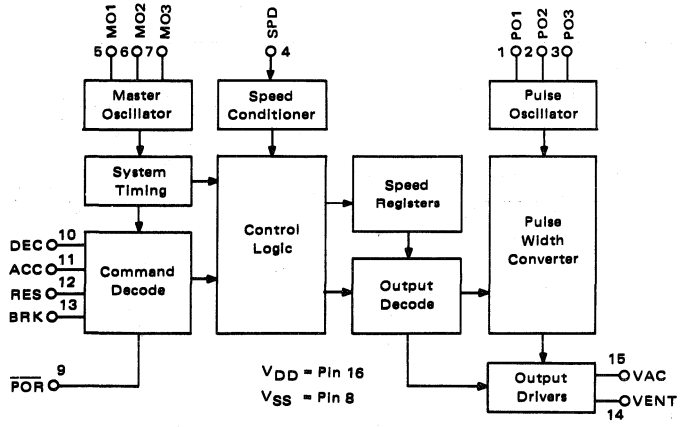
MC14459
MC14459A

AUTOMOTIVE SPEED CONTROL PROCESSOR

The MC14459 (&14459-A) device is designed to measure vehicle speed and provide pulse-width modulated outputs to trim a throttle positioning servo to maintain an internally stored reference speed.
The stored reference speed can be altered by the DECEL and ACCEL driver commands. The DECEL command trims down the speed, while ACCEL trims up the speed.
A BRAKE input is provided to turn off the outputs with a RESUME driver command to return the vehicle to the last stored speed.

- On-Chip Master Oscillator for System Time Reference
- Separate On-Chip Pulse Oscillator for Output Pulse Width Adjustment (Analogous to System Gain)
- Diode Protection on All Inputs
- Internal Redundant Brake and Minimum Speed Checks
- Acceleration Rates Controlled During ACCEL and RESUME Modes of Operation
- Low Frequency Speed Sensors Used
- No Throttle Position Feedback Required
- Power-On Reset
- Buffered Outputs Compatible with Discrete Transistor Driver Interface
- Low Power Dissipation
- Internal 4 x multiplier on Speed Input
- MC14459A has Internal 2 x multiplier on Speed Input.

BLOCK DIAGRAM

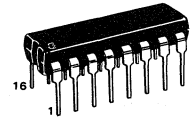


McMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

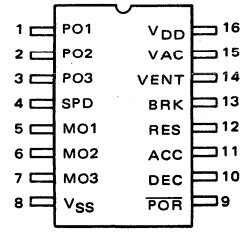
AUTOMOTIVE SPEED CONTROL PROCESSOR

(METRIC SPEEDS)



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltage referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +5.0	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Maximum Reverse Supply Current	I_{DD}	50	mAdc

ELECTRICAL CHARACTERISTICS (T_A = −40°C to +85°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Supply Voltage Pin 16	V_{DD}	–	5.0	5.6	6.0	Vdc
Output Voltage Pins 1, 2, 5, 6, 14, 15	V_{OL}	5.0	–	–	0.5	Vdc
	V_{OH}	5.0	5.0	–	–	Vdc
Input voltage Pins 3, 4, 7, 10, 11, 12, 13	V_{IL}	5.0	–	–	1.5	Vdc
	V_{IH}	5.0	3.5	–	–	Vdc
Input voltage Pin 9	V_{IL}	5.0	–	–	1.2	Vdc
	V_{IH}	5.0	3.2	–	–	Vdc
Input Hysteresis Pin 4 ($V_{IH} - V_{IL}$)	HYS	–	0.25	–	–	Vdc
Output Drive Current Pins 1, 2, 5, 6 V_{OH} = 4.6 Vdc	I_{OH}	5.0	−0.44	−0.88	–	mAdc
V_{OL} = 0.4 Vdc	I_{OL}	5.0	+0.44	+0.88	–	mAdc
Pins 14, 15 V_{OH} = 2.5 Vdc, V_{OL} = 0.4 Vdc	I_{OL} I_{OH}	5.0 5.0	+0.11 −2.0	+0.22 −4.0	–	mAdc mAdc
Input Current Pins 3, 4, 7, 10, 11, 12, 13 V_{IL} = 0.0 Vdc	I_{IL}	6.0	–	–	−1.0	μAdc
V_{OH} = 6.0 Vdc	I_{IH}	6.0	–	–	+1.0	μAdc
Pin 9 V_{IL} = 0.0 Vdc	I_{IL}	6.0	−50	−100	−200	μAdc
V_{IH} = 6.0 Vdc	I_{IH}	6.0	–	–	+1.0	μAdc
Supply Current Pin 16 (Both Oscillators Active, VAC and VENT Outputs High)	I_{DD}	6.0	–	0.6	10	mAdc

FIGURE 1 – SYSTEM TIMING

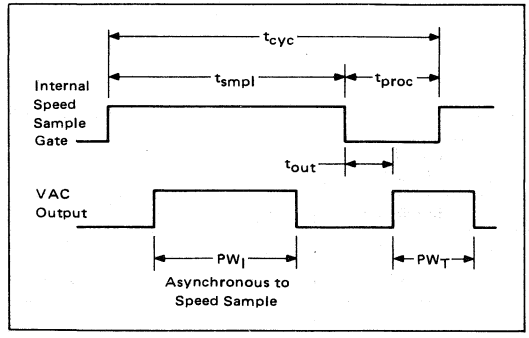
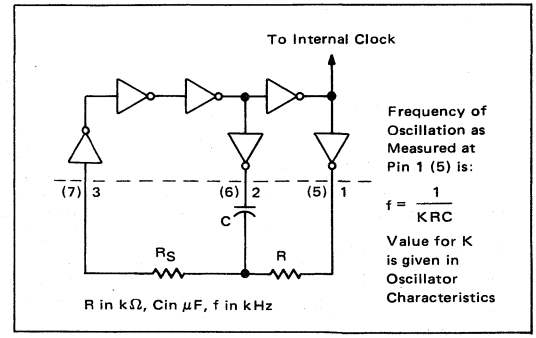


****FIGURE 2 – OSCILLATORS**



SWITCHING CHARACTERISATIONS (T_A = 25 °C, V_{DD} = 5 Vdc, FM = 2850 Hz, FP = 1600 Hz)

Characteristics		Symbol	Min.	Typ.	Max.	Unit
ACCEL Input Hold Time		t_{ACC}	16/fm	5.6	–	mS
DECEL Input Hold Time		t_{DEC}	16/fm	5.6	–	mS
RESUME Input Hold Time		t_{RES}	10	4	–	μS
BRAKE Input Hold Time		t_{BRK}	10	1	–	μS
Speed Input Frequency	14459-A 14459	fs	–	–	1425 712	Hz
Speed Sample Time (1008/fm)		t_{smpl}	–	353.7	–	mS
Speed Processing Time (16/fm)		t_{proc}	–	5.6	–	mS
System Cycle Time (1024/fm)		t_{cyc}	–	359.3	–	mS
Output Delay Time (9/fm)		t_{out}	–	3.2	–	mS
Output Pulse Width (proportional to 1/fp) Initializations		PW_T	280	–	960	mS
Trim Outputs		PW_T	10	–	80	mS

OSCILLATOR CHARACTERISTICS (R_{EXT} = 100K, R_S = 10K) (See Figure 2)

Parameter	Symbol	V_{DD}	Min.	Typ.	Max.	Unit
Oscillator Frequency Factor for fm and fp	K	5.0	–	2.43	–	–
Frequency Deviation vs Part-Part Processing	ΔP	5.0	−1.0	0	+1.0	%
Frequency Deviation vs Supply Voltage (V_{DD} = 4.5-6.0 Vdc) Refer to 5.0 Vdc Value	ΔV	–	–	–	2.0	%/Vdc
Frequency Deviation vs Temperature (−40 to +85 °C)	ΔT	5.0	–	–	100	ppm/°C
Frequency of Oscillation	f (max.)	–	–	–	20	kHz
Drive Impedance (Each Output)	R_{out}	5.0	225	450	900	OHM

Note:
Lower values of external resistance will increase the effects of drive impedance variations on the frequency of oscillation. All of the above variations are in part due to this phenomenon.

SYSTEM PERFORMANCE (T_A = 25 °C, V_{DD} = 5 Vdc, fm = 2850 Hz, f_s = 1.13 Hz/KPH (459), f_s = 2.26 Hz/KPH (459-A)

Characteristics	MC14459 Formulae	MC14459-A Formulae	Symbol	Typical	Unit
Speed Resolution	fm/4032 fs	fm/2016 fs	S_{RES}	0.63	KPH
Minimum Operating Speed	fm/84 fs	fm/42 fs	S_{MIN}	30	KPH
Maximum Stored Speed	fm/12.6 fs	fm/6.3 fs	S_{MAX}	200	KPH
Controlled Acceleration Rate					
(ACCEL or RESUME Modes)	$(fm)^2/(7.43)\ (10^6)$ fs	$(fm^2)/(3.72)\ (10^6)$ fs	A	0.97	M/SEC^2
Redundant Brake Speed Drop Below					
Reference Speed	−fm/84 fs	−fm/42 fs	S_{RB}	−30	KPH
Speed Deviation					
Assumes Suitable Mechanical		Automatic	ΔS_N	±1	KPH
Hook-Up and Pulse Oscillator		Transmission			
Frequency Adjusted to Suit			ΔS_T	±3	KPH
Throttle Servo Requirements					
ΔS_N Level Road (no wind ±1% grades)		Manual	ΔS_N	±2	KPH
ΔS_T Transient Road Conditions		Transmission			
(±15 KPH winds, ±7% grades)			ΔST	±4	KPH
Stored Speed Accuracy					
Steady-State (Acceleration = 0)			R_{SS}	±0.63	KPH
Transient (Acceleration = ±A m/sec^2)			R_{ST}	±1.26A	KPH

TRUTH TABLE

Output		
VAC	VEN	Servo Drive
0	0	Decrease Speed
0	1	Hold Speed
1	0	Invalid O/P
1	1	Increase Speed

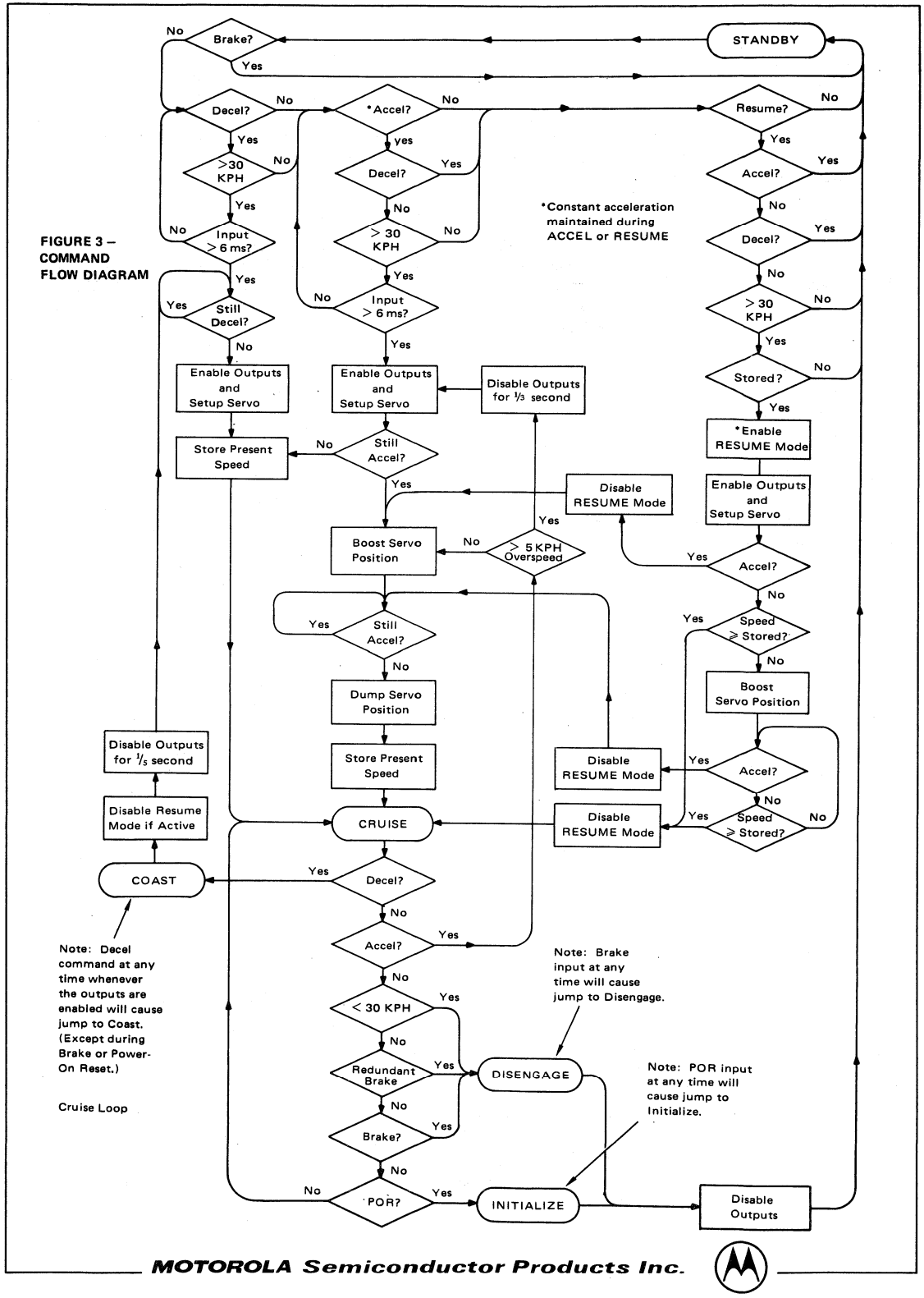


FIGURE 3 – COMMAND FLOW DIAGRAM

DEVICE OPERATION

PULSE OSCILLATOR (PO1, PO2, PO3; Pins 1, 2, 3)

These pins are the output pins of the output Pulse Oscillator, which is a three-terminal RC type. See Figure 2 for design parameters. This oscillator sets the relative pulse width of the VAC and VENT outputs.

SPEED (SPD, Pin 4)

This is the Speed input to be controlled or stored. This input is level sensitive with hysteresis to allow use of slowly changing waveforms. Input frequency should never exceed ¼ the Master Oscillator frequency (f_M) for 14459 or ½ the Master Oscillator frequency for 14459-A.

MASTER OSCILLATOR (MO1, MO2, MO3; Pins 5, 6, 7)

The Master Oscillator is a three-terminal RC type. See Figure 2 for design parameters. This oscillator sets the master system timing.

POWER-ON RESET (POR, Pin 9)

This pin is the Power-On Reset input. As long as this input is LOW, the internal system is cleared and the VAC and VENT outputs are disabled. An internal pullup device will source 50-200 μAdc of current from this pin to allow capacitor charging for automatic power-on reset.

DECEL (DEC, Pin 10)

This is the DECEL command input. When held HIGH both VAC and VENT outputs will be LOW. When the DECEL input returns LOW the last sample of the SPD input will be stored as the reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

ACCEL (ACC, Pin 11)

This is the ACCEL command input. When held HIGH the VAC and VENT outputs will be modulated to maintain a fixed rate of acceleration. When the ACCEL input returns LOW the last sample of the SPD input will be stored as the reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

continued

THROTTLE SERVO

A. Two Coil Vacuum Powered

Truth Table:

VAC	VENT	Throttle
Coil	Coil	Action
Off	Off	Release
Off	On	Hold
On	Off	Weak Pull
On	On	Pull

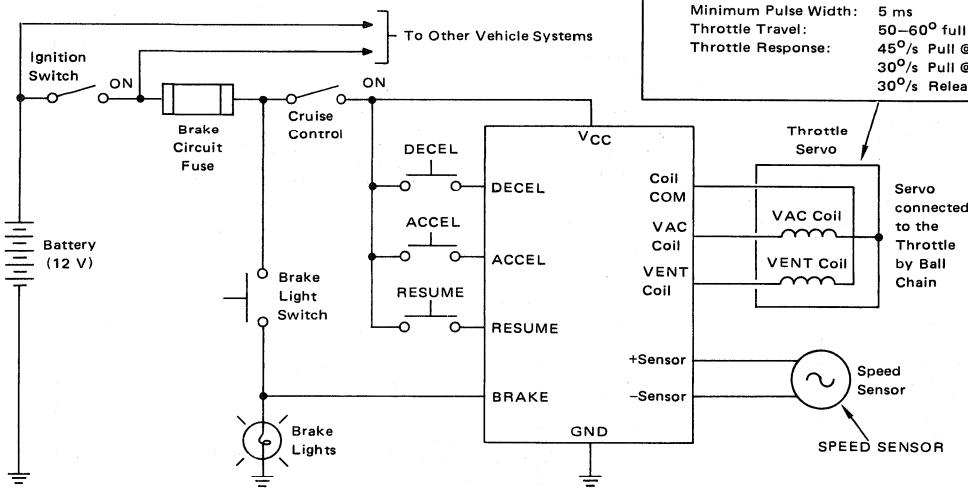
B. Coil Type

Coil Impedance: 80–90 Ω
Coil Inductance: 125–150 mH

C. Servo Response

Minimum Pulse Width: 5 ms
Throttle Travel: 50–60° full travel
Throttle Response: 45°/s Pull @ 12" VAC
30°/s Pull @ 7" VAC
30°/s Release

FIGURE 4 – TYPICAL AUTOMOTIVE CRUISE CONTROL APPLICATION



Electromagnetic Type for MC14459-A

Poles: 8/revolution
Output Freq.: 2.26 Kz/KPH (8136 pulse/KM)
Output Voltage: 2.0 V p-p @ 30 KPH
Max. Freq.: 1425 Hz (630 KPH)
DC Resistance: <40Ω

Electromagnetic Type for MC14459

Poles: 4/revolution
Output Freq.: 1.13 Hz/MPH (4068 pulses/km)
Output Voltage: > 2.0 Vp-p @ 30 KPH)
Max. Freq.: 712 Hz (630 KPH)
DC Resistance: <40Ω

DEVICE OPERATION continued

RESUME (RES, Pin 12)

This is the RESUME command input. When taken HIGH the system will lock into a mode where the VAC and VENT outputs are modulated to maintain a fixed rate acceleration. This acceleration ends when the SPD input sample matches the stored reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

BRAKE (BRK, Pin 13)

This is the BRAKE command input. When this input is taken HIGH the system is disabled (both VAC and VENT outputs LOW) until a DECEL, ACCEL, or RESUME command is received. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

VENT (Pin 14)

This is the VENT output. See Truth Table for operation.

VAC (Pin 15)

This is the VAC output. See Truth Table for operation.

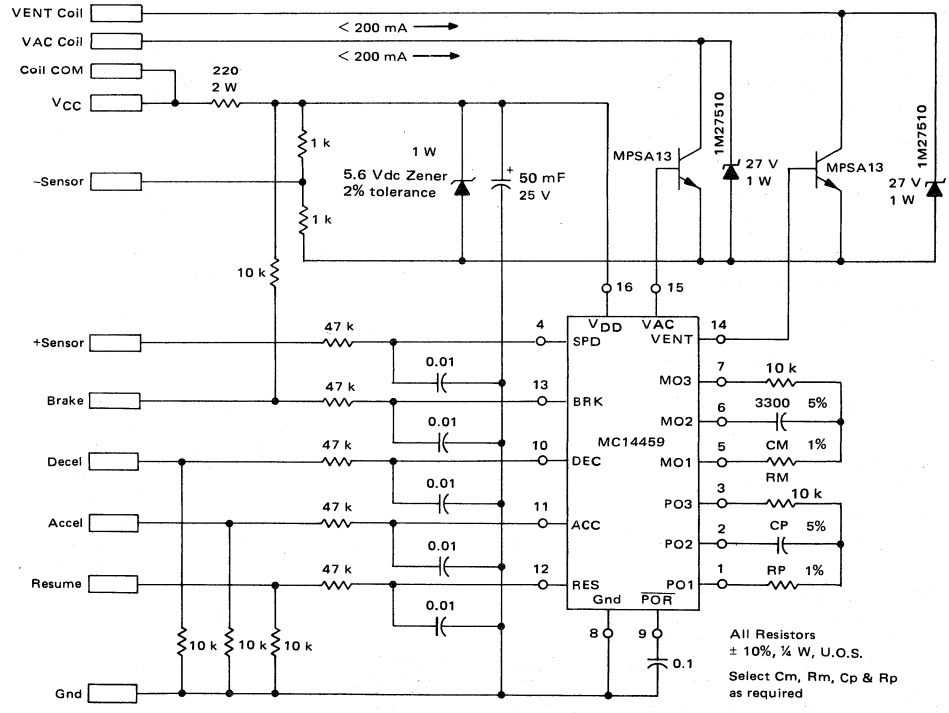
GROUND (V_{SS}, Pin 8)

Pin 8 is the ground connection for the package.

POSITIVE POWER SUPPLY (V_{DD}, Pin 16)

Pin 16 is the power supply connection for the package.

FIGURE 5 – PC BOARD MODULE FOR CRUISE CONTROL



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

Environment

Ambient Temperature (T_A)	$-40^{\circ}C$ to $85^{\circ}C$
V_{CC} Operating Range	11–15 Vdc
V_{CC} Transients	9–16 Vdc
Load Dump	80 V Peak decaying to 12 V in < 200 ms
Inductive	±300 V Peak decaying in < 1 ms
Jump Start	+24 Vdc for 5 min.
Reverse Battery	-12 Vdc continuous

MOTOROLA

MC14461
MC14462

SMOKE DETECTOR CIRCUIT

The MC14461 and MC14462 are smoke detector circuits fabricated using Motorola's standard CMOS process. The MC14461 has the detector input with the standard CMOS static protection. The MC14462 has an unprotected CMOS (MOSFET) input which is protected during shipment by a shorting bar. The shorting bar is broken after inserting into the final circuit. The shorting bar connects the detector input to a special ACTIVE guard pin. This ACTIVE guard reduces package leakage to the detector pin and also may be used to reduce circuit leakage to the detector. A wide range of operating versatility is designed into the integrated circuit to accommodate various smoke detector designs. Special timing has been incorporated to reduce or eliminate transient suppression capacitance.

The MC14461 is recommended for use with an FET interfacing the ion chamber to the MC14461. The MC14462 is recommended for direct interconnection to a single or dual ionization chamber.

- Meets UL217 Requirements – UL Recognized Component
- On-Chip FET (MC14462)
- On-Chip ACTIVE Guard (MC14462)
- 9 or 12.6 Volt Battery Operation
- Low Voltage Beep Alarm
- Two Mode Battery Test Option –
  DC Test, No Load
  Pulse Test, Under Load
- Typical Quiescent Current at 9 Volts
  6 μA for DC Battery Test Mode
  8 μA for Pulse Battery Test Mode
- On-Chip Osc Using 0.0018 μF Capacitor
- On-Chip Horn Predriver
- On-Chip Pulse Test Load Predriver
- On-Chip Zener Reference
- Multiple Unit Operation, Common Annunciator (MC14461)
- Adjustable Pulse Width Ranges for Beeping and
  Battery Test Sampling

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +15	Vdc
Input Voltage, All Inputs	V_{in}	-0.25 to V_{DD} +0.25	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	30	mAdc
Operating Temperature Range	T_A	0 to +50	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

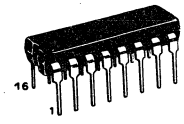
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

SMOKE DETECTOR CIRCUIT

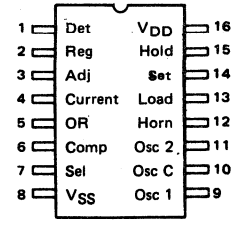
MC14462 – WITH ON-CHIP FET



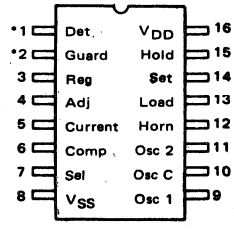
P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT

MC14461

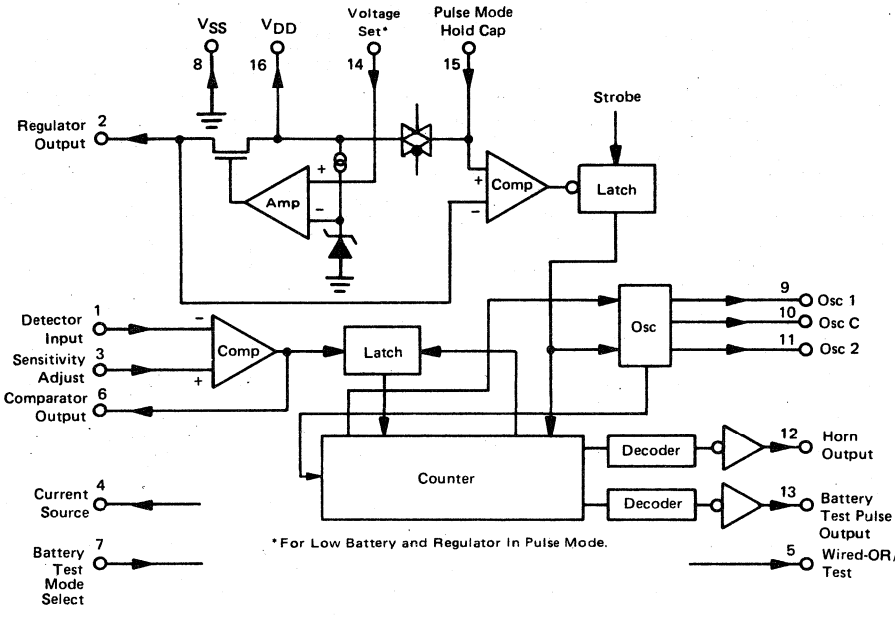


MC14462

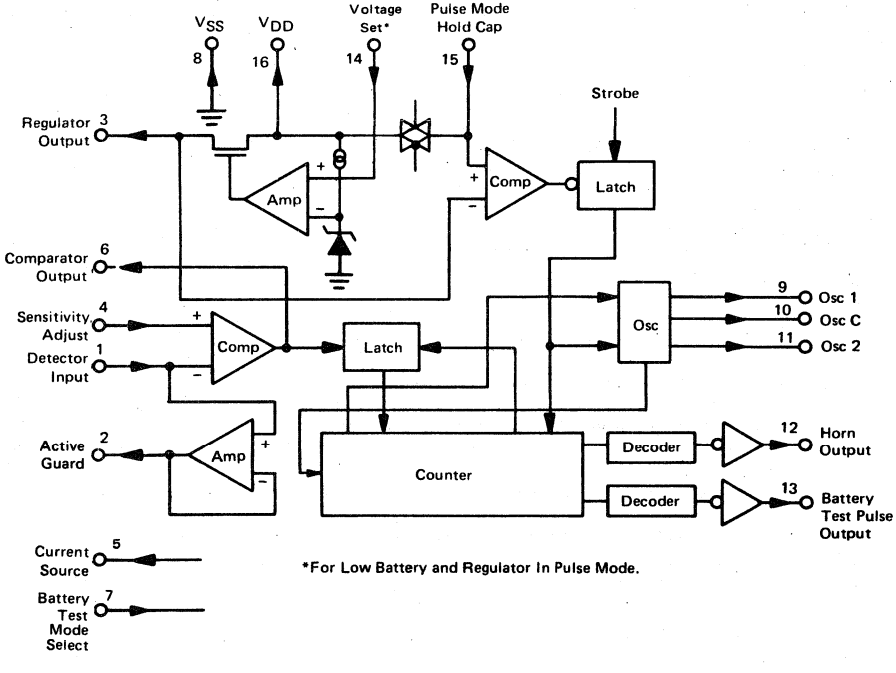


*Pin 1 shorted to Pin 2. The bar is removed after insertion into the circuit.

MC14461 BLOCK DIAGRAM



MC14462 BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Voltage referenced to V_{SS})

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0 to 14	Vdc
Time Between Low Battery Detect Beep	T2	45	s
Beep Pulse Width	T1	11	ms

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Standby Current	I_T	9.0				μAdc
Static Mode (Refer to Figure 3a or 3b)			–	6.0	9.0	
(R1 = 10 kΩ, R2 = 22 MΩ, R4 = 10 MΩ, C = 0.0018 μF, Pin 7 = V_{DD})						
Pulse Mode (Refer to Figure 1a or 1b)			–	8.0	11	
(R1 = 270 kΩ, R2 = 22 MΩ, R3 = Open, R4 = 10 MΩ, C = 0.0018 μF, Pin 7 = V_{SS})						
Output Source Current–Horn or Pulse (V_{OH} = 0.7 Vdc)	I_{OH}	9.0	12	24	–	mAdc
Input Current	I_{in}	9.0				
Detect–MC14462P			–	–	1.0	pAdc
Detect–MC14461P			–	0.01	20	nAdc
Sensitivity Adjust			–	0.01	20	nAdc
Pins 14 and 15			–	0.1	20	nAdc
Pin 7			–	0.0001	1.0	μAdc
Detector Common Mode Range	V_{CMR}	9.0	2.0	–	8.5	Vdc
		6.0	2.0	–	5.5	
Detector Input Offset Voltage (V_{in} = 4.5 V)	V_{Off}	9.0	–	±8.0	±50	mVdc
Reference Voltage	V_R					Vdc
Minimum Regulated		9.0	6.9	7.2	7.5	
(I_{Reg} = 7.0 μA (Note 1), V_{Reg} connected to Voltage Set)						
Below Regulation		6.0	5.86	5.90	–	
(I_{Reg} = 5.0 μA, V_{Reg} connected to Voltage Set)						
Low Battery Detect Level (Notes 1 and 2)	V_{Low}	–				Vdc
Static Mode			7.2	7.5	7.8	
Pulse Mode			6.9	7.2	7.5	
Comparator Output Drive Current		9.0				μAdc
(V_{OH} = 8.0 V)	I_{OH}		-25	–	–	
(V_{OL} = 1.0 V)	I_{OL}		50	–	–	
Common Annunicator–ON–Output Voltage–MC14461 (R_L = 100 k, Note 6)	V_{OH}	7.0	6.3	–	–	Vdc
Common Annunciator–ON–Input Voltage–MC14461 (R_L = 100 k, Note 6)	V_{IH}	9.0	6.3	–	–	Vdc
Common Annunicator–Output Duty Cycle–MC14461	–	9.0	–	50	–	%
ACTIVE Guard to Detector–MC14462–Note 4						mVdc
Input–Voltage Difference						
(V_{in} = 2.0 – 6.5 V)		7.0	–	–	±100	
(V_{in} = 2.0 – 8.5 V)		9.0	–	–	±100	

NOTES:

1. Regulator voltage adjustable above minimum by resistor setting. See Figures 2a, 2b, 3a, and 3b.
2. For low battery detect level, the zener diode circuitry requires the supply voltage to be 0.3 volt above the internal zener diode. This requirement translates into the low battery voltage. Set point in static mode must be 0.3 volt greater than the internal voltage. In the pulse mode, the pulse current must pull the battery down 0.3 volt if the minimum level is to be used. See circuit diagrams for further clarification.
3. The timing is adjustable and governed by the equations of page 6.
4. The ACTIVE guard can drive capacitance loads or high resistance to a ground. The ACTIVE guard can also be used to measure the chamber voltage without loading the chamber.
5. Pulse current can be used to drive an LED. Limit output to maximum ratings.
6. The two specifications given, warrant the operation of one smoke detector with a low battery of 7 volts, having the ability to turn on a smoke detector with a battery voltage of 9 volts. An option to add common annunciator on the MC14462 on Pin 6 replacing the comparator output. Consult factory for this special order.

MC14461

FIGURE 1a – SMOKE DETECTOR CIRCUIT USING PULSE MODE BATTERY TEST WITH LEVEL LOW BATTERY DETECTION AT INTERNAL ZENER VOLTAGE

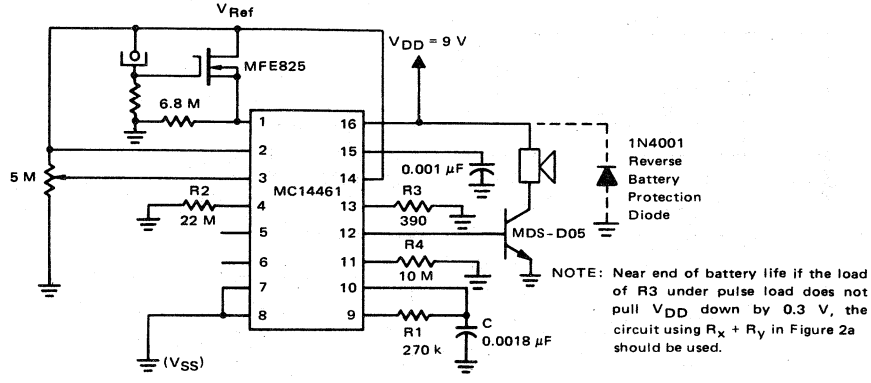


FIGURE 2a – SMOKE DETECTOR CIRCUIT USING PULSE MODE BATTERY TEST WITH ADJUSTABLE VOLTAGE FOR LOW LEVEL BATTERY DETECTION

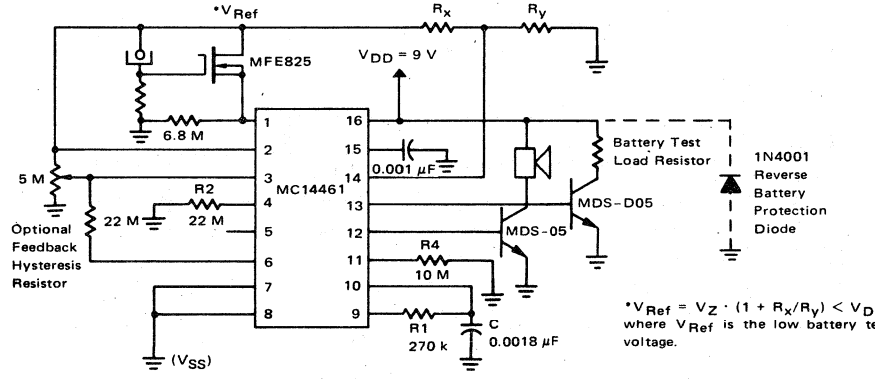
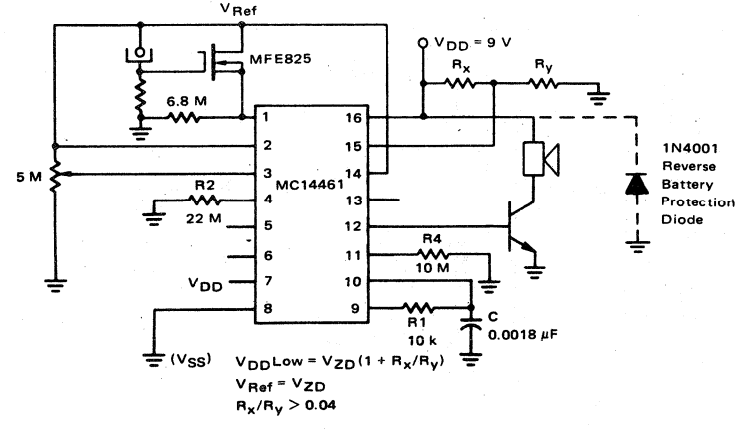


FIGURE 3a – SMOKE DETECTOR CIRCUIT USING STATIC MODE AND INTERNAL ZENER VOLTAGE EQUAL TO REGULATED VOLTAGE



MC14462

FIGURE 1b – SMOKE DETECTOR CIRCUIT USING PULSE MODE BATTERY TEST WITH LEVEL LOW BATTERY DETECTION AT INTERNAL ZENER VOLTAGE

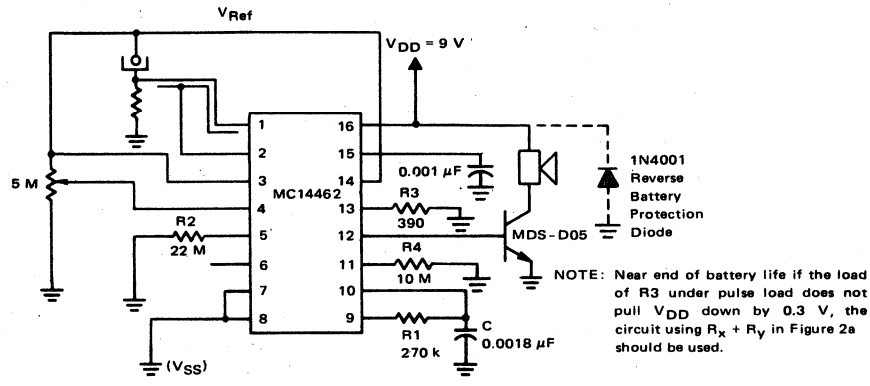
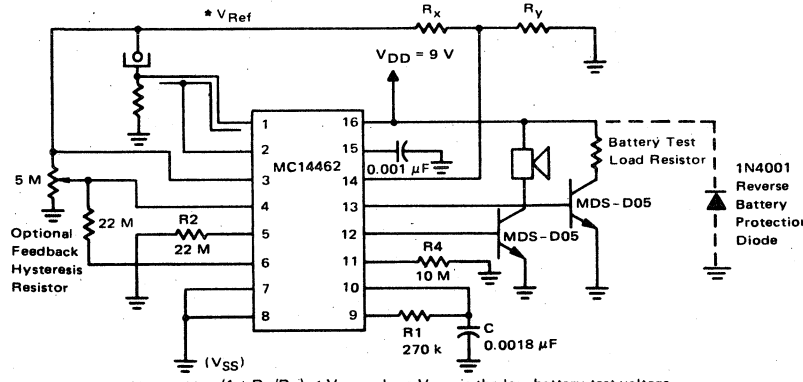
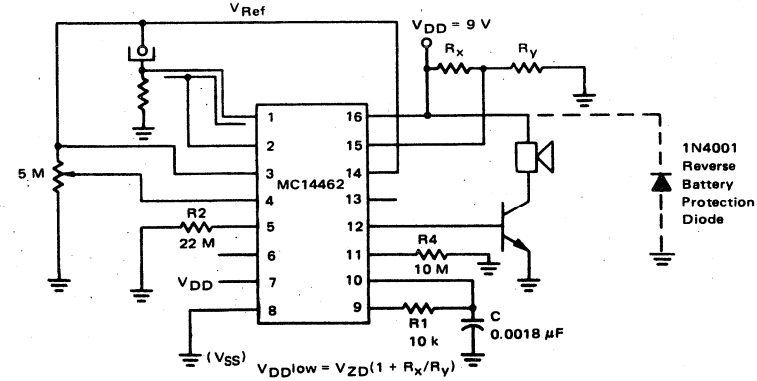


FIGURE 2b – SMOKE DETECTOR CIRCUIT USING PULSE MODE BATTERY TEST WITH ADJUSTABLE VOLTAGE FOR LOW LEVEL BATTERY DETECTION

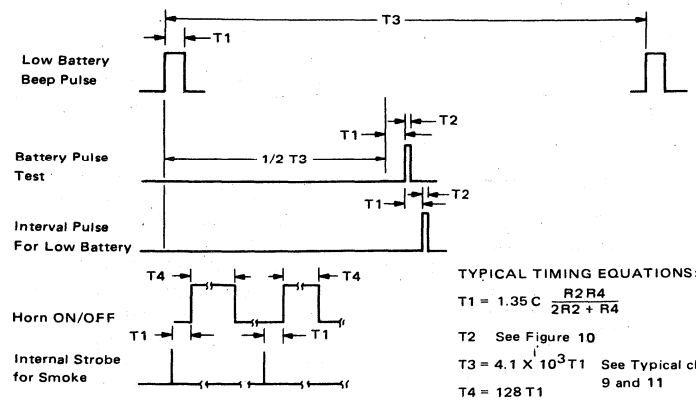


*$V_{Ref} = V_Z \cdot (1 + R_x/R_y) < V_{DD}$, where V_{Ref} is the low battery test voltage.

FIGURE 3b – SMOKE DETECTOR CIRCUIT USING STATIC MODE AND INTERNAL ZENER VOLTAGE EQUAL TO REGULATED VOLTAGE



TIMING DIAGRAM



TYPICAL TIMING EQUATIONS:

$T1 = 1.35\,C\,\frac{R2\,R4}{2R2 + R4}$

T2 See Figure 10

$T3 = 4.1 \times 10^{3} T1$ See Typical characteristic curves, Figure 9 and 11

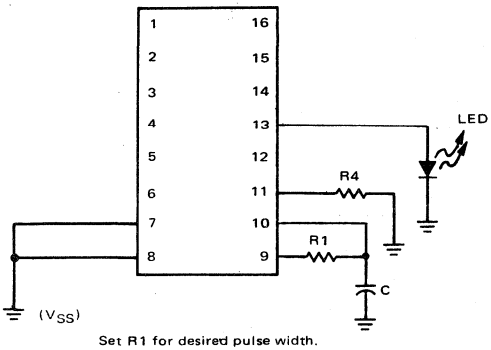
T4 = 128 T1

NOTE: Circuits with the low battery beep pulse of 2T1, or 4T1 are available on special order. Consult factory for minimum order required.

OPERATIONAL DESCRIPTION

MC14461	MC14462	
Pin 1	Pin 1	**Detector Input.** Accepts a negative direction signal for smoke. Input for the MC14461 has the standard CMOS diode-resistor protection. Input for the MC14462 does not have the protection network.
–	Pin 2	**Active Guard.** This pin provides an active guard that tracks the detector input. This output may be used to measure chamber voltage level.
Pin 2	Pin 3	**Regulator Output.** Output of a series-type regulator. This output regulates until battery falls below regulator setting. After that, the regulator equals the battery output to within 100 mV.
Pin 3	Pin 4	**Sensitivity Adjust.** Accepts a voltage, usually from a potentiometer, at which the Detector Input switches. Switching occurs within ±50 mV of the voltage and the Detector Input.
Pin 4	Pin 5	**Current Source.** Sets the quiescent current for the internal amplifiers. Values between 10 and 22 megohms are recommended.
Pin 5	–	**Wired OR/Test.** For common annunciation, this pin together with ground (V_{SS}) may be connected to a large number of units in common. Any unit going high at this pin will turn on all units. This pin may also be used as a test pin with an SPST switch between this pin and V_{DD}. The output is the 50% ON/OFF duty cycle of the horn.
Pin 6	Pin 6	**Comparator Output.** May be used in testing circuit. May also be used with a resistor to Pin 1 to obtain hysteresis between smoke detection turn-on and turn-off. V_{DD} level represents Smoke and ground level represents No-Smoke.
Pin 7	Pin 7	**Battery Test Mode Select.** When connected to V_{SS}, the circuit operates in pulse-testing mode for low battery detection. When wired to V_{DD}, the circuit operates in the static (dc) mode to test for low battery.
Pin 8	Pin 8	V_{SS}. Negative Battery Terminal.
Pin 9	Pin 9	**Osc 1.** The resistor connected to this pin and the capacitor controls the time to sample the battery for the low battery pulse test mode operation. See typical timing diagrams and equations.
Pin 10	Pin 10	**Osc C.** Timing capacitor is connected to this pin. The value of this capacitor is related to the value of the resistor on Pins 4 and 11.
Pin 11	Pin 11	**Osc 2.** A resistor connected to this pin will determine the period of oscillation. See typical curves and timing equations.
Pin 12	Pin 12	**Horn Output.** This terminal sources current of 12 mA when the horn is turned on. When the horn is turned off, this terminal is shorted to ground. An NPN transistor may be directly driven from this pin. The horn operates on a 50% duty cycle, for example, 1.3 seconds ON, 1.3 seconds OFF.
Pin 13	Pin 13	**Battery Test Pulse Output.** For pulse loads to 12 mA, a resistor to ground is recommended. For pulse loads greater than 12 mA, an NPN transitor with a resistive load is recommended. The terminal is normally connected to ground potential internally.
Pin 14	Pin 14	**Voltage Set for Regulator Output.** This teminal is the input to set the level for the voltage of the regulator output. When this pin is connected directly to Pin 2, the regulated output and the low voltage level is set at the internal zener diode voltage, nominally 7.2 volts. When a resistive divider is used, the regulated voltage can be set above the zener diode voltage level.
Pin 15	Pin 15	**Pulse Mode Hold Cap.** When using low battery pulse mode operation, this pin requires a non-critical value capacitor, typically 0.001 μF. The battery voltage is sampled during the load pulse time and the information is held and used after the load pulse time. This operation eliminates the effects of load transients.
Pin 16	Pin 16	V_{DD}. Positive Battery Terminal.

FIGURE 4 – CIRCUIT WITH PULSING LED ADDED
(Pulse Mode Only)



Set R1 for desired pulse width.

CIRCUIT DESCRIPTION

The MC14461 and MC14462 are integrated circuits for use with smoke detectors. The circuits are primarily used with ionization-type smoke detectors operating at 9 volts, but are also readily adaptable to the higher 12.6-volt operation. For battery operation, the circuits may be operated in the pulse battery test mode or in the DC test mode. In the pulse test mode, the on-chip oscillator runs continuously, requiring an added 2 μA. In this mode, both the pulse width for sampling and the pulse load current are selectable by resistors. In the DC battery test mode, the on-chip oscillator only operates when the battery is low or smoke is detected. For both operating modes, the voltage threshold at low battery is externally selectable by two resistors. The oscillator operates through a multistage counter to obtain sampling rates of, for example, 40 seconds, while allowing beep-alarm pulses of, for example, 10 milliseconds and battery test pulses of 0.5 milliseconds. The frequency of the oscillator is sufficiently high to avoid the use of costly high-value, less reliable capacitors.

The input of the MC14462 is an FET with high impedance for direct use with ionization chambers. Pins 1 and 2 are shorted together as protection during handling and testing.

The input of the MC14461 is protected against static discharge. An FET operated in source-follower mode may be connected to this input. The IC requires no more thar the standard precautions for the CMOS digital logic family.

The output for the horn and dummy load for pulse testing will source a minimum of 12 mA and may be used to drive an inexpensive transistor directly. An active n-channel transistor is used to pull down the output when the output is low. This transistor provides a ground path for the base of the driver transistor to keep that transistor off.

When greater than 12 mA is desired for pulse battery test, an external NPN transistor is required to drive the dummy load. Otherwise, a resistor load to ground is required.

The oscillator has a wide range of adjustments and requires a capacitor and resistor for setting the frequency. The resistor allows independent setting of the battery sample pulse width. The rate of the beep alarm and the pulse battery test are the same.

The MC14461 and MC14462 contain other internal features. There is internal latching that makes the circuit insensitive to transients due to battery test, horn-blowing, and beep alarm, in other words, when the battery is loaded down. The horn is turned on and off with the smoke-detection circuit, automatically reactivating during the off time. An external low-value capacitor, together with internal circuitry, delays the low-voltage battery measurement until after pulse battery load period. This capacitor stores the low-voltage information.

In the MC14461, a single pin controls a common annunciator circuit. If this pin and ground is wired common to a multiple set of units, a high-level signal turns on all units. Any unit may initiate all horns.

On-Chip FET–MC14462

The basic problems for on-chip FET can be summarized in the following two areas:

1. Protection of the input circuit during testing, packaging, and insertion.
2. Package pin-to-pin leakage current and circuit leakage current once installed.

An unprotected gate input, i.e., a gate input without diode protection network, has a very low probability of leakage unless that oxide is destroyed. To protect the gate through the functions of high-speed testing, packaging, and handling during insertion until connected to the chamber, a pin-to-pin shorting bar is used. This bar is clipped out after insertion into the circuit.

To reduce package pin-to-pin leakage and circuit leakages, an adjacent pin ACTIVE guard voltage is provided. This voltage follows the detector voltage guarding the input. The voltage is provided by an on-chip 1:1 amplifier. The circuit of Figure 5 shows such a circuit. The operational amplifier (Amp) in Figure 5 is connected as a 1:1 gain amplifier. In the ideal case, this means the voltage from Pin 1 to 2 is 0 and therefore leakage is 0. However, amplifiers are not ideal and the effectiveness of this amplifier is limited by its deviation from the ideal 1:1 gain.

Assume the leakage is presented by a resistance, R_X, with the operational amplifier having a gain, A, and an offset voltage, V_O. The guard voltage V_g in terms of the

CIRCUIT DESCRIPTION (continued)

detector input voltage, V_I, is given by the equation:

$$V_g = \frac{A}{1+A} V_I + \frac{A}{1+A} V_O$$

Normally, the leakage current, i_ℓ, is given by the equation:

$$i_\ell = \frac{V_I}{R_X};$$

whereas, the guard alters this equation as follows:

$$i_\ell = \frac{V_I}{R_X A} + \frac{V_O}{R_X}, \text{ when } A >> 1.$$

With respect to the first term, the leakage is reduced by the gain of the amplifier which is of the order of 10,000. The second term is dominant. With a worst case of 50 mV offset, the leakage is reduced by 100 for an input voltage of 5 volts. This factor of 100 worst-case is significant.

Since the guard is an amplifier output, this guard may be used in the circuit. It may be carried to the foil in the board. It may be connected to an enclosure pattern, enclosing both pin 1 and the pad for the wire leading to the ion chamber. Furthermore, it can be used as a guard connected to the chamber itself in a guard configuration within the chamber. See Figures 6 and 7.

With respect to the shorting bar protecting the input during test, packaging, and insertion, a shorting bar bridges pins 1 and 2. Pin 2 has natural diode protection due to the source-drain diodes at the output of the amplifier. Thus the circuit can be functionally tested for the input parameters such as the comparator detector level for smoke, etc. The guard and the input are fully connected in the final circuit before breaking the shorting bar.

This on-chip FET method allows for use of plastic packages leading to low-cost, system-effective smoke detector circuits.

FIGURE 5 – SMOKE DETECTOR WITH ACTIVE GUARD VOLTAGE

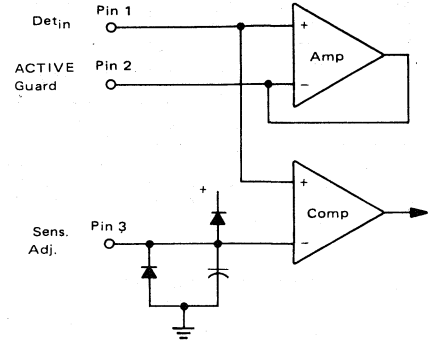


FIGURE 6 – PC BOARD LAYOUT WITH GUARD

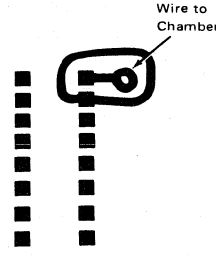


FIGURE 7 – PC BOARD LAYOUT WITH GUARD AND IONIZATION PELLET

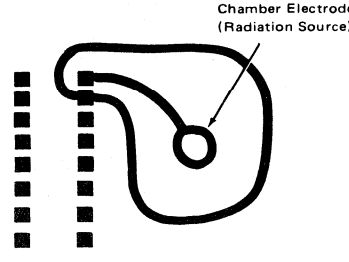


FIGURE 8 – TYPICAL HORN OR PULSE OUTPUT CHARACTERISTICS

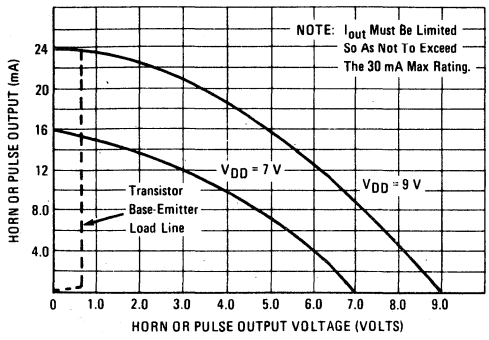


FIGURE 9 – TYPICAL TIME BETWEEN LOW BATTERY BEEP OR TEST PULSE versus TIMING CAPACITANCE

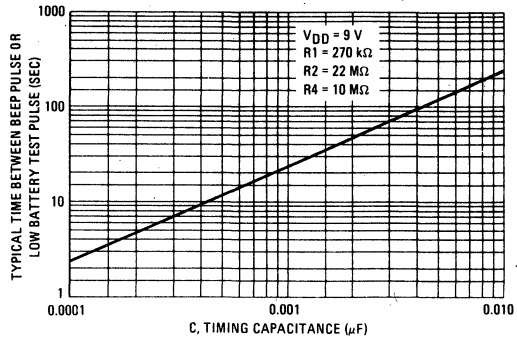


FIGURE 10 – TYPICAL TEST PULSE WIDTH IN PULSE MODE versus RESISTOR, R1

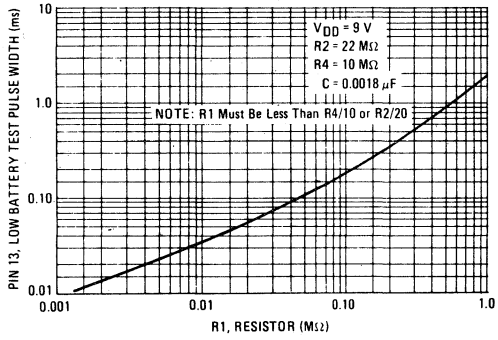


FIGURE 11 – TYPICAL TIME BETWEEN LOW BATTERY PULSES versus RESISTOR R4

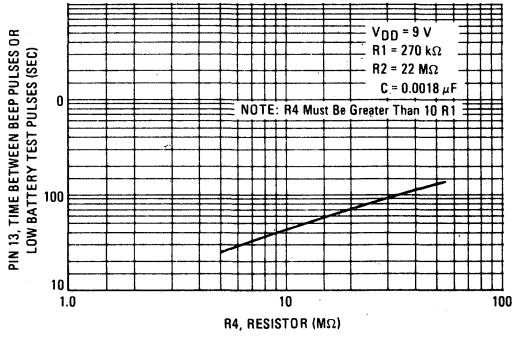


FIGURE 12 – TYPICAL REFERENCE OUTPUT versus SUPPLY VOLTAGE

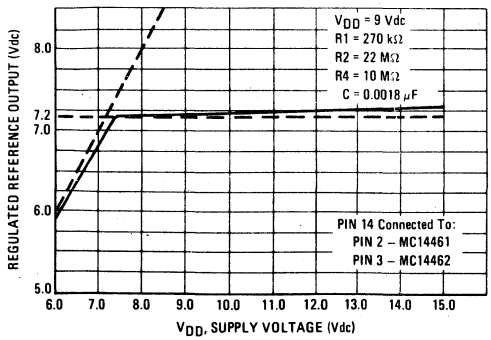
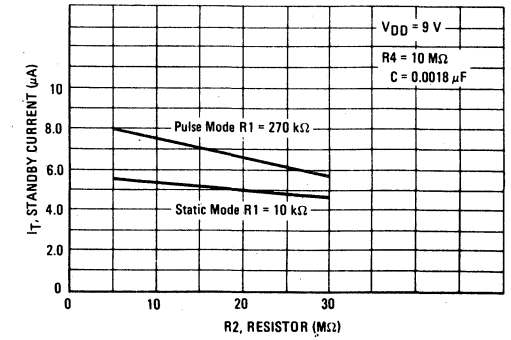


FIGURE 13 – TYPICAL STANDBY CURRENT versus SET RESISTOR, R2



APPLICATIONS INFORMATION

1. The MC14461 and MC14462 devices are designed to be relatively transient-free. However, the horn current loop—which includes the horn, emitter, and collector of the driver transistor, and the battery can place excessive transients that can affect the timing circuits and the input circuit which operate at high-impedance levels. Care must be taken in PC board layout with respect to ground and V_{DD}. For example, 3 or 4 inches of battery lead represents sufficient inductance to generate a substantial Ldi/dt transient. Usually a bypass capacitance, V_{DD} to ground of 0.001 μF, will isolate this transient to bypass the IC. A test for transient interference is to place a bypass capacitance across V_{DD} to ground near the IC and determine if the timing or smoke detection is altered.

2. To protect the IC during static discharge tests, it is recommended that the IC be shielded. Since the regulator drives the chamber, and if the chamber anode cannot be shielded, a 100 k resistor in series with the chamber-to-regulator pin is recommended. If static voltage reaches the detector pin on the MC14462 through the chamber in the particular chamber design (when the chamber anode is exposed to high static voltage), external capacitance added to this pin may solve the problem by absorbing the energy. The passing of static discharge tests in UL 217 requirements is dependent upon the design of the overall smoke detector structure. Many alternate methods of design are available to the designer which are beyond the scope of this data sheet.

3. The common annunciator may be connected via a two-wire system. The signal is a 50% ON/50% OFF duty cycle. To detect the particular detector sensing smoke via an LED at the detector, the signal may be taken from the comparator out and amplified to the LED. For systems that are powered from a common source rather than local battery, the timing of each detector can be set differently. This timing affects the period of the square wave pulse on the common annunciator line and that difference in the period can be used to detect which detector senses smoke at a master station.

Circuit diagrams external to or containing Motorola products are included as a means of illustration only. Complete information sufficient for construction purposes may not be fully illustrated. Although the information herein has been carefully checked and is believed to be reliable, Motorola assumes no responsibility for inaccuracies. Information herein does not convey to the purchaser any license under the patent rights of Motorola or others.

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MOTOROLA

MC14464
MC14465

Advance Information

CMOS MSI

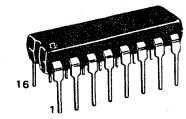
(LOW-POWER COMPLEMENTARY MOS)

SMOKE DETECTOR CIRCUITS FOR PHOTOELECTRIC CHAMBERS

SMOKE DETECTOR CIRCUITS

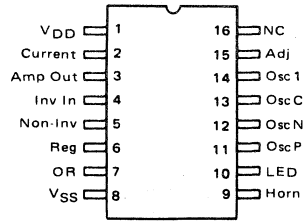
The MC14464 and MC14465 use linear CMOS technology to implement a smoke detector that senses reflected light from minute smoke particles. An LED provides a pulsed light source while a wide area silicon diode acts as a detector. The received pulse is amplified and compared to an externally set threshold to determine whether smoke or no smoke is present. The MC14464 is designed to drive an external NPN transistor connected to a mechanical horn while the MC14465 has an open drain N-Channel and modulated output useful in controlling a piezoelectric horn driver circuit. Features include:

- Meets UL 217 Specifications
- Adjustable Low Battery Trip Point
- Adjustable Smoke Threshold
- On-Chip Voltage Regulator
- Adjustable Smoke Sample Rate
- Sample Rate Increases 8 to 1 When Smoke is Detected
- Multi-Station Wired-OR Capability
- Battery Level Sampled Under Load
- Built-In Reverse Battery Protection
- Low Quiescent Current 7.0 μA at 9.0 V Typical
- Adjustable LED Pulse Width

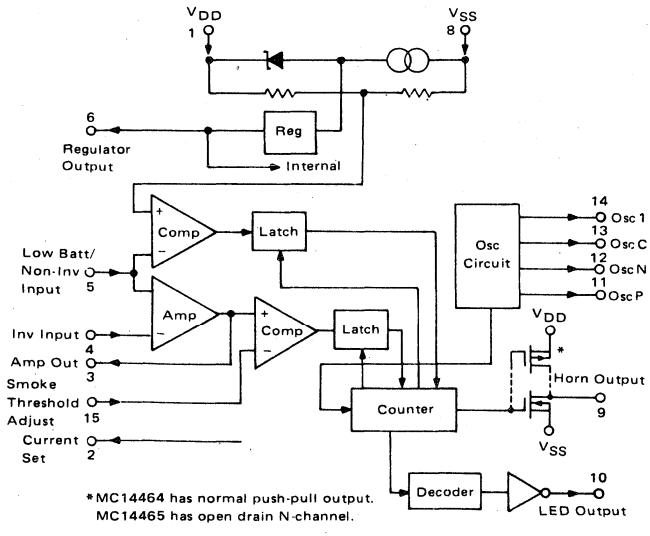


P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



*MC14464 has normal push-pull output.
MC14465 has open drain N-channel.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	0 to +15	Vdc
Voltage at Any Pin Except 11, 12, 14 Voltage at Pin 11 Voltage at Pin 12 Voltage at Pin 14	V_{in}	−0.3 to V_{DD} + 0.3 −0.6 to V_{DD} + 15 −15 to V_{DD} + 0.3 −4.0 to V_{DD} + 4.0	Vdc
Horn Drive Current, Pin 9	I_{out}	−30	mA
LED Drive Current, Pin 10	I_{out}	15	
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_A	0 to +50	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C
Reverse Battery Voltage	V_{RB}	−10 V for 4 s	—

RECOMMENDED OPERATING CONDITIONS

Oscillator Frequency	50 Hz
Oscillator/LED Pulse Width	200 μs
Supply Voltage	7 to 10 V
RESULTING TIME	
No-Smoke Sample Rate	10 s
Smoke Sample Rate	1.28 s
Low Battery Beep Pulse Width	20 ms
Low Battery Period	40 s

TIMING RELATIONSHIPS

Characteristic	Formula
LED Pulse Width	1.1 $R_N C$
Osc Frequency	$f = 1.1/C (R_P + R_N)$
Low Battery Alarm Pulse Width	1/f
LED No-Smoke Sample Rate	512/f
LED Smoke Sample Rate	64/f
Low Battery Alarm Period	2048/f
Smoke Alarm Horn-On*	120/f
Smoke Alarm Horn-Off*	8/f

*MC14464 only

ELECTRICAL CHARACTERISTICS (T_A = 25°C, R_{bias} = 10 MΩ, $V_{DD} - V_{SS}$ = 9.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Standby Current	I_{DD}	—	—	—	μA
Output Drive Current Horn (V_{out} = 0.7 V) LED ($V_{out} - V_S$ = 0.5 V)	 I_{OH} I_{OL}	 — —	 — —	 — —	mA
Regulated Voltage	V_S	**Values have not been determined at this time. For further information, contact Motorola CMOS Marketing.**			Vdc
Smoke Amplifier Open Loop Gain DC Open Loop Gain 1.0 kHz Offset Voltage Slew Rate	 A_{VOL} A_{VOL} V_{OS} SR				 dB dB mV V/μs
Input Current Pins 4, 5, 15	I_{in}				μA
Low Battery Level	V_{LB}	—	—	—	

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

CIRCUIT DESCRIPTION

Voltage Regulator

Pin 6 is regulated voltage with respect to V_{DD} at a voltage of typically V_{DD} - 4.0 V. It consists of an internal zener diode with a buffer amplifier capable of approximately 7.0 mA. The temperature coefficient is approximately +0.6 mV/°C.

Low Battery Voltage Warning

The low battery comparator is strobed for one clock period out of every 2048 clock periods (i.e., 20 ms out of 40 seconds). During this time the battery is loaded by the LED pulse and a comparison is made between 2/3 of the battery level and the voltage at pin 5. This signal is stored in a latch until the appropriate time at which the horn output is activated for one clock cycle.

For checking and adjusting the low battery voltage trip point, the oscillator frequency cannot simply be speeded up. This would not only shorten the 40-second beep period as desired, but would also shorten the 20 ms strobe period. A proposed speed-up circuit in Figure 1 can be used. This circuit provides 2048 pulses in 20 ms and then allows 20 ms to maintain the proper strobe interval. Thus the low battery period becomes 40 ms, but strobe timing is unaffected.

Smoke Alarm Circuit

The signal source for smoke detection is a photodiode that converts received light into electric current. This diode should be connected into pin 4 and amplified via the internal operational amplifier. The threshold for smoke detection is controlled via the voltage to pin 15. Since the smoke is detected as a reflected short burst of light, the detector/amplifier combination has to be considered as an ac signal. The diode has approximately 200 pF self-capacitance and the amplifier has a fixed slew rate, both of which limit the minimum LED pulse width for normal operation. The bias current of the smoke amplifier and the following comparator is increased one oscillator period before the LED-pulse starts. This increase in bias current causes a change of input offset voltage which in turn generates an output signal. The RC time constant of the feedback network around the op amp should be shorter than one oscillator period so that the amplifier output is not distrubed by the increase of bias current at the trailing edge of the LED pulse.

Temperature Compensation

Usually the photodiode detector exhibits a −2%/°C temperature coefficient which reduces sensitivity to smoke at elevated temperature. The usual correction for this is the addition of a negative temperature coefficient resistor controlling LED current. Then, as temperature increases, LED current will increase while sensitivity remains approximately constant. Temperature compensation can also be accomplished by increasing the LED pulse width as temperature increases. The internal oscillator circuit contributes to this with a 0.1%/°C positive temperature coefficient that increases the output pulse width at elevated temperatures. However, a temperature variable resistor should be substituted for R_N (pin 12) for full compensation using this method.

APPLICATIONS

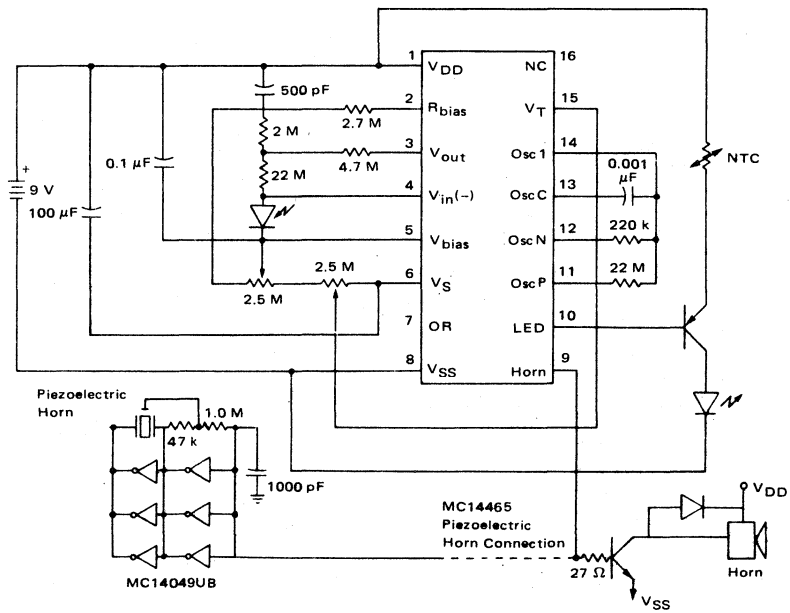
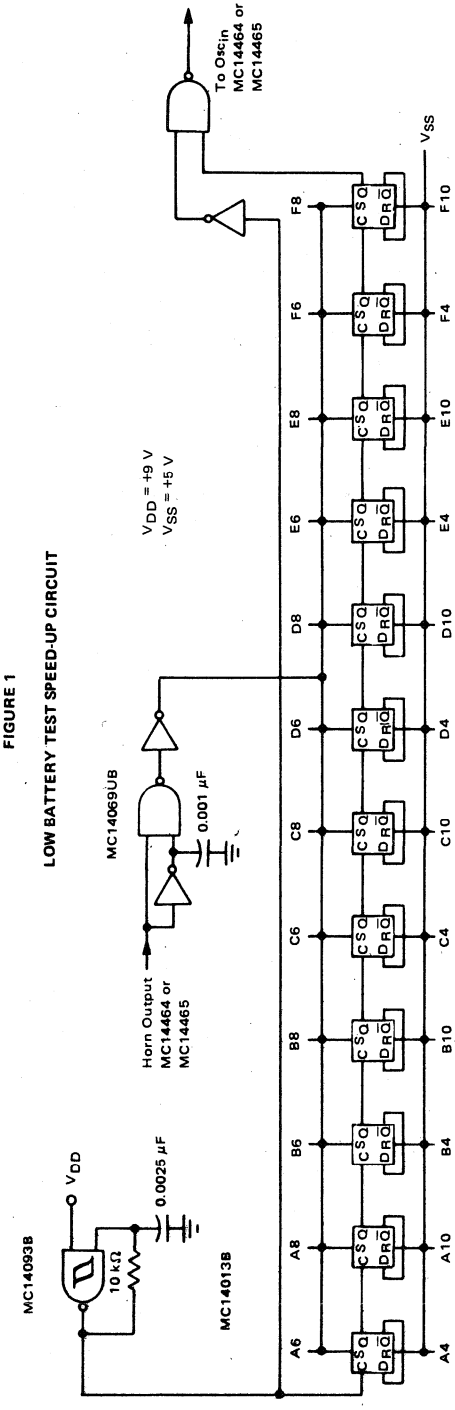
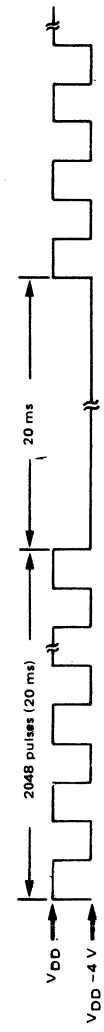


FIGURE 1

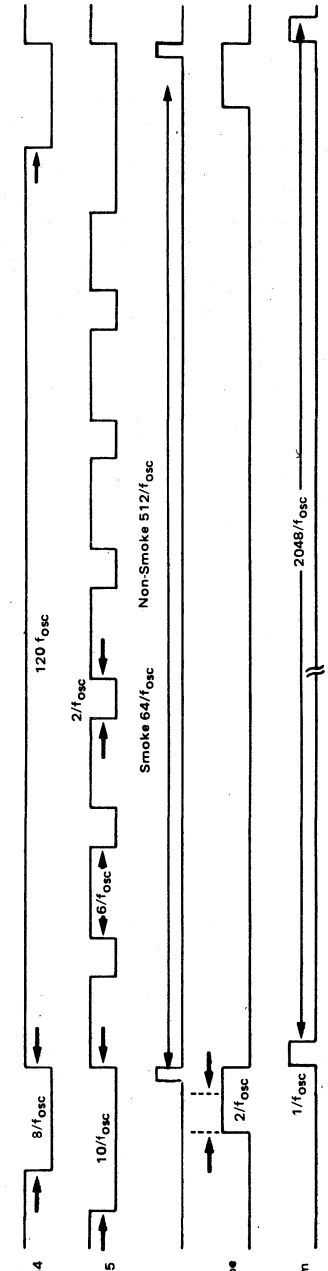
LOW BATTERY TEST SPEED-UP CIRCUIT



TIMING DIAGRAM FOR LOW BATTERY TEST SPEED-UP CIRCUIT



TIMING DIAGRAM



MOTOROLA

MC14469

ADDRESSABLE ASYNCHRONOUS RECEIVER/TRANSMITTER

The MC14469 Addressable Asynchronous Receiver Transmitter is constructed with MOS P-channel and N-channel enhancement devices in a single monolithic structure (CMOS). The MC14469 receives one or two eleven-bit words in a serial data stream. The first incoming word contains the address and when the address matches, the MC14469 is enabled to transmit two data words. Each of the transmitted words contains eight data bits, even parity bit, start and stop bit, in UART compatible format.

The received word contains seven address bits and the address of the MC14469 is set on seven pins. Thus 2^7 or 128 units can be interconnected in simplex or full duplex data transmission. In addition to the address received, seven command bits may optionally be received for data or control use.

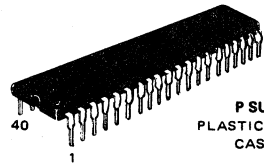
The MC14469 finds application in transmitting data from remote A-to-D converters, remote MPUs or remote digital transducers to a master computer or MPU.

- Supply Voltage Range — 4.5 Vdc to 18 Vdc
- Low Quiescent Current — 75 μAdc maximum @ 5 Vdc
- Data Rates to 4800 Baud
- Receive — Serial to Parallel
  Transmit — Parallel to Serial
- Transmit and Receive Simultaneously in Full Duplex
- Crystal or Resonator Operation for On-Chip Oscillator

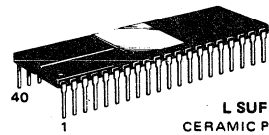
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

ADDRESSABLE ASYNCHRONOUS RECEIVER/TRANSMITTER



P SUFFIX
PLASTIC PACKAGE
CASE 711

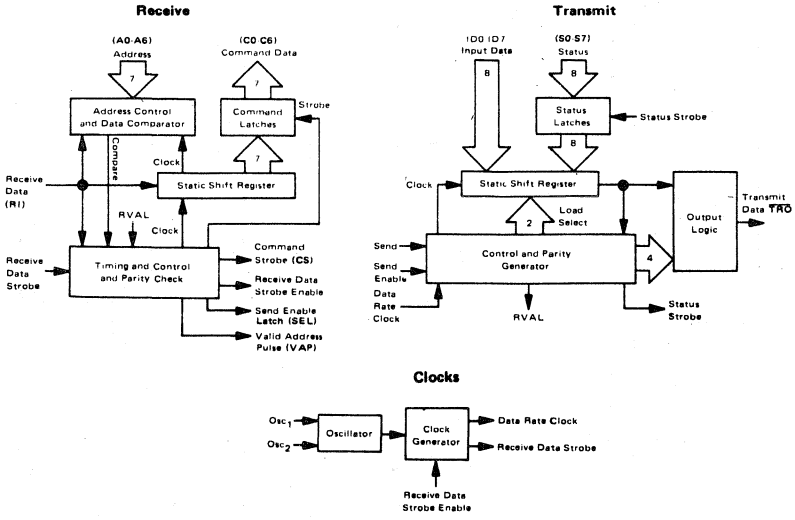


L SUFFIX
CERAMIC PACKAGE
CASE 715

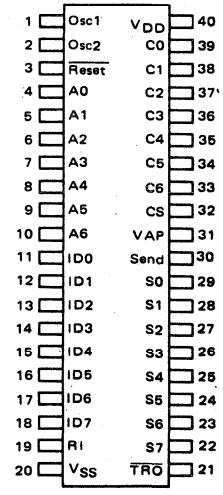
ORDERING INFORMATION

MC14xxx	Suffix	Denotes
	L	Ceramic Package
	P	Plastic Package

BLOCK DIAGRAMS



PIN ASSIGNMENTS



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 20.

	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

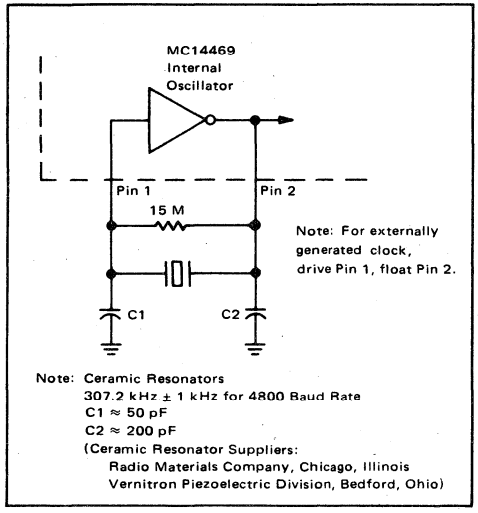
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95		14.95	15	–	14.95	–	
Input Voltage # "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (Except Pin 2)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.35	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Output Drive Current (Pin 2 Only)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.19	–	-0.16	-0.32	–	-0.13	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.04	–	-0.035	-0.07	–	-0.03	–	
(V_{OH} = 9.5 Vdc)		10	-0.09	–	-0.08	-0.16	–	-0.06	–	
(V_{OH} = 13.5 Vdc)		15	-0.29	–	-0.27	-0.48	–	-0.2	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.1	–	0.085	0.17	–	0.07	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.17	–	0.14	0.28	–	0.1	–	
(V_{OL} = 1.5 Vdc)		15	0.50	–	0.42	0.84	–	0.3	–	
Maximum Frequency	f_{max}	4.5	400	–	365	550	–	310	–	kHz
Input Current	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Pull-Up Current (Pins 4-18)	I_{UP}	15	12	120	10	50	100	8.0	85	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	75	–	0.010	75	–	565	μAdc
		10	–	150	–	0.020	150	–	1125	
		15	–	300	–	0.030	300	–	2250	
Supply Voltage	V_{DD}	–	+4.5	+18.0	+4.5	–	+18.0	+4.5	+18.0	Vdc

Noise immunity specified for worst-case input combination.
Noise Margin both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

FIGURE 1 – OSCILLATOR CIRCUIT



Note: Ceramic Resonators
307.2 kHz ± 1 kHz for 4800 Baud Rate
C1 ≈ 50 pF
C2 ≈ 200 pF
(Ceramic Resonator Suppliers:
Radio Materials Company, Chicago, Illinois
Vernitron Piezoelectric Division, Bedford, Ohio)

FIGURE 2 – RECTIFIED POWER FROM DATA LINES CIRCUIT

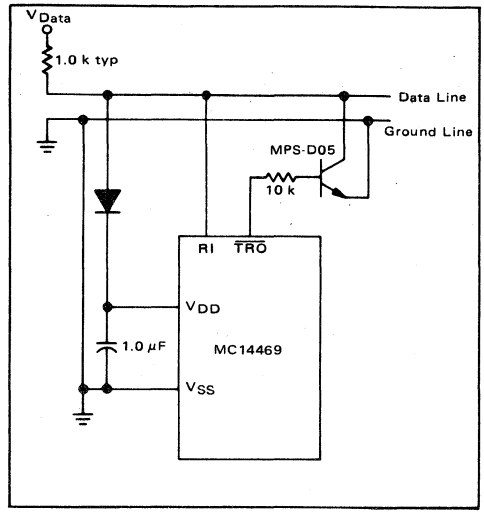
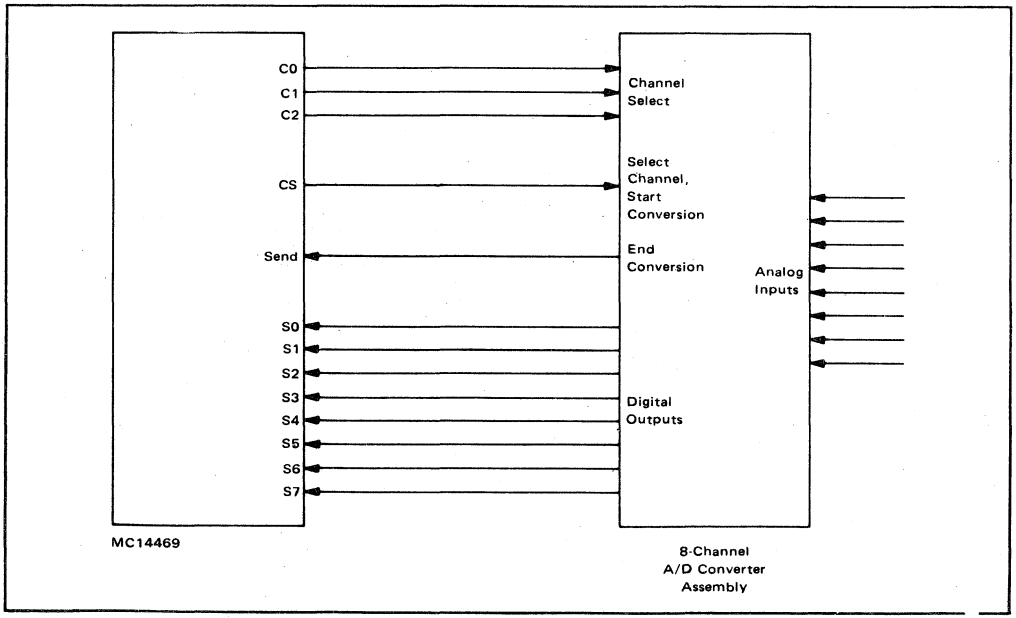


FIGURE 3 – A-D CONVERTER INTERFACE



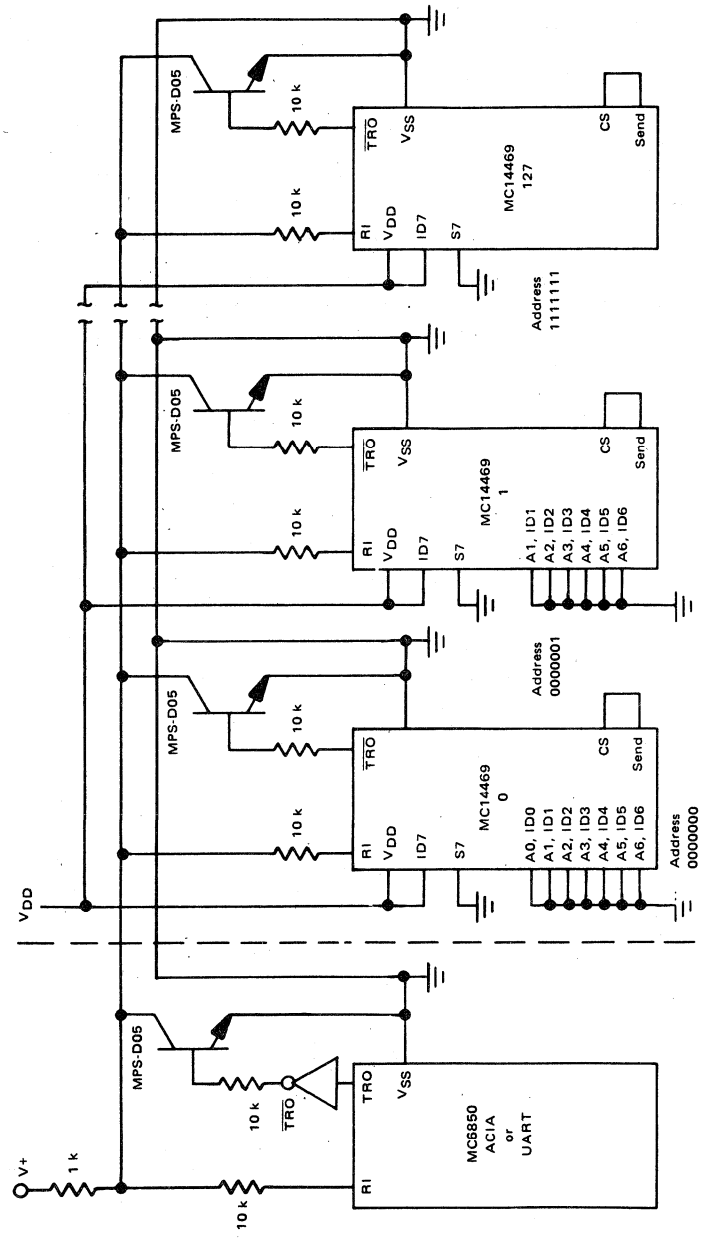
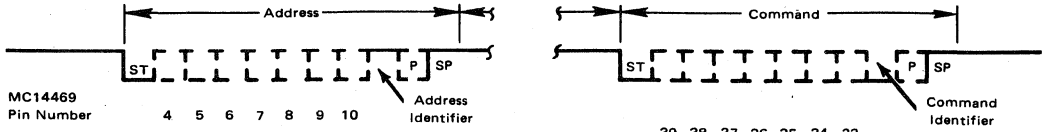


FIGURE 4 – SINGLE LINE, SIMPLEX DATA TRANSMISSION

Note: For Simplex operation the ID7 must be tied high, S7 must be tied low and the 7-bit ID must be the same as the 7-bit address (or set to some unused address) to prevent erroneous responses.

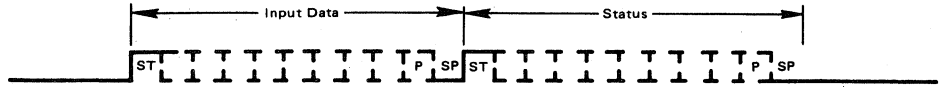
RECEIVE DATA (RI; Pin 19)



MC14469 Pin Number	4	5	6	7	8	9	10
Pin Designation	A0	A1	A2	A3	A4	A5	A6
MC6850 ACIA Pin Number	22	21	20	19	18	17	16
Pin Designation	D0	D1	D2	D3	D4	D5	D6

	39	38	37	36	35	34	33
	C0	C1	C2	C3	C4	C5	C6
	22	21	20	19	18	17	16
	D0	D1	D2	D3	D4	D5	D6

TRANSMIT DATA ($\overline{TRO}$; Pin 21)



MC14469 Pin Numbers	11	12	13	14	15	16	17	18	29	28	27	26	25	24	23	22
Pin Designation	ID0	ID1	ID2	ID3	ID4	ID5	ID6	ID7	S0	S1	S2	S3	S4	S5	S6	S7
MC6850 ACIA Pin Number	22	21	20	19	18	17	16	15	22	21	20	19	18	17	16	15
Pin Designation	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7

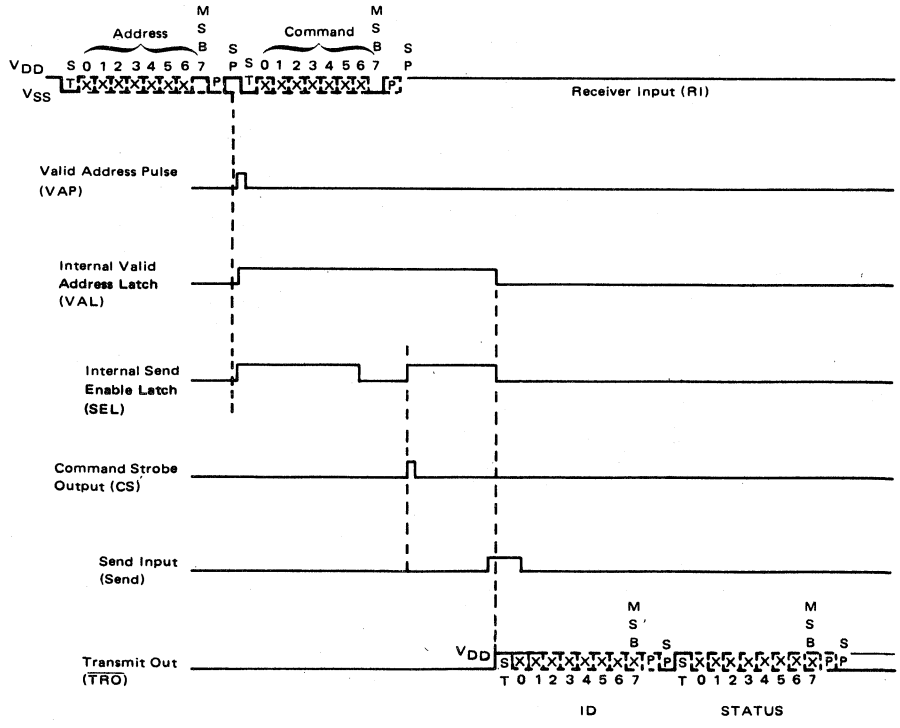
ST = Start Bit
P = Parity Bit
SP = Stop Bit

A0 → A6 = Address Bits
C0 → C6 = Command Bits
D0 → D7 = ACIA Bus Bits

ID0 → ID7 = MC14469 Identification Code
S0 → S7 = MC14469 Status Code

CORRESPONDING DATA POSITION AND PINS FOR MC14469 AND MC6850

TYPICAL RECEIVE/SEND CYCLE



DEVICE OPERATION

OSCILLATOR (Osc1, Osc2; Pins 1, 2) – These pins are the oscillator input and output. (See Figure 1.)

RESET ($\overline{\text{Reset}}$; Pin 3) – When this pin is pulled low, the circuit is reset and ready for operation.

ADDRESS (A0-A6; Pin 4, 5, 6, 7, 8, 9, 10) – These are the address setting pins which contain the address match for the received signal.

INPUT DATA (ID0-ID7; Pins 11, 12, 13, 14, 15, 16, 17, 18) – These pins contain the input data for the first eight bits of data to be transmitted.

RECEIVE INPUT (RI; Pin 19) – This is the receive input pin.

NEGATIVE POWER SUPPLY (V_{SS}; Pin 20) – This pin is the negative power supply connection. Normally this pin is system ground.

TRANSMIT REGISTER OUTPUT SIGNAL ($\overline{\text{TRO}}$; Pin 21) – This pin transmits the outgoing signal. Note that it is inverted from the incoming signal. It must go through one stage of inversion if it is to drive another MC14469.

SECOND or STATUS INPUT DATA (S0-S7; Pins 22, 23, 24, 25, 26, 27, 28, 29) – These pins contain the input data for the second eight bits of data to be transmitted.

SEND (Send; Pin 30) – This pin accepts the send command after receipt of an address.

VALID ADDRESS PULSE (VAP; Pin 31) – This is the output for the valid address pulse upon receipt of a matched incoming address.

COMMAND STROBE (CS; Pin 32) – This is the output for the command strobe signifying a valid set of command data on pins 33-39.

COMMAND WORD (C0-C6; Pins 33, 34, 35, 36, 37, 38, 39) – These pins are the readout of the command word which is the second word of the received signal.

POSITIVE POWER SUPPLY (V_{DD}; Pin 40) – This pin is the package positive power supply pin.

OPERATING CHARACTERISTICS

The receipt of a start bit on the Receive Input (RI) line causes the receive clock to start at a frequency equal to that of the oscillator divided by 64. All received data is strobed in at the center of a receive clock period. The start bit is followed by eight data bits. Seven of the bits are compared against states of the address of the particular circuit (A0-A6), while the eighth bit signifies an address word "1", or a command word "O". Next, a parity bit is received and checked by the internal logic for even parity. Finally a stop bit is received. At the completion of the cycle if the address compared, a Valid Address Pulse (VAP) occurs. Immediately following the address word, a command word is received. It also contains a start bit, eight data bits, even parity bit, and a stop bit. The eight data bits are composed of a seven-bit command, and a "0" which indicates a command word. At the end of the command word a Command Strobe Pulse (CS) occurs.

A negative transition on the Send input initiates the transmit sequence. Again the transmitted data is made up of two eleven-bit words. The data portion of the first word is made up from Input Data inputs (ID0-ID7), and the data for the second word from Second Input Data (S0-S7) inputs. This data is latched before the start of transmit of the first of the two words. The transmitted signal is the inversion of the standard UART TRO, which allows the use of an inverting amplifier to drive the lines.

The oscillator can be crystal controlled or ceramic resonator controlled for required accuracy. Pin 1 may be driven from an external clock source. See Figure 1.

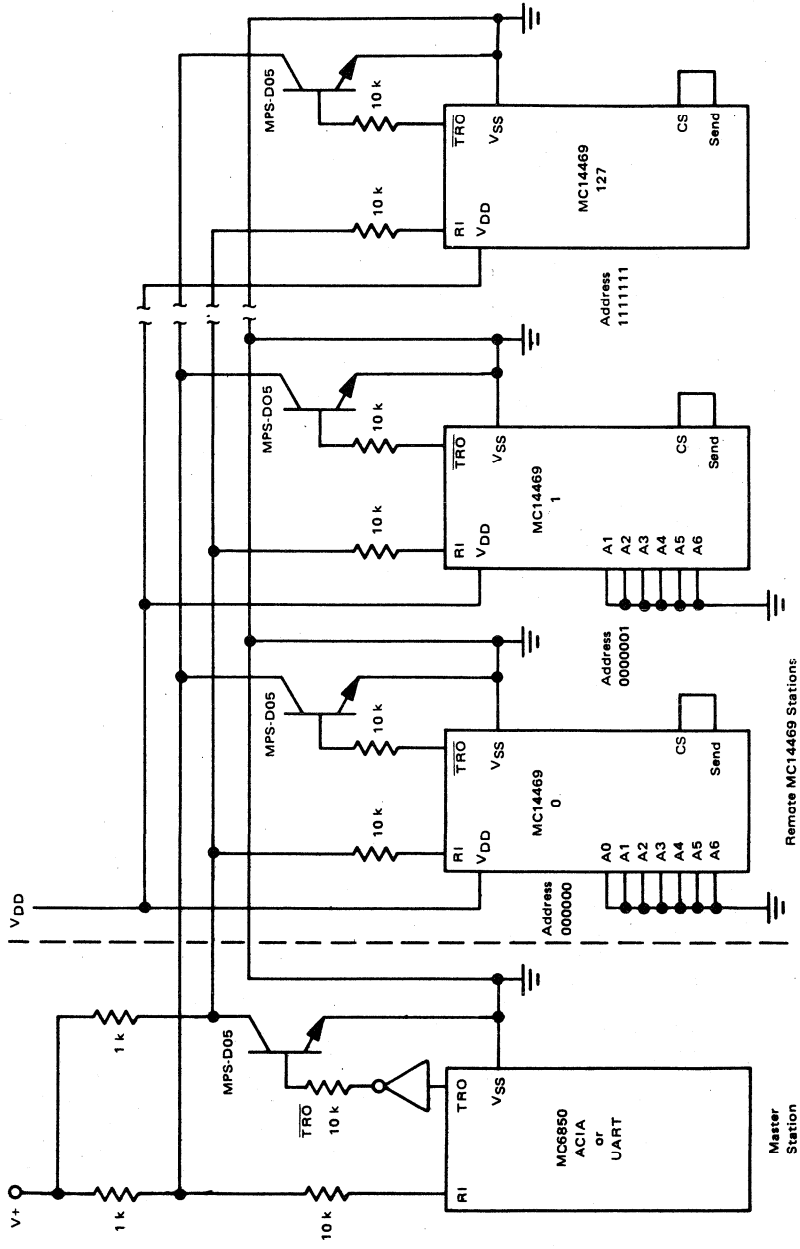
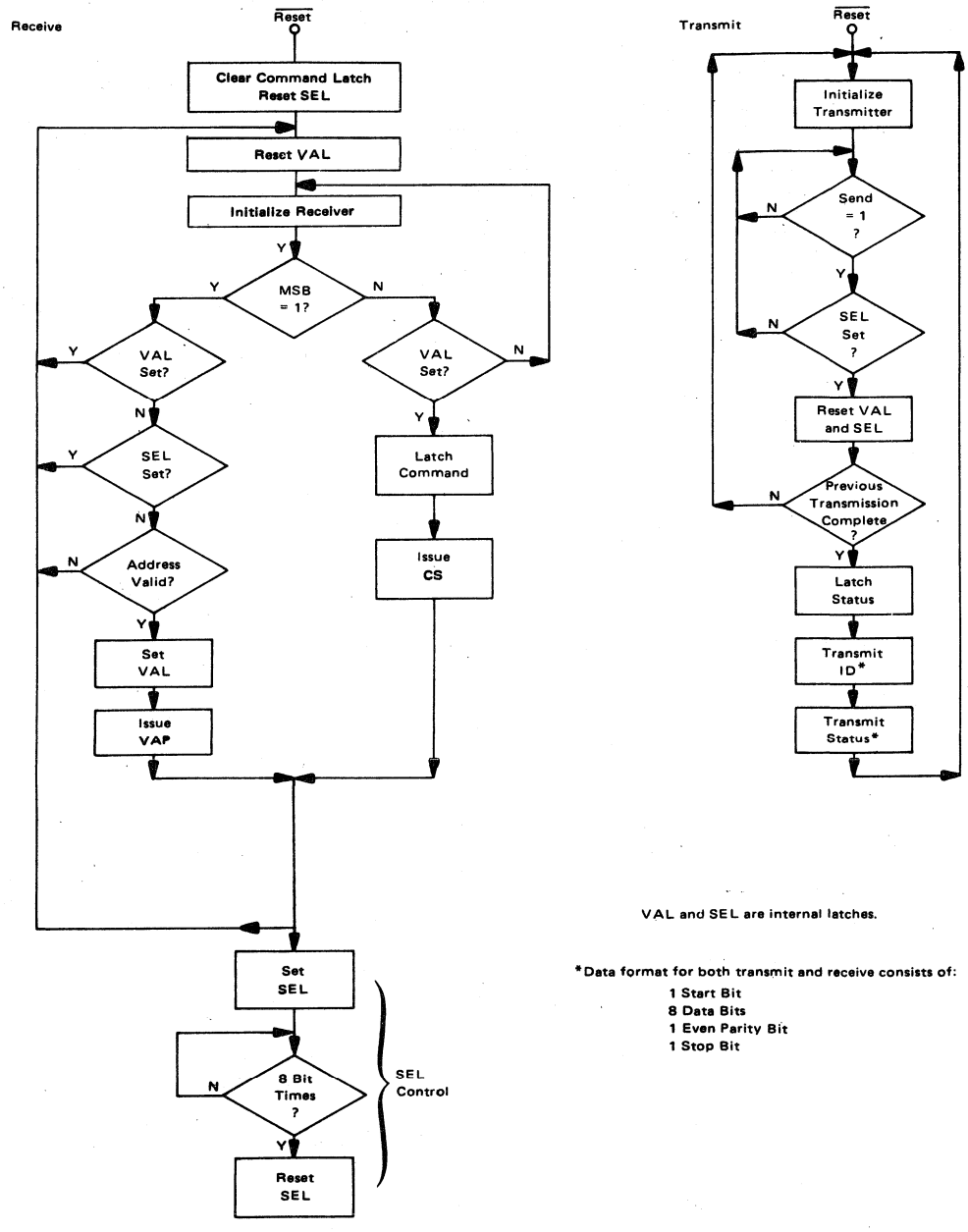


FIGURE 5 – DOUBLE LINE, FULL DUPLEX DATA TRANSMISSION

FIGURE 6 – FLOW CHART OF MC14469 OPERATION



VAL and SEL are internal latches.

*Data format for both transmit and receive consists of:

1 Start Bit
8 Data Bits
1 Even Parity Bit
1 Stop Bit

MOTOROLA

MC14490

HEX CONTACT BOUNCE ELIMINATOR

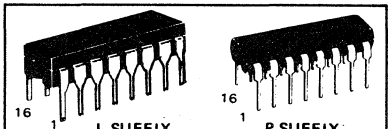
The MC14490 is constructed with complementary MOS enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the "make" and the "break" of a contact closure. The clock for operation of the MC14490 is derived from an internal R-C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another MC14490.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Six Debouncers per Package
- Internal Pullups on All Data Inputs
- Internal Oscillator (R-C), or External Clock Source
- TTL Compatible Data Inputs/Outputs
- Single Line Input, Debounces Both "Make" and "Break" Contacts
- Does Not Require "Form C" (Single Pole Double Throw) Input Signal
- Cascadable for Longer Time Delays
- Schmitt Trigger on Clock Input (Pin 7)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14490EFL/FL/FP)
  = 3.0 Vdc to 6.0 Vdc (MC14490EVL/VL/VP)

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

HEX CONTACT BOUNCE ELIMINATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

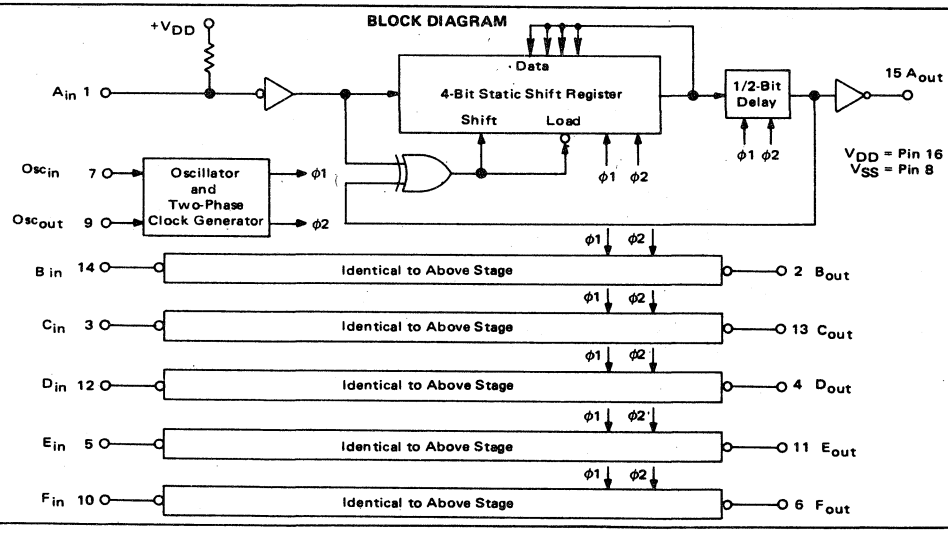
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14490

Suffix	Denotes
L	Ceramic Package
P	Plastic Package
F	Extended Operating Voltage Range (3V to 18V)
V	Limited Operating Voltage Range (3V to 6V)
Blank	Standard Operating Temperature Range (-40 to +85°C)
E	Extended Operating Temperature Range (-55 to +125°C)

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage – MC14490EFL/FL/FP – MC14490EVL/VL/VP	V_{DD}	 +18 to -0.5 +6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range MC14490EFL/EVL MC14490FL/FP/VL/VP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}** Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.02	–	0	0.02	–	0.10	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current ***	I_{OH}									mAdc
Source										
Oscillator Output										
(V_{OH} = 2.5 Vdc)		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
Debounce Outputs										
(V_{OH} = 2.5 Vdc)		5.0	-0.60	–	-0.50	-2.6	–	-0.4	–	
(V_{OH} = 9.5 Vdc)		10	-0.60	–	-0.50	-1.4	–	-0.4	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-5.4	–	-1.2	–	
Sink	I_{OL}									mAdc
Oscillator Output										
(V_{OL} = 0.4 Vdc)		5.0	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.4	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Debounce Outputs										
(V_{OL} = 0.4 Vdc)		5.0	2.4	–	2.2	4.0	–	1.8	–	
(V_{OL} = 0.5 Vdc)		10	4.0	–	3.3	10	–	2.7	–	
(V_{OL} = 1.5 Vdc)		15	12	–	10	40	–	8.1	–	
Input Leakage Currents Debounce Inputs ($V_{IH} = V_{DD}$)	I_{IH}	–	–	–	–	10	–	–	–	pAdc
Pullup Resistor Source Current Debounce Inputs ($V_{IL} = V_{SS}$)	I_{IL}	5.0	210	375	140	190	255	70	130	μAdc
		10	415	740	280	380	500	145	265	
		15	610	1100	415	570	750	215	400	
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Current Pin 7 = V_{SS}	I_{DD}	5.0	–	100	–	40	120	–	150	μAdc
		10	–	180	–	75	225	–	280	
		15	–	550	–	225	675	–	840	

*T_{low} = -55°C for MC14490EFL, EVL; -40°C for MC14490FL, FP, VL, VP.
T_{high} = +125°C for MC14490EFL, EVL; +85°C for MC14490FL, FP, VL, VP.
**Only 5-volt specifications apply to MC14490EVL, VL, VP devices.
***Care must be taken not to exceed maximum current ratings (See Maximum Ratings Table and Figure 2).

SWITCHING CHARACTERISTICS (C_L = 15 pF)

Characteristic	Symbol	V_{DD}** Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Rise Time	t_{TLH}									ns
All Outputs		5.0	–	–	–	70	–	–	–	
		10	–	–	–	35	–	–	–	
		15	–	–	–	25	–	–	–	
Output Fall Time	t_{THL}									ns
Oscillator Output		5.0	–	–	–	70	–	–	–	
		10	–	–	–	35	–	–	–	
		15	–	–	–	25	–	–	–	
Debounce Outputs		5.0	–	–	–	50	–	–	–	ns
		10	–	–	–	25	–	–	–	
		15	–	–	–	18	–	–	–	
Propagation Delay Time	t_{PHL}									ns
Oscillator Input to		5.0	–	–	–	625	–	–	–	
Debounce Outputs		10	–	–	–	250	–	–	–	
		15	–	–	–	200	–	–	–	
	t_{PLH}	5.0	–	–	–	700	–	–	–	ns
		10	–	–	–	275	–	–	–	
		15	–	–	–	200	–	–	–	
Maximum Clock Frequency	f_{cl}									MHz
(50% Duty Cycle)		5.0	–	–	–	0.4	–	–	–	
		10	–	–	–	1.0	–	–	–	
		15	–	–	–	1.3	–	–	–	
Minimum Setup Time	t_{su}	5.0	–	–	–	200	–	–	–	ns
(See Figure 1)		10	–	–	–	40	–	–	–	
		15	–	–	–	30	–	–	–	
Maximum External Clock Input	t_{TLH},									ns
Rise and Fall Time	t_{THL}	5.0	No Limit							
Oscillator Input		10								
		15								
Typical Oscillator Frequency	f_{osc}	–	$f = \frac{0.375\ V_{DD}}{C_{ext}}$ (V_{DD} in Vdc, C_{ext} in pF)							MHz

*T_{low} = -55°C for MC14490 EFL, EVL; -40°C for MC14490FL, FP, VL, VP.
T_{high} = +125°C for MC14490 EFL, EVL; +85°C for MC14490FL, FP, VL, VP
**Only 5-volt specifications apply to MC14490 EVL, VL, VP devices.

FIGURE 1 – TYPICAL SWITCHING TIME WAVEFORMS

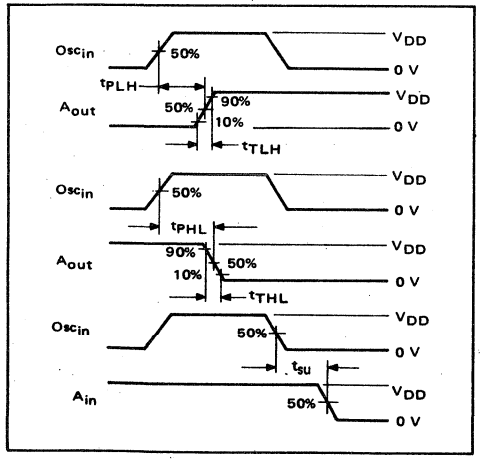
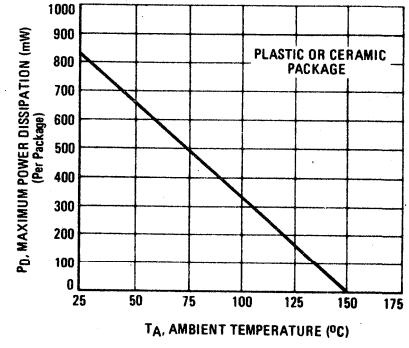


FIGURE 2 – AMBIENT TEMPERATURE POWER DERATING



THEORY OF OPERATION

The MC14490 Hex Contact Bounce Eliminator is basically a digital integrator. The circuit can integrate both up and down. This enables the circuit to eliminate bounce on both the leading and trailing edges of the signal, shown in the timing diagram of Figure 3.

Each of the six Bounce Eliminators is composed of a 4½-bit register (the integrator) and logic to compare the input with the contents of the shift register, as shown in Figure 4. The shift register requires a series of timing pulses in order to shift the input signal into each shift register location. These timing pulses (the clock signal) are represented in the upper waveform of Figure 3. Each of the six Bounce Eliminator circuits has an internal resistor as shown in Figure 4. A pullup resistor was incorporated rather than a pulldown resistor in order to implement switched ground input signals, such as those coming from relay contacts and push buttons. By switching ground, rather than a power supply lead, system faults (such as shorts to ground on the signal input leads) will not cause excessive currents in the wiring and contacts. Signal lead shorts to ground are much more probable than shorts to a power supply lead.

When the relay contact is open the shift register is loaded with a 1 (positive logic assumed) on each positive edge of the clock signal. To understand the operation, we assume all bits of the shift register are loaded with 1's and the output is at a 1 or high level.

At clock edge 1 (Figure 3) the input has gone low and a 0 (low level) has been loaded into the first bit or storage location of the shift register. Just after the positive edge of clock 1 the input signal has bounced back to a logic 1. This causes the shift register to be reset to all 1's in all four bits — thus starting the timing sequence over again.

During clock edges 3 to 6 the input signal has stayed low. Thus a logic 0 has been shifted into all four shift register bits and, as shown, the output goes to a 0 during the positive edge of clock pulse 6.

It should be noted that there is a 3½ to 4½ clock period delay between the clean input signal and output signal. In this example there is a delay of 3.8 clock periods from the beginning of the clean input signal.

After some time period of N clock periods, the contact is opened and at N+7 a 1 is loaded into the first bit. Just after N+7, when the input bounces low, all bits are reset to 0. At N+8 nothing happens because the input and output are low and all bits of the shift register are 0. At time N+9 and thereafter the input signal is a high (1) clean signal. At N+13 the output goes high (1) as a result of four 1's being shifted into the shift register.

Assuming the input signal is long enough to be clocked through the Bounce Eliminator, the output signal will be no longer or shorter than the clean input signal plus or minus one clock period.

The amount of time distortion between the input and output signals is a function of the difference in bounce characteristics on the edges of the input signal and the clock frequency. Since most relay contacts have more bounce when making as compared to breaking, the overall delay, counting bounce period, will be greater on the leading edge of the input signal than on the trailing edge. Thus, the output signal will be shorter than the input signal — if you include the leading edge bounce in the overall timing calculation.

The only requirement on the clock frequency in order to obtain a bounce free output signal is that four clock periods do not occur while the input signal is in a false state. Referring to Figure 3, a false state is seen to occur three times at the beginning of the input signal. The input signal goes low three times before it finally settles down to a valid low state. The first three low pulses are referred to as false states.

If the user has an available clock signal of the proper frequency, it may be used by connecting it to the oscillator input (pin 7). However, if an external clock is not available the user can place a small capacitor across the oscillator input and output pins in order to start up an internal clock source (as shown in Figure 4). The clock signal at the oscillator output pin may then be used to clock other MC14490 Bounce Eliminator packages. With the use of the MC14490, a large number of signals can be cleaned up, with the requirement of only one small capacitor external to the Hex Bounce Eliminator packages.

FIGURE 3 – TIMING DIAGRAM

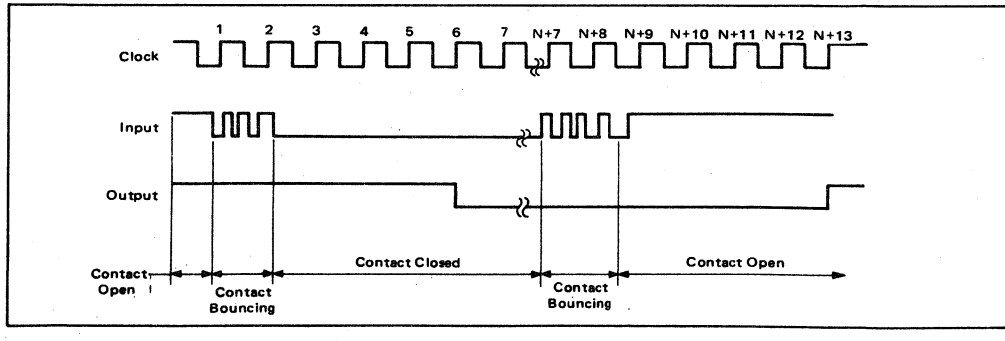
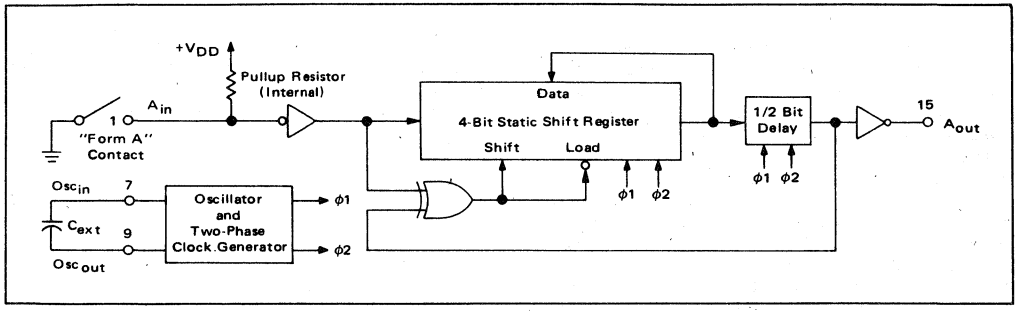


FIGURE 4 – TYPICAL "FORM A" CONTACT DEBOUNCE CIRCUIT
(Only One Debouncer Shown)



OPERATING CHARACTERISTICS

The single most important characteristic of the MC14490 is that it works with a single signal lead as an input, making it directly compatible with mechanical contacts (Form A and B).

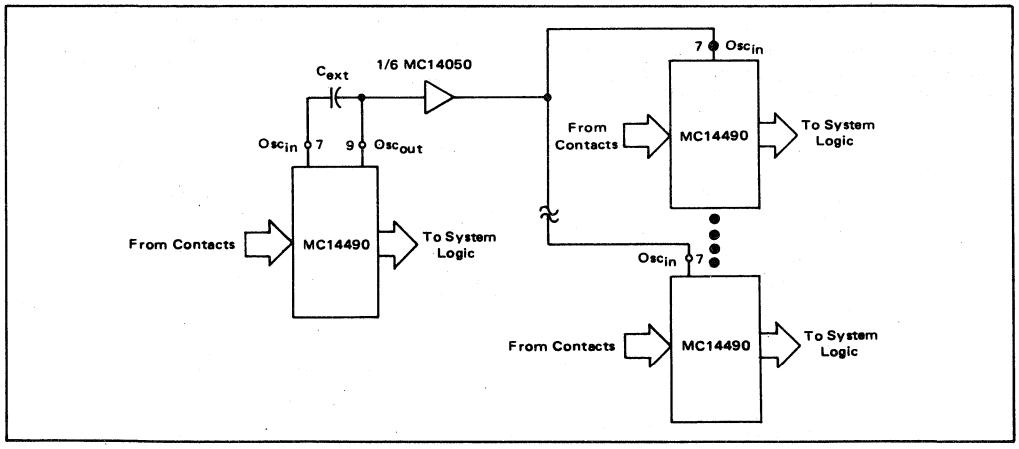
The circuit has a built in pullup resistor on each input. The worst case value of the pullup resistor (determined from the Electrical Characteristics table) is used to calculate the contact wetting current. If more contact current is required, an external resistor may be connected between V_{DD} and the input.

Because of the built in pullup resistors, the inputs cannot be driven with a single standard CMOS gate when V_{DD} is below 5 V. At this voltage, the input should be driven with paralleled standard gates or by the MC14049 or MC14050 buffers.

The clock input circuit (pin 7) has Schmitt trigger shaping such that proper clocking will occur even with very slow clock edges, eliminating any need for clock preshaping. In addition, other MC14490 oscillator inputs can be driven from a single oscillator output buffered by an MC14050 (see Figure 5).

The MC14490 is TTL compatible on both the inputs and the outputs. When V_{DD} is at 4.5 V, the buffered outputs can sink 1.6 mA at 0.4 V. The inputs can be driven with TTL as a result of the internal input pullup resistors.

FIGURE 5 – TYPICAL SINGLE OSCILLATOR DEBOUNCE SYSTEM

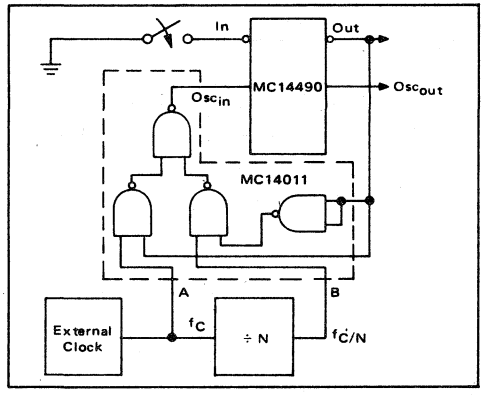


TYPICAL APPLICATIONS

ASYMMETRICAL TIMING

In applications where different leading and trailing edge delays are required (such as a fast attack/slow release timer.) Clocks of different frequencies can be gated into the MC14490 as shown in Figure 6. In order to produce a slow attack/fast release circuit leads A and B should be interchanged. The clock out lead can then be used to feed clock signals to the other MC14490 packages where the asymmetrical input/output timing is required.

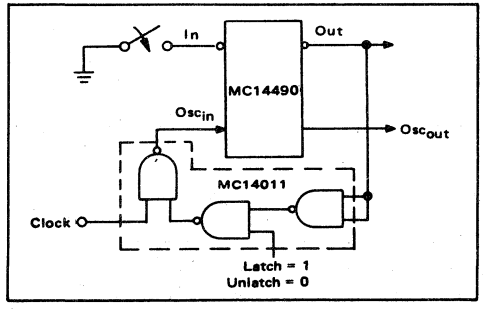
FIGURE 6 – FAST ATTACK/SLOW RELEASE CIRCUIT



LATCHED OUTPUT

The contents of the Bounce Eliminator can be latched by using several extra gates as shown in Figure 7. If the latch lead is high the clock will be stopped when the output goes low. This will hold the output low even though the input has returned to the high state. Any time the clock is stopped the outputs will be representative of the input signal four clock periods earlier.

FIGURE 7 – LATCHED OUTPUT CIRCUIT



MULTIPLE TIMING SIGNALS

As shown in Figure 8, the Bounce Eliminator circuits can be connected in series. In this configuration each output is delayed by four clock periods relative to its respective input. This configuration may be used to generate multiple timing signals such as a delay line, for programming other timing operations.

One application of the above is shown in Figure 9, where it is required to have a single pulse output for a single operation (make) of the push button or relay contact. This only requires the series connection of two Bounce Eliminator circuits, one inverter, and one NOR gate in order to generate the signal $A\overline{B}$ as shown in Figures 9 and 10. The signal $A\overline{B}$ is four clock periods in length. If the inputs to the NOR gate are interchanged the pulse $\overline{A}B$ will be generated upon release or break of the contact. With the use of a few additional parts many different pulses and waveshapes may be generated.

FIGURE 8 – MULTIPLE TIMING CIRCUIT CONNECTIONS

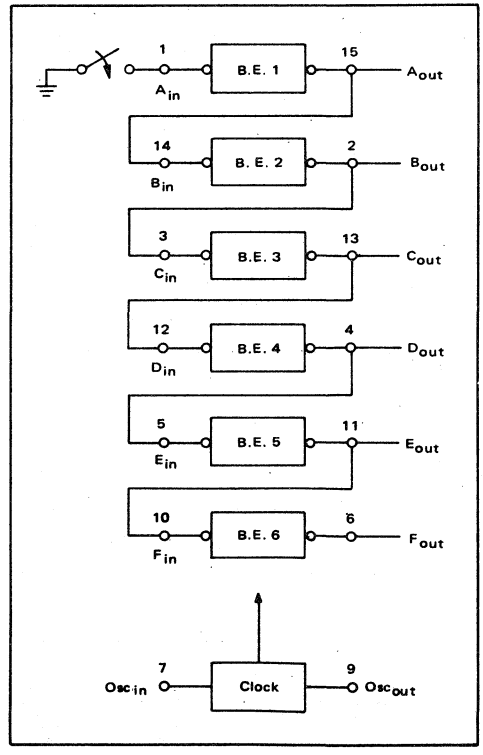


FIGURE 9 – SINGLE PULSE OUTPUT CIRCUIT

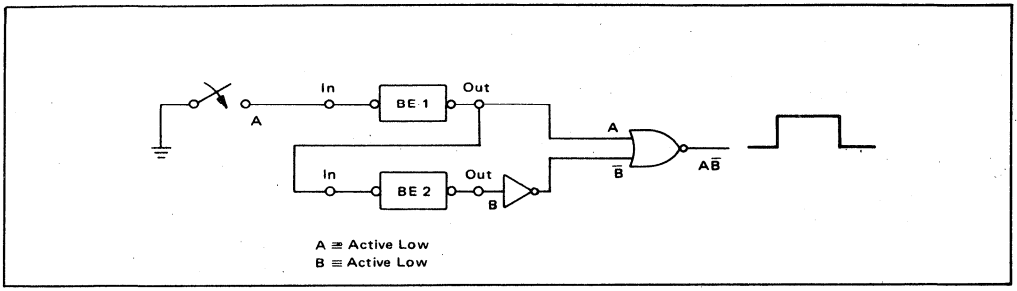
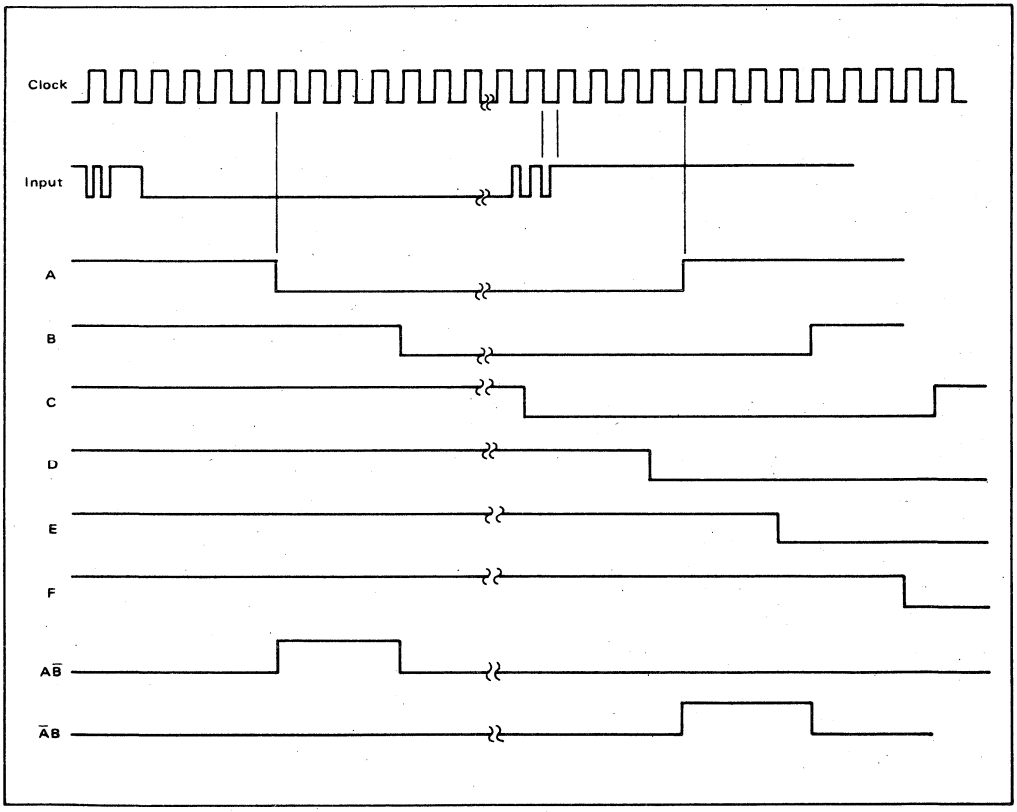


FIGURE 10 – MULTIPLE OUTPUT SIGNAL TIMING DIAGRAM



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14491

MULTI-FUNCTION DEBOUNCE CIRCUIT

The MC14491 AL/CL is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure.

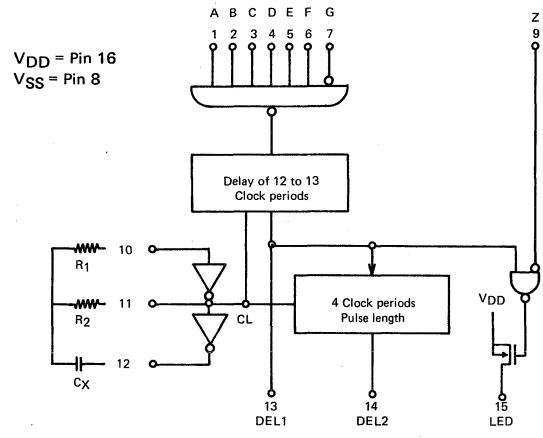
The structure provides two different delayed output signals depending on the logical input conditions. The delay-time (12 or 4 durations of the internally generated clock periods), can be adjusted within a wide range. The delay is controlled by 3 external passive components (2 resistors and 1 capacitor). The device has been specifically designed for alarm detection in electrical power plant equipment. However it can also be used for industrial debounce applications.

- Wide range of delay 12 μs to 12 s
- Two different delays
- Externally adjustable delays
- Noise pulses at the logical inputs will not disturb the function
- Output can be used to drive LED displays

MAXIMUM RATINGS (Voltage referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14491	V_{DD}	+18 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I_{DD}	10	mAdc
Operating Temperature Range — MC14491	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM

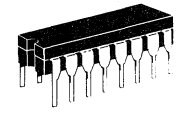


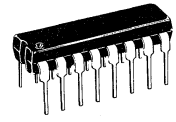
CMOS

(LOW-POWER COMPLEMENTARY MOS)

MULTI-FUNCTION DEBOUNCE CIRCUIT

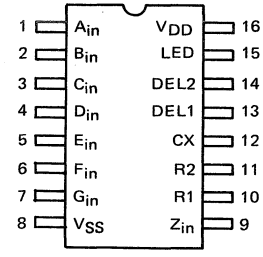
L Suffix
Ceramic Package
Case 620





P Suffix
Plastic Package
Case 648

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} or V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either, V_{SS} or V_{DD}).

For further details of this circuit please contact your local Sales Office.

MOTOROLA

MC14492

2 x 2 x 2 CROSSPOINT SWITCH

The MC14492 consists of a pair of 2 x 2 matrices of bilateral CMOS switches, controlled by a common selection matrix.
The device is intended for switching analog signals in communications systems. The use of a low voltage threshold processing in combination with a five element transmission gate provides an excellent linearity of the RON transfer characteristic.
The selection array consists of a 2 x 2 matrice decoding network which addresses the latch associated with the selected pair of switches. The SWITCH CONTROL input allows for storing the logical information in the latches to close or open the selected switch. The MASTER RESET when high forces all the switches to the open state provided that address inputs are at the low level.

- Diode protection on all inputs
- Noise immunity = 45% V_{DD}
- Supply voltage range = 3 Vdc to 18 Vdc
- High ON-OFF voltage ratio (feed through) — 105 dB typical @ RL = 3 KΩ, F = 3.4 kHz
- Low crosstalk between adjacent switches — 110 dB typical @ RL = 3 KΩ, F = 3.4 kHz
- Low RON, 40 Ω typical @ V_{DD}-V_{SS} = 15 Vdc
- Linearized transfer characteristics, ΔRON < 5Ω @ V_{in} = (V_{DD} −4 Vdc) to (V_{SS} +4 Vdc) V_{DD} = 15 Vdc.

FIGURE 1 — SWITCH CIRCUIT SCHEMATIC

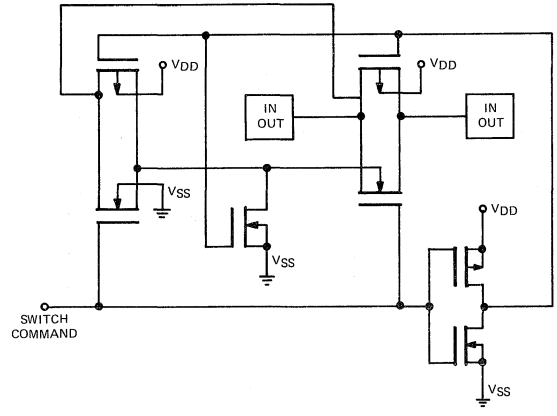
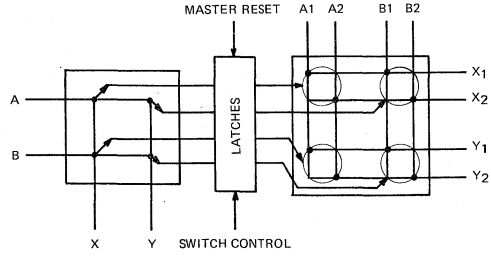


FIGURE 2 — BLOCK DIAGRAM

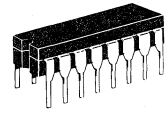


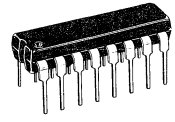
CMOS

(LOW-POWER COMPLEMENTARY MOS)

2 x 2 x 2 CROSSPOINT SWITCH

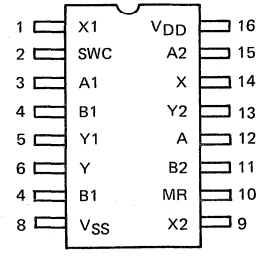
L Suffix
Ceramic Package
Case 620





P Suffix
Plastic Package
Case 648

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} and V_{out} are not constrained to the range V_{SS} (V_{in} or V_{out}) ≤ V_{DD}.
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied and the outputs are shored to V_{SS} and are at a peak sinewave voltage.

For further details of this circuit please contact your local Sales Office.

MOTOROLA

MC14493
MC14494

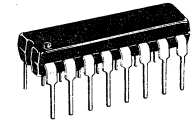
BINARY TO SEVEN SEGMENT LATCH/DECODER/DRIVER FOR 1½ DIGITS

The MC14493 and the MC14494 are 1½ digit 7 segment decoder and driver circuits designed for TV program number display or general purpose applications.

- The MC14493 provides binary plus one decoding
- The MC14494 provides binary decoding
- Designed to drive common cathode LED displays
- VCR output is activated whenever program 16 is displayed
- High current sourcing outputs with internal limiting resistance
- Internal input Level shift.

CMOS

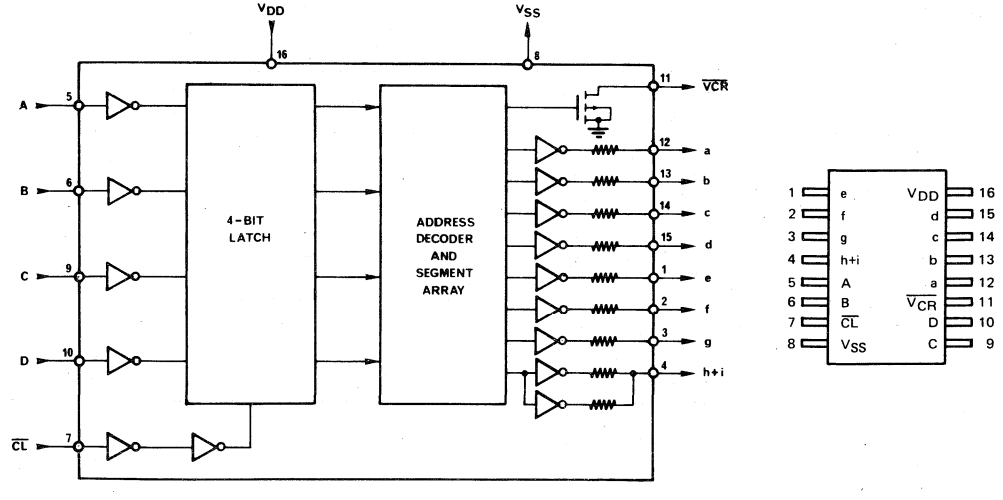
SEVEN SEGMENT DECODER/DRIVER



CASE 648
PLASTIC PACKAGE

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated, voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

FIGURE 1 – BLOCK DIAGRAM & PIN ASSIGNEMENT



MAXIMUM RATING (T_A = 25 °C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 V to +18	Vd_c
Input Voltage, all Inputs	V_{IN}	−0.5 V to V_{DD} + 0.5	Vd_c
DC Current Drain per Input	I	10	mA
Dissipation per Output Driver Pins 1, 2, 3, 12, 13, 14, 15 Pin 4	P_{OH}	 50 100	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (All voltages referenced to V_{SS} = 0, T_A = 0 to 70 °C)

Characteristics		Symbol	Min.	Max.	Unit
DC Supply Voltage		V_{DD}	4.5	16	V
Input Voltage		V_{IL}		0.8	V
	(V_{DD} = 15 V) (V_{DD} = 5 V)	V_{IH}	4 3.5		V
Input Current		I_{IN}		±1	μA
$\overline{VCR}$, Output, open drain	(V_{OH} = V_{DD})	I_{OH}		±1	μA
	(V_{OL} = 0.5 V, V_{DD} = 5 V) (V_{OL} = 0.5 V, V_{DD} = 15 V)	I_{OL}	0.2 1		mA
Outputs a,b,c,d,e,f,g	(V_{OH} = 2.0 V, V_{DD} = 5 V) (V_{OH} = 1.5 V, V_{DD} = 5 V) (V_{OH} = 12 V, V_{DD} = 15 V) (V_{OH} = 11.5 V, V_{DD} = 15 V)	I_{OH}	−7.5 −7.5 	 −11.5 −11.5	mA
	(V_{OL} = 1 V, V_{DD} = 5 V) (V_{OL} = 1 V, V_{DD} = 15 V)	I_{OL}	0.1 0.5		mA
Output h + i	(V_{OH} = 2 V, V_{DD} = 5 V) (V_{OH} = 1.5 V, V_{DD} = 15 V) (V_{OH} = 12 V, V_{DD} = 15 V) (V_{OH} = 11.5 V, V_{DD} = 15 V)	I_{OH}	−15 −15 	 −23 −23	mA
	(V_{OL} = 1 V, V_{DD} = 5 V) (V_{OL} = 1 V, V_{DD} = 15 V)	I_{OL}	0.2 1.0		mA

INPUT/OUTPUT FUNCTIONS

SEGMENT DRIVER (a, b, c, d, e, f, g, h, i; Pins 1, 2, 3, 4, 12, 13, 14, 15).

The segment drivers are emitter-follower NPN-transistors. To limit the output current, a resistor typically 290 ohms is integrated internally at each output. Therefore, external resistors are not necessary when driving an LED at the supply voltage of V_{DD} = 5.0 volts.

OUTPUT $\overline{VCR}$ (Pin 11)

This output is activated (goes to low) whenever the address corresponding to program 16 is selected. Otherwise the output is open. See the truth table.

INPUT LATCH (A, B, C, D; Pins 5, 6, 8, 10)

The block diagram is shown on page 1. The inputs A, B, C and D are fed to a 4-bit latch which is controlled by clock (CL). Two modes of operation are available.

CLOCK (CL; Pin 7)

The data on the inputs A, B, C aNd D will pass through the latch and will be displayed immediately when the clock is low. In this mode of operation the circuit is performing the function of a conventional decoder/driver. The data may be loaded into the latch when CL = low and will be latched with the rising edge of CL. The data will remain stored as long as CL is high.

TABLE 1 – TABLE OF INSTRUCTIONS

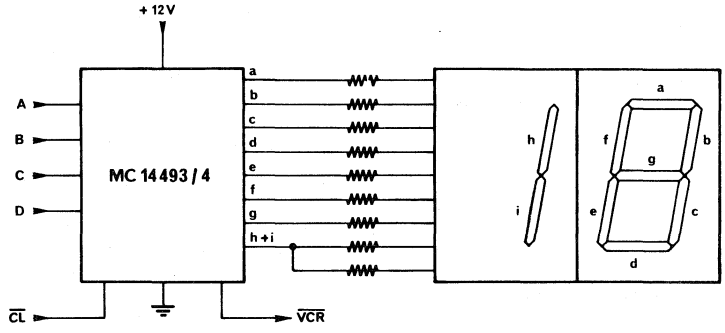
14493 TRUTH TABLE

A	B	C	D	a	b	c	d	e	f	g	h+i	VCR	Display
0	0	0	0	0	1	1	0	0	0	0	0	1	1
1	0	0	0	1	1	0	1	1	0	1	0	1	2
0	1	0	0	1	1	1	1	0	0	1	0	1	3
1	1	0	0	0	1	1	0	0	1	1	0	1	4
0	0	1	0	1	0	1	1	0	1	1	0	1	5
1	0	1	0	1	0	1	1	1	1	1	0	1	6
0	1	1	0	1	1	1	0	0	0	0	0	1	7
1	1	1	0	1	1	1	1	1	1	1	0	1	8
0	0	0	1	1	1	1	1	0	1	1	0	1	9
1	0	0	1	1	1	1	1	1	1	0	1	1	10
0	1	0	1	0	1	1	0	0	0	0	1	1	11
1	1	0	1	1	1	0	1	1	0	1	1	1	12
0	0	1	1	1	1	1	1	0	0	1	1	1	13
1	0	1	1	0	1	1	0	0	1	1	1	1	14
0	1	1	1	1	0	1	1	0	1	1	1	1	15
1	1	1	1	1	0	1	1	1	1	1	1	0	16

14494 TRUTH TABLE

A	B	C	D	a	b	c	d	e	f	g	h+i	VCR	Display
0	0	0	0	1	0	1	1	1	1	1	1	0	16
1	0	0	0	0	1	1	0	0	0	0	0	1	1
0	1	0	0	1	1	0	1	1	0	1	0	1	2
1	1	0	0	1	1	1	1	0	0	1	0	1	3
0	0	1	0	0	1	1	0	0	1	1	0	1	4
1	0	1	0	1	0	1	1	0	1	1	0	1	5
0	1	1	0	1	0	1	1	1	1	1	0	1	6
1	1	1	0	1	1	1	0	0	0	0	0	1	7
0	0	0	1	1	1	1	1	1	1	1	0	1	8
1	0	0	1	1	1	1	1	0	1	1	0	1	9
0	1	0	1	1	1	1	1	1	1	0	1	1	10
1	1	0	1	0	1	1	0	0	0	0	1	1	11
0	0	1	1	1	1	0	1	1	0	1	1	1	12
1	0	1	1	1	1	1	1	0	0	1	1	1	13
0	1	1	1	0	1	1	0	0	1	1	1	1	14
1	1	1	1	1	0	1	1	0	1	1	1	1	15

FIGURE 2 – TYPICAL CONFIGURATION



NOTE: Series resistors are necessary if V_{DD} is higher than 5 V.

Circuit diagrams utilizing Motorola products are incuded as a means of illustrating typical semiconductor applications, consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any licénse under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14495

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

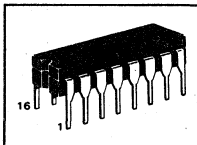
BCD-TO-SEVEN SEGMENT HEXADECIMAL LATCH/ DECODER/DRIVER

The MC14495 BCD-to-seven segment hexidecimal latch/decoder/ driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch. It can be used with LED seven segment displays without resistor interface at 5 volt supply. The resistors of typically 290 ohms are internal to the part.

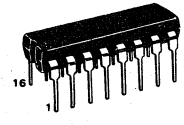
Applications include MPU systems display driver, instrument display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs With Internal Limiting Resistance
- Latch Storage of Code
- Supply Voltage Range = 4.5 Vdc to 16 Vdc
- Internal Input Level Shift:
  Input +5 CMOS to V_{DD} of +5 to +16 Vdc
  Input +5 V TTL with Pull-up, to V_{DD} of +5 to +16 Vdc

BCD-TO-SEVEN SEGMENT HEXADECIMAL LATCH/DECODER/DRIVER



L SUFFIX
CERAMIC PACKAGE
CASE 620

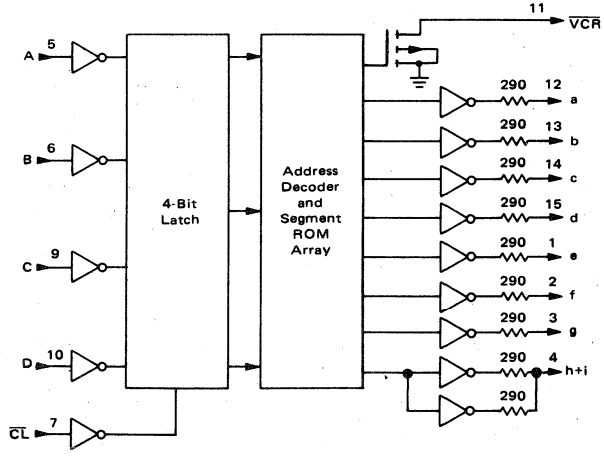


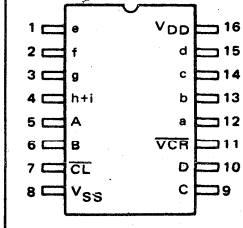
P SUFFIX
PLASTIC PACKAGE
CASE 648

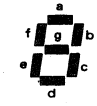
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

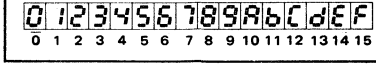
BLOCK DIAGRAM







ALPHANUMERIC DISPLAY



TRUTH TABLE

INPUTS				OUTPUTS									
D	C	B	A	a	b	c	d	e	f	g	h+i	VCR	DISPLAY
0	0	0	0	1	1	1	1	1	1	0	0	Open	0
0	0	0	1	0	1	1	0	0	0	0	0	Open	1
0	0	1	0	1	1	0	1	1	0	1	0	Open	2
0	0	1	1	1	1	1	1	0	0	1	0	Open	3
0	1	0	0	0	1	1	0	0	1	1	0	Open	4
0	1	0	1	1	0	1	1	0	1	1	0	Open	5
0	1	1	0	1	0	1	1	1	1	1	0	Open	6
0	1	1	1	1	1	1	0	0	0	0	0	Open	7
1	0	0	0	1	1	1	1	1	1	1	0	Open	8
1	0	0	1	1	1	1	1	0	1	1	0	Open	9
1	0	1	0	1	1	1	0	1	1	1	1	Open	A
1	0	1	1	0	0	1	1	1	1	1	1	Open	b
1	1	0	0	1	0	0	1	1	1	0	1	Open	C
1	1	0	1	0	1	1	1	1	0	1	1	Open	d
1	1	1	0	1	0	0	1	1	1	1	1	Open	E
1	1	1	1	1	0	0	0	1	1	1	1	0	F

MAXIMUM RATINGS (Voltages referenced to V_{SS}).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Maximum Continuous Output Power (Source) per Output @ 25 °C Pins 1, 2, 3, 12, 13, 14, 15 Pin 14	P_{OHmax}	 50 100	mW

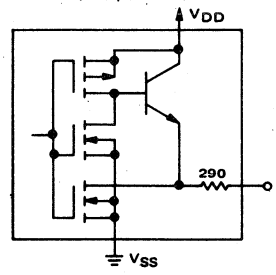
‡$P_{OHmax} = I_{OH}(V_{DD} - V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS (All voltages referenced to $V_{SS} = 0$, T_A -25°C)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}		4.5		16	Vdc
Input Voltage	V_{IL}		–		0.8	Vdc
	V_{IH}	V_{DD} = 15V V_{DD} = 5.0V	4.0 3.5		– –	Vdc
Input Current	I_{in}		–		±10	μAdc
Output $\overline{VCR}$, Pin 11	I_{OH}	$V_{OH} = V_{DD}$	–		±10	μAdc
Open Drain Output	I_{OL}	V_{OL} = 0.5V, V_{DD} = 5.0V V_{OL} = 0.5V, V_{DD} = 15V	0.2 1.0		– –	mA
Outputs a, b, c, d, e, f, g	I_{OH}	V_{OH} = 2.0V, V_{DD} = 5.0V V_{OH} = 1.5V, V_{DD} = 5.0V V_{OH} = 12V, V_{DD} = 15V V_{OH} = 11.5V, V_{DD} = 15V	-7.5 – -7.5 –		 -11.5 -11.5	mA
	I_{OL}	V_{OL} = 1.0V, V_{DD} = 5.0V V_{OL} = 1.0V, V_{DD} = 15V	0.1 0.5		– –	mA
Output h + i	I_{OH}	V_{OH} = 2.0V, V_{DD} = 5.0V V_{OH} = 1.5V, V_{DD} = 5.0V V_{OH} = 12V, V_{DD} = 15V V_{OH} = 11.5V, V_{DD} = 15V	-15 – -15 –		– -23 – -23	mA
	I_{OL}	V_{OL} = 1V, V_{DD} = 5.0 V V_{OL} = 1.0 V, V_{DD} = 15V	0.2 1.0		– –	mA

OUTPUT CIRCUIT
(Except Pin 11)



INPUT/OUTPUT FUNCTIONS

Segment Driver (a, b, c, d, e, f, g, h, i; Pins 1, 2, 3, 4, 12, 13, 14, 15)

The segment drivers are emitter-follower NPN-transistors. To limit the output current, a resistor typically 290 ohms is integrated internally at each output. Therefore, external resistors are not necessary when driving an LED at the supply voltage of V_{DD} = 5.0 volts.

OUTPUT ($\overline{VCR}$; Pin 11)

This output is activated (goes to low) whenever the address corresponding to program 16 is selected. Otherwise the output is open. See the truth table.

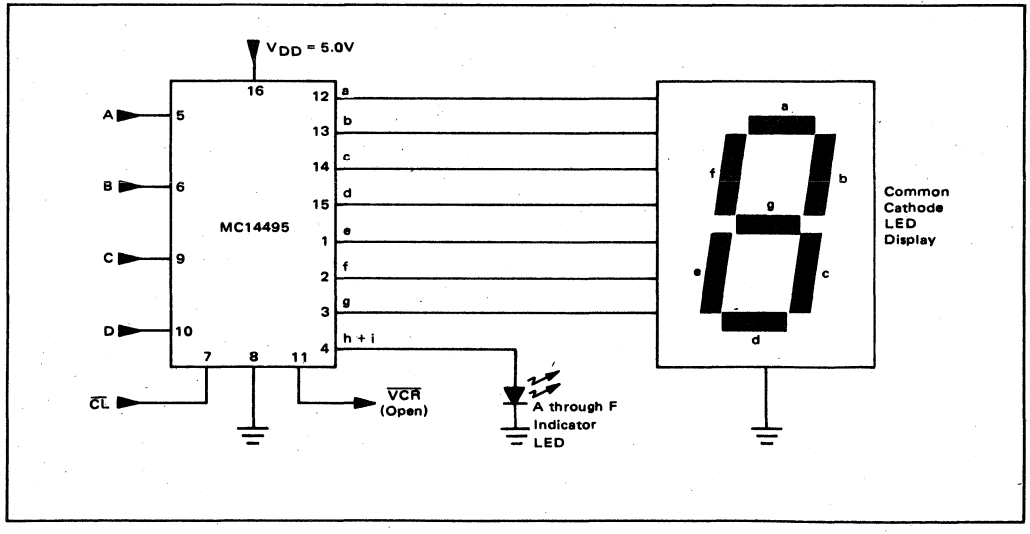
INPUT LATCH (A,B, C, D; Pins 5, 6, 8, 10)

The block diagram is shown on page 1. The inputs A, B, C, and D are fed to a 4-bit latch which is controlled by clock ($\overline{CL}$). Two modes of operation are available.

CLOCK ($\overline{CL}$; Pin 7)

The data on the inputs A, B, C and D will pass through the latch and will be displayed immediately when the clock is low. In this mode of operation the circuit is performing the function of a conventional decoder/driver. The data may be loaded into the latch when $\overline{CL}$ = low and will be latched with the rising edge of $\overline{CL}$. The data will remain stored as long as $\overline{CL}$ is high.

TYPICAL CIRCUIT @ V_{DD} = 5.0V



MOTOROLA

MC14500B

CMOS LSI

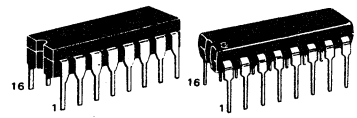
(LOW-POWER COMPLEMENTARY MOS)

INDUSTRIAL CONTROL UNIT

INDUSTRIAL CONTROL UNIT

The MC14500B Industrial Control Unit (ICU) is a single bit CMOS processor. The ICU is designed for use in systems requiring decisions based on successive single bit information. An external ROM stores the control program. With a program counter (and output latches and input multiplexers, if required) the ICU in a system forms a stored program controller that replaces combinatorial logic. Applications include relay logic processing, serial data manipulation and control. The ICU also may control an MPU or be controlled by an MPU.

- 16 Instructions
- DC to 1.0 MHz Operation at V_{DD} = 5 V
- On Chip Clock (Oscillator)
- Executes One Instruction per Clock Cycle
- 3 V to 18 V Operation
- Noise Immunity Typically 45% of V_{DD}
- Quiescent Current 5.0 μAdc Typical at V_{DD} = 5 V
- Capable of Driving One Low-Power Schottky Load or Two Low-Power TTL Loads over Full Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

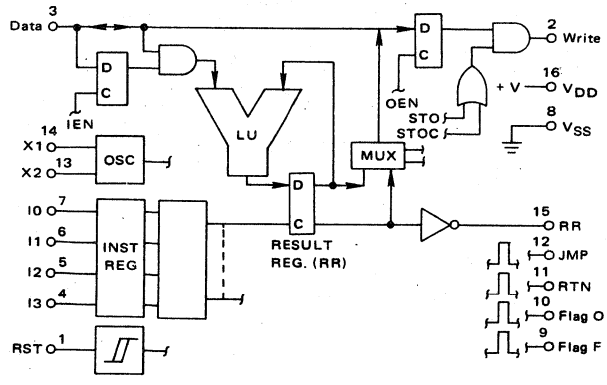
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

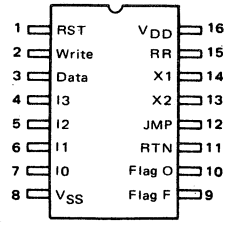
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

Detailed operation and applications are given in the "MC14500B Industrial Control Unit" handbook.

BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD}	T_{low}*		25°C			T_{high}*		Unit
			Vdc	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage #	"0 Level"	V_{IL}									Vdc
RST, D, X2											
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	11.0	–	11.0	8.25	–	11.0	–	
Input Voltage #	"0" Level	V_{IL}									Vdc
I0, I1, I2, I3											
(V_O = 4.5 or 0.5 Vdc)			5.0	–	0.8	–	1.1	0.8	–	0.8	
(V_O = 9.0 or 1.0 Vdc)			10	–	1.6	–	2.2	1.6	–	1.6	
(V_O = 13.5 or 1.5 Vdc)			15	–	2.4	–	3.4	2.4	–	2.4	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	2.0	–	2.0	1.9	–	2.0	–	
(V_O = 1.0 or 9.0 Vdc)			10	6.0	–	6.0	3.1	–	6.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	10	–	10	4.3	–	10	–	
Output Drive Current	Source	I_{OH}									mAdc
Data, Write (AL/CL/CP Device)											
(V_{OH} = 4.6 Vdc)			5.0	-1.0	–	-1.0	-2.0	–	-1.0	–	
(V_{OH} = 9.5 Vdc)			10	–	–	–	-6.0	–	–	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-12	–	–	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	1.6	–	1.6	3.2	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)			10	–	–	–	6.0	–	–	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	12	–	–	–	
Output Drive Current	Source	I_{OH}									mAdc
Other Outputs (AL Device)											
(V_{OH} = 2.5 Vdc)			5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)			5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)			10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)			15	-4.2	–	-3.4	8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current	Source	I_{OH}									mAdc
Other Outputs (CL/CP Device)											
(V_{OH} = 2.5 Vdc)			5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)			5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)			10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)			15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	3.6	–	3.0	8.8	–	2.4	–	

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Current, RST (AL/CL/CP Device)	I_{in}	15	25	–	–	150	–	–	250	μAdc
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (Data)	C_{in}	–	–	–	–	15	–	–	–	pF
Input Capacitance (All Other Inputs) (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0 10 15	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	μAdc
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0 10 15	– – –	20 40 80	– – –	0.005 0.010 0.015	20 40 80	– – –	150 300 600	μAdc
**Total Supply Current at an External Load Capacitance (C_L) on All Outputs	I_T	–	I_T = (1.5 μA/kHz) f + I_{DD} I_T = (3.0 μA/kHz) f + I_{DD} I_T = (4.5 μA/kHz) f + I_{DD}							μAdc

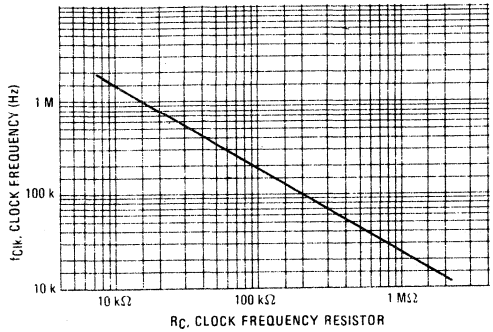
* T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
** The formulas given are for the typical characteristics only at 25°C.
# Noise immunity specified for worst-case input combination.

SWITCHING CHARACTERISTICS (T_A = 25°C; t_r = t_f = 20 ns for X and I inputs; C_L = 50 pF for JMP, X1, RR, Flag O, Flag F; C_L = 130 pF + 1TTL load for Data and Write.)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	All Types Typ	All Types Max	Unit
Propagation Delay Time X1 to RR	t_{PLH}, t_{PHL}	5.0 10 15	– – –	250 125 100	500 250 200	ns
X1 to Flag F, Flag O, RTN, JMP		5.0 10 15	– – –	200 100 85	400 200 170	ns
X1 to Write		5.0 10 15	– – –	225 125 100	450 250 200	ns
X1 to Data		5.0 10 15	– – –	250 120 100	500 240 200	ns
RST to RR		5.0 10 15	– – –	250 125 100	500 250 200	ns
RST to X1		5.0 10 15	– – –	450 200 150	Note 1	ns
RST to Flag F, Flag O, RTN, JMP		5.0 10 15	– – –	400 200 150	800 400 300	ns
RST to Write, Data		5.0 10 15	– – –	450 225 175	900 450 350	ns
Clock Pulse Width, X1	$t_{W(cl)}$	5.0 10 15	400 200 180	200 100 90	— — —	ns
Reset Pulse Width, RST	$t_{W(R)}$	5.0 10 15	500 250 200	250 125 100	— — —	ns
Setup Time — Instruction	$t_{su(I)}$	5.0 10 15	400 250 180	200 125 90	– – –	ns
Data	$t_{su(D)}$	5.0 10 15	200 100 80	100 50 40	– – –	ns
Hold Time — Instruction	$t_{h(I)}$	5.0 10 15	100 50 50	0 0 0	– – –	ns
Data	$t_{h(D)}$	5.0 10 15	200 100 100	100 50 50	– – –	ns

NOTE 1. Maximum Reset Delay may extend to one-half clock period.

FIGURE 1 – TYPICAL CLOCK FREQUENCY versus RESISTOR (R_C)

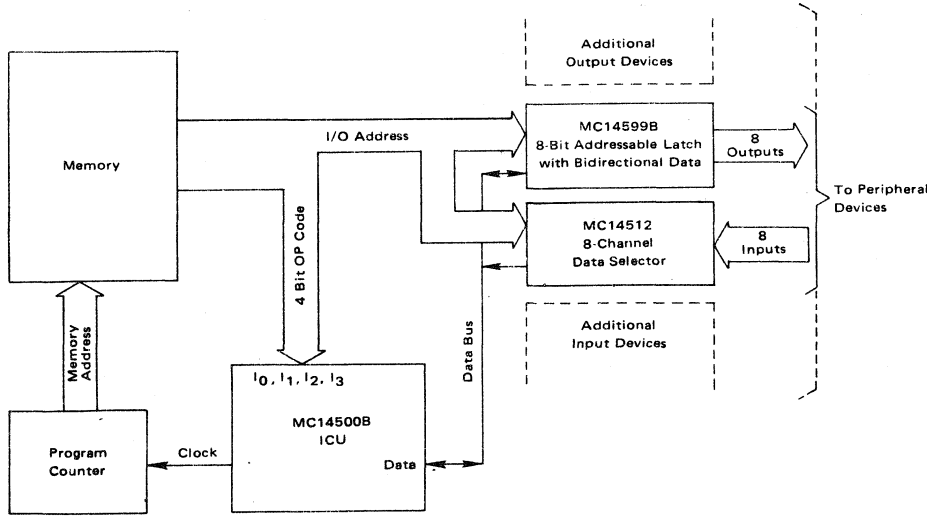


Pin No.	Function	Symbols
1	Chip Reset	RST
2	Write Pulse	Write
3	Data In/Out	Data
4	MSB Instruction Word	I_3
5	Bit 2 Instruction Word	I_2
6	Bit 1 Instruction Word	I_1
7	LSB Instruction Word	I_0
8	Negative Supply (Ground)	V_{SS}
9	Flag on NOP F	Flag F
10	Flag on NOP O	Flag O
11	Subroutine Return Flag	RTN
12	Jump Instruction Flag	JMP
13	Oscillator Input	X2
14	Oscillator Output	X1
15	Result Register	RR
16	Positive Supply	V_{DD}

TABLE 1. MC14500B INSTRUCTION SET

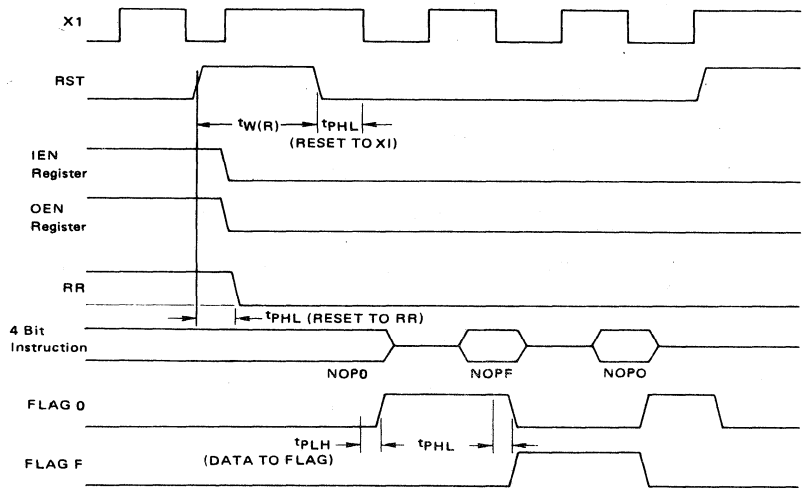
Instruction Code	Mnemonic	Action
0 0000	NOPO	No change in registers. RR → RR, Flag O → ⎍
1 0001	LD	Load result register. Data → RR
2 0010	LDC	Load complement. $\overline{Data}$ → RR
3 0011	AND	Logical AND. RR·Data → RR
4 0100	ANDC	Logical AND complement. RR·$\overline{Data}$ → RR
5 0101	OR	Logical OR. RR + Data → RR
6 0110	ORC	Logical OR complement. RR + $\overline{Data}$ → RR
7 0111	XNOR	Exclusive NOR. If RR = Data, RR → 1
8 1000	STO	Store. RR → Data Pin, Write → ⎍
9 1001	STOC	Store complement. $\overline{RR}$ → Data Pin, Write → ⎍
A 1010	IEN	Input enable. Data → IEN Register
B 1011	OEN	Output enable. Data → OEN Register
C 1100	JMP	Jump. JMP Flag → ⎍
D 1101	RTN	Return. RTN Flag → ⎍ and skip next instruction
E 1110	SKZ	Skip next instruction if RR = 0
F 1111	NOPF	No change in registers. RR → RR, Flag F → ⎍

FIGURE 2 – OUTLINE OF A TYPICAL ORGANIZATION FOR A MC14500B-BASED SYSTEM

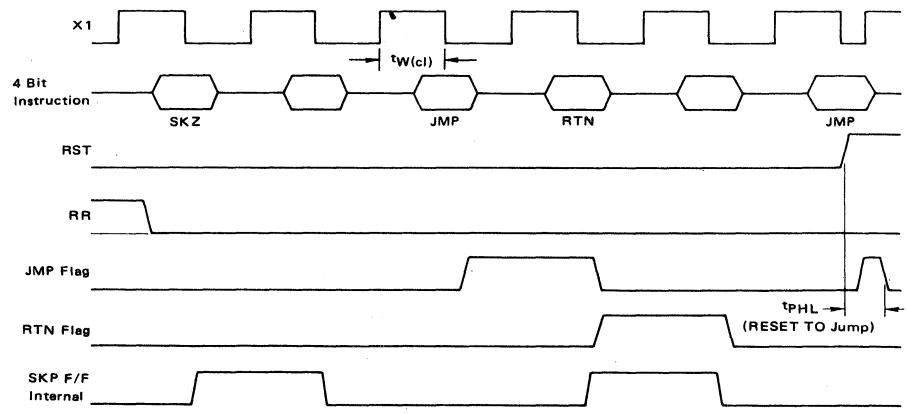


TIMING WAVEFORMS

Instructions NOPO, NOPF
RR, IEN, OEN remain unaffected



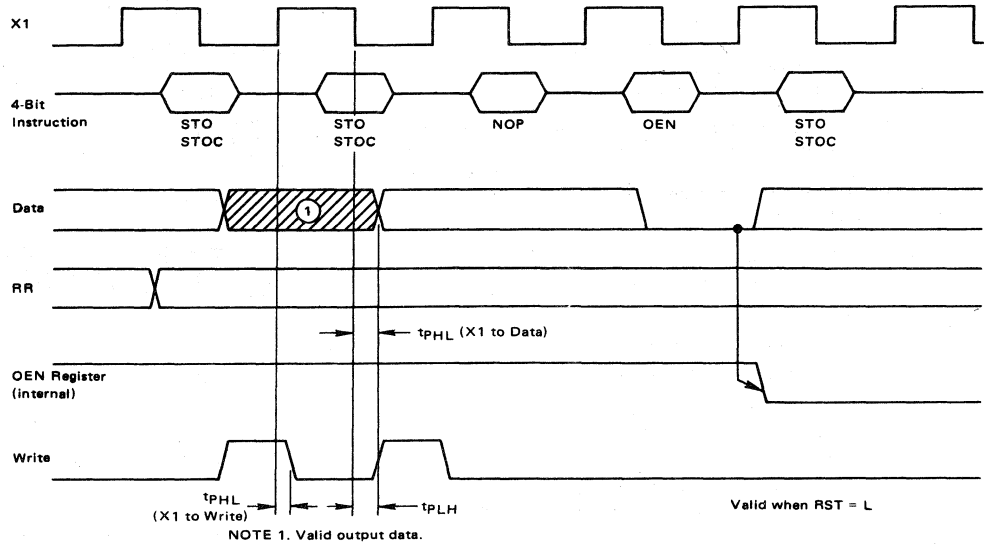
Instructions SKZ, JMP, RTN
RR, IEN, OEN remain unaffected



*Instructions Ignored.

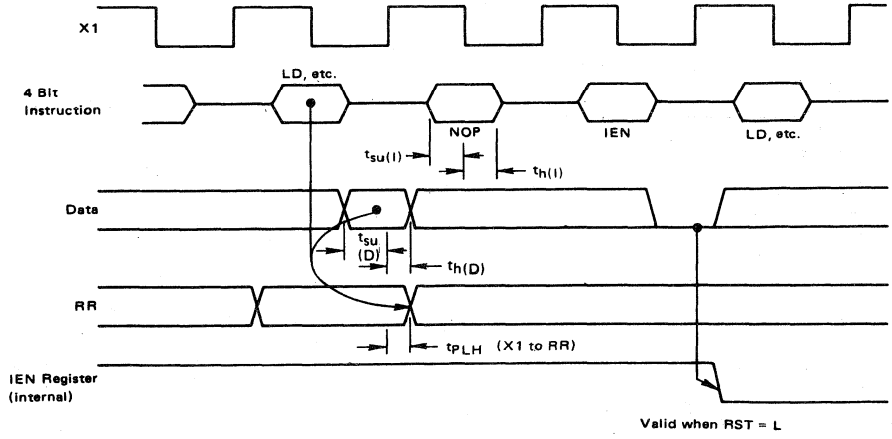
TIMING WAVEFORMS

Instructions STO, STOC, OEN



NOTE 1. Valid output data.

Instructions LD, LDC, AND, ANDC OR, ORC, XNOR, IEN



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14501UB

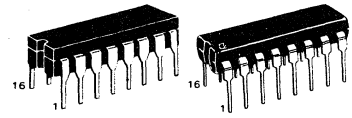
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE GATE
DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE

The MC14501UB constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

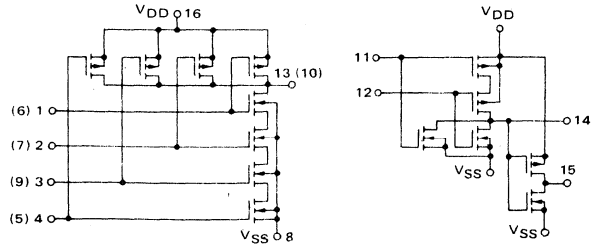
ORDERING INFORMATION

MC14XXXUB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

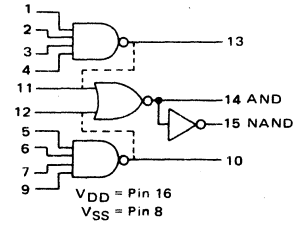
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



Numbers in parenthesis are for second 4-input gate.

LOGIC DIAGRAM
(POSITIVE LOGIC)



Use Dotted Connection Externally to Obtain 8-Input AND/NAND

Note: Pin 14 must not be used as an input to the inverter.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.4	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.6	
(V_O = 1.4 or 3.6 Vdc) "1" Level	V_{IH}	5.0	3.6	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.1	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	–	11.25	8.25	–	11.0	–	
Output Drive Current	I_{OH}									mAdc
(AL Device)										
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
(V_{OH} = 9.5 Vdc) NAND		10	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OH} = 13.5 Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OH} = 2.5 Vdc) NOR		5.0	−2.1	–	−1.75	−3.0	–	−1.22	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.42	–	−0.35	−0.63	–	−0.24	–	
(V_{OH} = 9.5 Vdc)		10	−1.06	–	−0.88	−1.58	–	−0.62	–	
(V_{OH} = 13.5 Vdc)		15	−3.1	–	−2.63	−6.12	–	−1.84	–	
(V_{OH} = 2.5 Vdc) NOR-		5.0	−3.6	–	−3.0	−5.1	–	−2.1	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.72	–	−0.6	−1.08	–	−0.42	–	
(V_{OH} = 9.5 Vdc) Inverter		10	−1.8	–	−1.5	−2.7	–	−1.05	–	
(V_{OH} = 13.5 Vdc)		15	−5.4	–	−4.5	−10.5	–	−3.15	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc) NAND		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
(V_{OL} = 0.4 Vdc) NOR		5.0	0.92	–	0.77	1.32	–	0.54	–	mAdc
(V_{OL} = 0.5 Vdc)		10	2.34	–	1.95	3.37	–	1.36	–	
(V_{OL} = 1.5 Vdc)		15	6.12	–	5.1	13.2	–	3.57	–	
(V_{OL} = 0.4 Vdc) NOR-		5.0	1.54	–	1.28	2.2	–	0.90	–	mAdc
(V_{OL} = 0.5 Vdc) Inverter		10	3.90	–	3.25	5.63	–	2.27	–	
(V_{OL} = 1.5 Vdc)		15	10.2	–	8.5	22	–	5.95	–	
Output Drive Current	I_{OH}									mAdc
(CL/CP Device)										
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	−0.8	−1.7	–	−0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.2	–	−0.16	−0.36	–	−0.12	–	
(V_{OH} = 9.5 Vdc) NAND		10	−0.5	–	−0.4	−0.9	–	−0.3	–	
(V_{OH} = 13.5 Vdc)		15	−1.4	–	−1.2	−3.5	–	−1.0	–	
(V_{OH} = 2.5 Vdc) NOR		5.0	−1.68	–	−1.4	−3.0	–	−1.05	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.34	–	−0.28	−0.63	–	−0.21	–	
(V_{OH} = 9.5 Vdc)		10	−0.84	–	−0.7	−1.58	–	−0.52	–	
(V_{OH} = 13.5 Vdc)		15	−2.52	–	−2.1	−6.12	–	−1.57	–	
(V_{OH} = 2.5 Vdc) NOR-		5.0	−2.88	–	−2.4	−5.1	–	−1.8	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.58	–	−0.48	−1.08	–	−0.36	–	
(V_{OH} = 9.5 Vdc) Inverter		10	−1.44	–	−1.2	−2.7	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.32	–	−3.6	−10.5	–	−2.7	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc) NAND		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
(V_{OL} = 0.4 Vdc) NOR		5.0	0.79	–	0.66	1.32	–	0.54	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.98	–	1.65	3.37	–	1.36	–	
(V_{OL} = 1.5 Vdc)		15	5.4	–	4.5	13.2	–	3.57	–	
(V_{OL} = 0.4 Vdc) NOR-		5.0	1.32	–	1.1	2.2	–	0.90	–	mAdc
(V_{OL} = 0.5 Vdc) Inverter		10	3.3	–	2.75	5.63	–	2.27	–	
(V_{OL} = 1.5 Vdc)		15	9.0	–	7.5	22.0	–	5.95	–	

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.2\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (2.4\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.6\ \mu A/kHz)\ f + I_{DD}$							

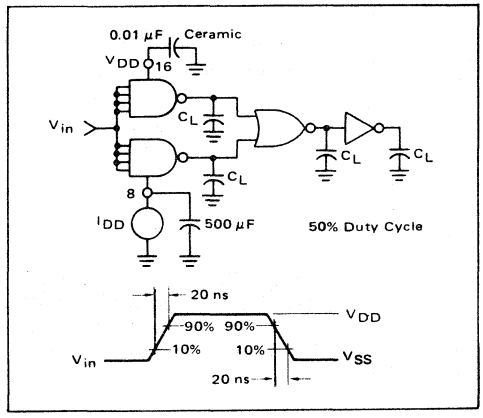
*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS** (C_L = 50 pF, T_A = 25°C)

Characteristic		Figure	Symbol	V_{DD}	Typ All Types	Max	Unit
Output Rise Time	NAND, NOR	2, 3	t_{TLH}				ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns				5.0	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns				10	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns				15	65	130	
Output Fall Time	NAND, NOR	2, 3	t_{THL}				ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns				5.0	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns				10	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns				15	40	80	
Output Rise Time	NOR-Inverter	3	t_{TLH}				ns
t_{TLH} = (1.35 ns/pF) C_L + 32.5 ns				5.0	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns				10	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 17 ns				15	40	80	
Output Fall Time	NOR-Inverter	3	t_{THL}				ns
t_{THL} = (0.67 ns/pF) C_L + 26.5 ns				5.0	60	120	
t_{THL} = (0.45 ns/pF) C_L + 17.5 ns				10	40	80	
t_{THL} = (0.37 ns/pF) C_L + 11.5 ns				15	30	60	
Propagation Delay Time	NAND	2	t_{PLH}, t_{PHL}				ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 45 ns				50	130	260	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 37 ns				10	70	140	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns				15	50	100	
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns	NOR	3	t_{PLH}, t_{PHL}	5.0	115	230	ns
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 32 ns				10	65	130	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 20 ns				15	45	90	
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 45 ns	NOR-Inverter	3	t_{PLH}, t_{PHL}	5.0	130	260	ns
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 37 ns				10	70	140	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns				15	50	100	

** The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 2 – 4-INPUT "NAND" GATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

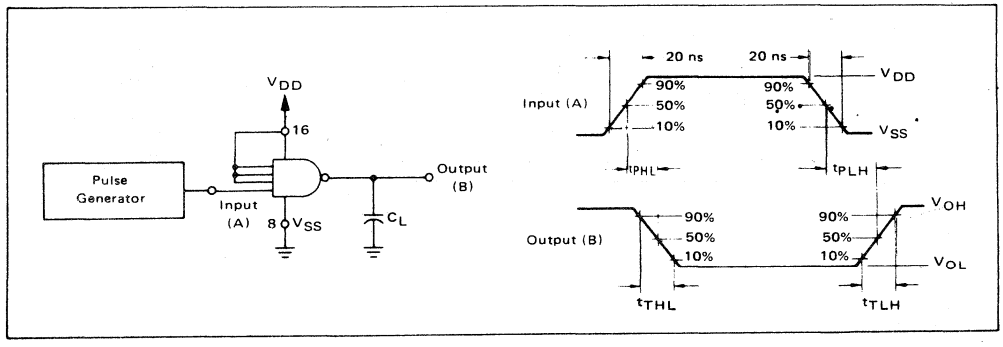
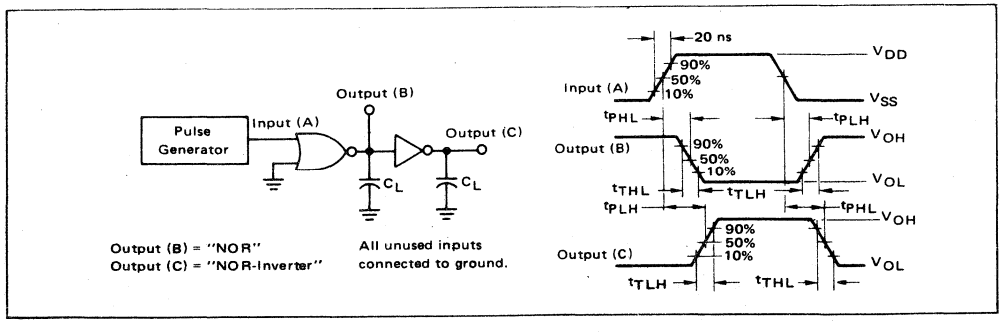


FIGURE 3 – "NOR" GATE and "NOR-INVERTER" SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MOTOROLA

MC14502B

STROBED HEX INVERTER/BUFFER

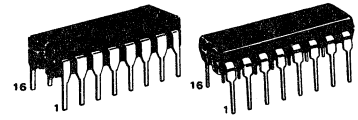
The MC14502B is a strobed hex buffer/inverter with 3-state output, an inhibit control, and guaranteed TTL drive over the temperature range. The 3-state output simplifies design by allowing a common bus.

- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Separate Output Disable Control
- 3-State Output
- Output Impedance = 200 ohms @ 5.0 V Supply Guaranteed Over Full Temperature Range
- Input Impedance = 10^{12} ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

STROBED HEX INVERTER/BUFFER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

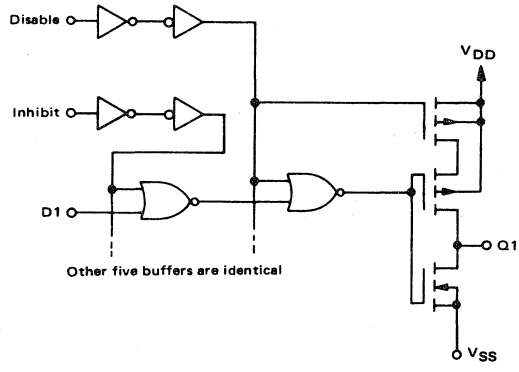
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

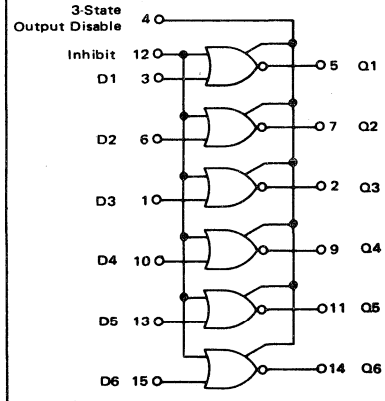
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	30	mAdc
Operating Temperature Range — AL Device	T_A	−55 to +125	°C
CL/CP Device		−40 to +85	
Storage Temperature Range	T_{stg}	−65 to +150	°C

CIRCUIT DIAGRAM



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

D_n	Inhibit	Disable	Q_n
0	0	0	1
1	0	0	0
X	1	0	0
X	X	1	High Impedance

X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	3.5	–	2.8	6.6	–	2.0	–	mAdc
(V_{OL} = 0.5 Vdc)		10	7.8	–	6.3	17	–	4.4	–	
(V_{OL} = 1.5 Vdc)		15	29	–	24	66	–	16	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	2.3	–	1.9	6.6	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	5.0	–	4.2	17	–	3.4	–	
(V_{OL} = 1.5 Vdc)		15	19	–	16	66	–	13	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (2.7 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (5.3 µA/kHz) f + I_{DD}							
		15	I_T = (8.0 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (0.6 ns/pF) C_L + 10 ns		5.0	–	40	80	
t_{THL} = (0.3 ns/pF) C_L + 5.0 ns		10	–	20	40	
t_{THL} = (0.27 ns/pF) C_L + 1.5 ns		15	–	15	30	
Propagation Delay Time Data to Q	t_{PHL}	5.0	–	135	270	ns
		10	–	55	110	
		15	–	40	80	
Propagation Delay Time, Inhibit to Q	t_{PHL}	5.0	–	335	670	ns
		10	–	145	290	
		15	–	95	190	
Propagation Delay Time Data to Q, Inhibit to Q	t_{PLH}	5.0	–	295	590	ns
		10	–	130	260	
		15	–	95	190	
3-State Propagation Delay, Output "1" to High Impedance	t_{PHZ}	5.0	–	65	130	ns
		10	–	30	60	
		15	–	25	50	
3-State Propagation Delay, High Impedance to "1" Level	t_{PZH}	5.0	–	260	520	ns
		10	–	105	210	
		15	–	80	160	
3—State Propagation Delay, Output "0" to High Impedance	t_{PLZ}	5.0	–	150	300	ns
		10	–	70	140	
		15	–	55	110	
3-State Propagation Delay, High Impedance to "0" Level	t_{PZL}	5.0	–	160	320	ns
		10	–	65	130	
		15	–	50	100	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT TEST CIRCUIT (I_{OH})

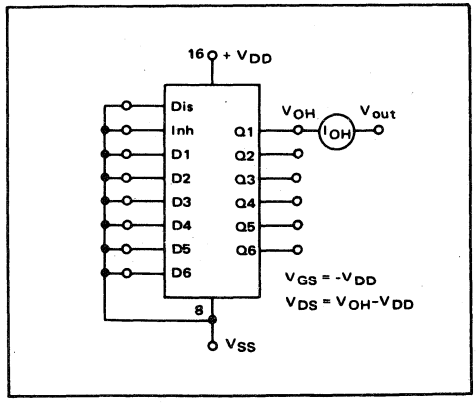


FIGURE 2 – TYPICAL OUTPUT SINK CURRENT TEST CIRCUIT (I_{OL})

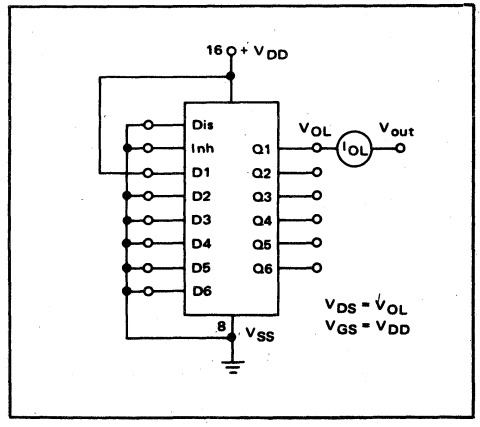


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

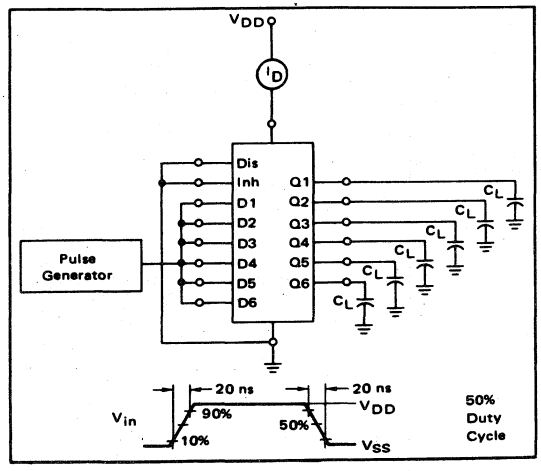


FIGURE 4 – AMBIENT TEMPERATURE POWER DERATING

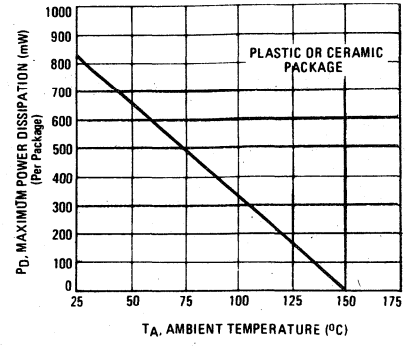


FIGURE 5 – AC TEST CIRCUIT AND WAVEFORMS (t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH})

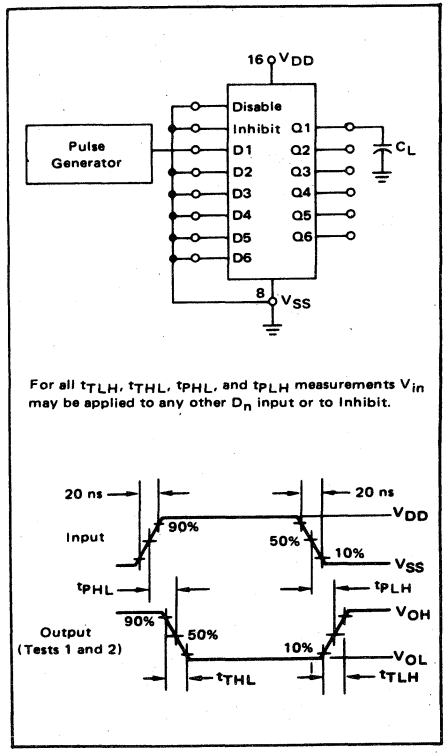
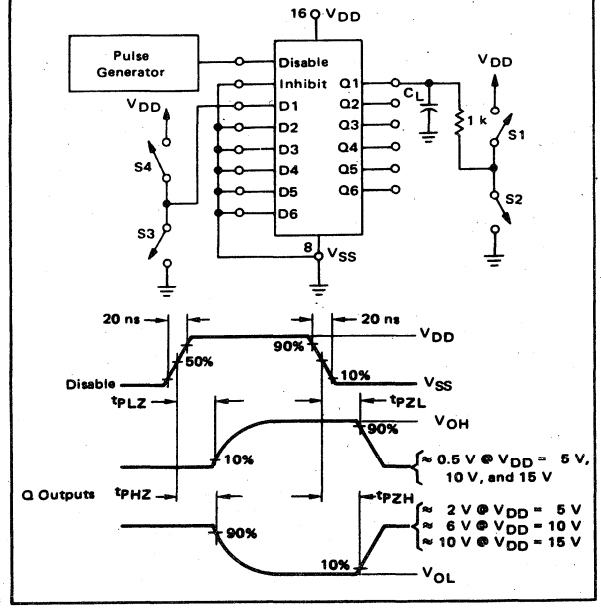


FIGURE 6 – 3-STATE AC TEST CIRCUIT AND WAVEFORMS (t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL})

Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open



MOTOROLA

MC14503B

HEX NON-INVERTING 3-STATE BUFFER

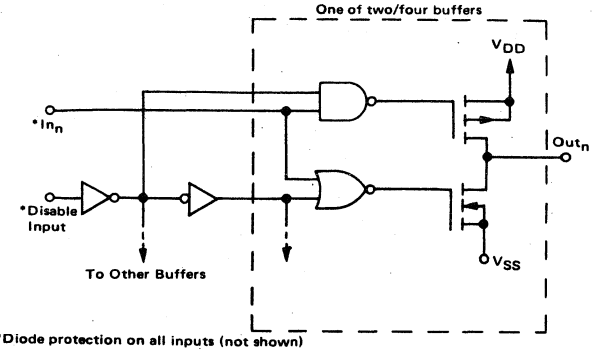
The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

- 3-State Outputs
- TTL Compatible — Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Symmetrical Turn-On and Turn-off Delays
- Symmetrical Output Rise and Fall Times
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	25	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

CIRCUIT DIAGRAM



*Diode protection on all inputs (not shown)

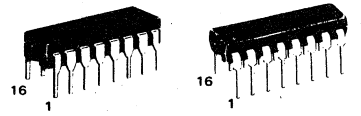
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX 3-STATE BUFFER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix

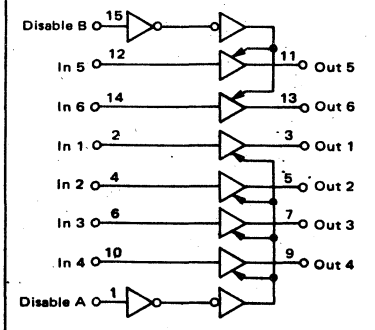
Suffix	Denotes
L	Ceramic Package
P	Plastic Package
A	Extended Operating Temperature Range
C	Limited Operating Temperature Range

TRUTH TABLE

In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

X = Don't Care

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Noise Immunity# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.75	
"1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.4 or 3.6 Vdc)		10	7.0	–	7.0	5.5	–	7.0	–	
(V_O = 2.8 or 7.2 Vdc)		15	11.25	–	11.25	8.25	–	11.25	–	
(V_O = 3.5 or 11.5 Vdc)										
Output Drive Current (AL Device)***	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		4.5	-4.3	–	-3.6	-5.0	–	-2.5	–	
(V_{OH} = 2.5 Vdc)		5.0	-5.8	–	-4.80	-6.1	–	-3.0	–	
(V_{OH} = 4.6 Vdc)		5.0	-1.2	–	-1.02	-1.4	–	-0.7	–	
(V_{OH} = 9.5 Vdc)		10	-3.1	–	-2.60	-3.7	–	-1.8	–	
(V_{OH} = 13.5 Vdc)		15	-8.2	–	-6.80	-14.1	–	-4.8	–	
Sink	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		4.5	2.2	–	1.8	2.1	–	1.2	–	
(V_{OL} = 0.4 Vdc)		5.0	2.6	–	2.1	2.3	–	1.3	–	
(V_{OL} = 0.5 Vdc)		10	6.5	–	5.5	6.2	–	3.8	–	
(V_{OL} = 1.5 Vdc)		15	19.2	–	16.10	25.00	–	11.2	–	
Output Drive Current (CL/CP Device)***	I_{OH}						–			mAdc
(V_{OH} = 2.5 Vdc) Source		4.75	-4.0	–	-3.60	-5.5	–	-2.4	–	
(V_{OH} = 2.5 Vdc)		5.0	-4.6	–	-4.20	-6.1	–	-3.0	–	
(V_{OH} = 4.6 Vdc)		5.0	-1.0	–	-0.88	-1.4	–	-0.7	–	
(V_{OH} = 9.5 Vdc)		10	-2.4	–	-2.20	-3.7	–	-1.8	–	
(V_{OH} = 13.5 Vdc)		15	-6.6	–	-6.00	-14.1	–	-4.8	–	
Sink	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		4.75	2.1	–	1.95	2.2	–	1.25	–	
(V_{OL} = 0.4 Vdc)		5.0	2.3	–	2.10	2.3	–	1.3	–	
(V_{OL} = 0.5 Vdc)		10	6.0	–	5.45	6.2	–	3.8	–	
(V_{OL} = 1.5 Vdc)		15	15.2	–	13.80	25.00	–	11.2	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±3.0	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_Q	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**†	I_{DD}	5.0	(I_T = 2.5 µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package)		10	(I_T = 6.0 µA/kHz) f + I_{DD}							
(C_L = 50 pF on all outputs)		15	(I_T = 10 µA/kHz) f + I_{DD}							
(All outputs switching, 50% Duty Cycle)										
3-State Output Leakage Current	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	µAdc
(AL Device)			–		–			–		
3-State Output Leakage Current	I_{TL}	15	–	±1.0	–	±0.0001	±1.0	–	±7.5	µAdc
(CL/CP Device)			–		–			–		

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

I_T is in µA (per package) C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C
***Care must be taken not to exceed maximum current ratings (see maximum ratings table and Figure 1).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V_{CC}	All Types Typ	All Types Max	Unit
Output Rise Time	t_{TLH}				ns
t_{TLH} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{TLH} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{TLH} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Output Fall Time	t_{THL}				ns
t_{THL} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{THL} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{THL} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Turn-Off Delay Time, all Outputs	t_{PLH}				ns
t_{PLH} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PLH} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PLH} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
Turn-On Delay Time, all Outputs	t_{PHL}				ns
t_{PHL} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PHL} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PHL} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
3-State Propagation Delay Time	t_{PHZ}	5.0	75	150	ns
Output "1" to High Impedance		10	40	80	
		15	35	70	
Output "0" to High Impedance	t_{PLZ}	5.0	80	160	ns
		10	40	80	
		15	35	70	
High Impedance to "1" Level	t_{PZH}	5.0	65	130	ns
		10	25	50	
		15	20	40	
High Impedance to "0" Level	t_{PZL}	5.0	100	200	ns
		10	35	70	
		15	25	50	

*The formulas given are for the typical characteristics only.

FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING

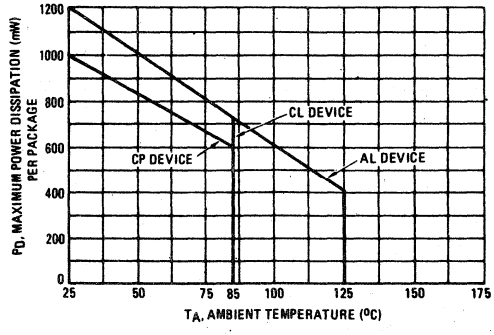


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH})

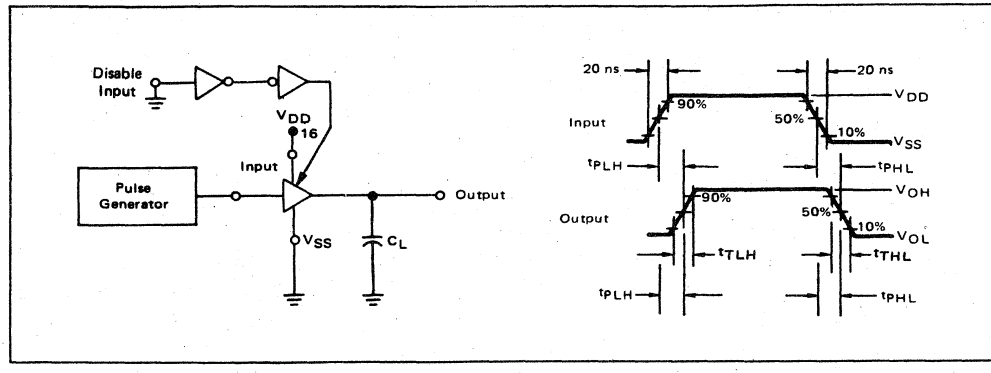
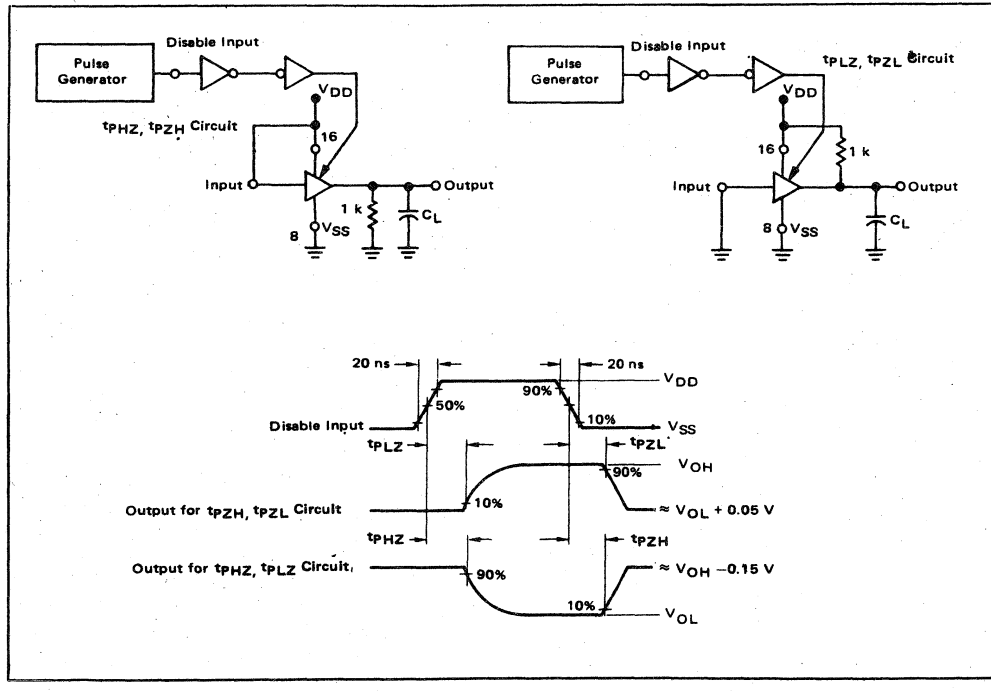


FIGURE 3 – 3 STATE AC TEST CIRCUITS AND WAVEFORMS
(t_{PLZ}, t_{PHZ}, t_{PZH}, t_{PZL})



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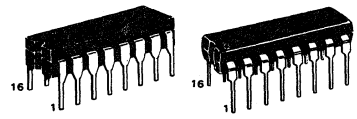
TTL or CMOS to CMOS
HEX LEVEL SHIFTER

HEX LEVEL SHIFTER FOR TTL to CMOS or CMOS to CMOS

The MC14504B is a hex non-inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level. Either up or down level translating is accomplished by selection of power supply levels V_{DD} and V_{CC}. The V_{CC} level sets the input signal levels while V_{DD} selects the output voltage levels.

Supply current is typically 1 nA @ V_{DD} = 10 V for CMOS to CMOS operation. When translating from TTL to CMOS supply current is typically 2.5 mA taken from V_{CC}.

- UP Translates from a Low to a High Voltage or
  DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for V_{DD} and V_{CC}
- Diode Protected Inputs to V_{SS}
- Capable of Driving Two Low Power TTL Loads,
  One Low Power Schottky TTL Load or
  Two HTL Loads over the Rated Temperature Range



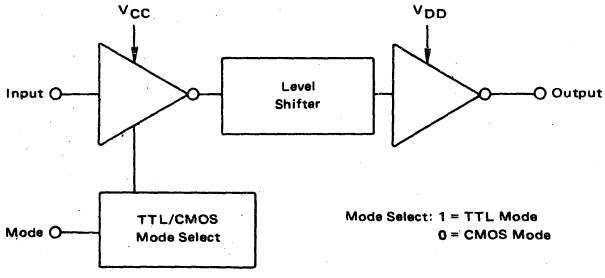
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

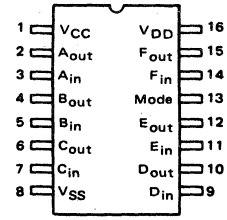
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

LOGIC DIAGRAM



1/6 of package shown.

PIN ASSIGNMENT



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	−0.5 to +18	Vdc
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq V_{in} \leq V_{CC}$ and $V_{SS} \leq V_{out} \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either V_{SS} or V_{CC}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{CC} Vdc	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	–	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = 0 V		–	10	–	0.05	–	0	0.05	–	0.05	
		–	15	–	0.05	–	0	0.05	–	0.05	
V_{in} = V_{CC} "1" Level	V_{OH}	–	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		–	10	9.95	–	9.95	10	–	9.95	–	
		–	15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}										Vdc
(V_{OL} = 1.0 Vdc) TTL–CMOS		5	10	–	0.8	–	1.3	0.8	–	0.8	
(V_{OL} = 1.5 Vdc) TTL–CMOS		5	15	–	0.8	–	1.3	0.8	–	0.8	
(V_{OL} = 1.0 Vdc) CMOS–CMOS		5	10	–	1.5	–	2.25	1.5	–	1.4	
(V_{OL} = 1.5 Vdc) CMOS–CMOS		5	15	–	1.5	–	2.25	1.5	–	1.5	
(V_{OL} = 1.5 Vdc) CMOS–CMOS		10	15	–	3.0	–	4.5	3.0	–	2.9	
Input Voltage "1" Level	V_{IH}										Vdc
(V_{OH} = 9.0 Vdc) TTL–CMOS		5	10	2.0	–	2.0	1.5	–	2.0	–	
(V_{OH} = 13.5 Vdc) TTL–CMOS		5	15	2.0	–	2.0	1.5	–	2.0	–	
(V_{OH} = 9.0 Vdc) CMOS–CMOS		5	10	3.6	–	3.5	2.75	–	3.5	–	
(V_{OH} = 13.5 Vdc) CMOS–CMOS		5	15	3.6	–	3.5	2.75	–	3.5	–	
(V_{OH} = 13.5 Vdc) CMOS–CMOS		10	15	7.1	–	7.0	5.5	–	7.0	–	
Output Drive Current (AL Device)	I_{OH}										mAdc
(V_{OH} = 2.5 Vdc) Source		–	5.0	−3.0	–	−24	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		–	5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		–	10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		–	15	−4.2	–	3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	–	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		–	10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		–	15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}										mAdc
(V_{OH} = 2.5 Vdc) Source		–	5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		–	5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		–	10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		–	15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{QL}	–	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		–	10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		–	15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL)	I_{in}	–	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP)	I_{in}	–	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD} or	–	5.0	–	0.05	–	0.0005	0.05	–	1.5	μAdc
(Per Package)	I_{CC}	–	10	–	0.10	–	0.0010	0.10	–	3.0	
CMOS–CMOS Mode		–	15	–	0.20	–	0.0015	0.20	–	6.0	
Quiescent Current (CL/CP Device)	I_{DD} or	–	5.0	–	0.5	–	0.0005	0.5	–	3.8	μAdc
(Per Package)	I_{CC}	–	10	–	1.0	–	0.0010	1.0	–	7.5	
CMOS–CMOS Mode		–	15	–	2.0	–	0.0015	2.0	–	15.0	
Quiescent Current (AL/CL/CP Device)	I_{DD}	5.0	5.0	–	0.5	–	0.0005	0.5	–	3.8	μAdc
(Per Package)		5.0	10	–	1.0	–	0.0010	1.0	–	7.5	
TTL–CMOS Mode		5.0	15	–	2.0	–	0.0015	2.0	–	15.0	
Quiescent Current (AL/CL/CP Device)	I_{CC}	5.0	5.0	–	5.0	–	2.5	5.0	–	6.0	mAdc
(Per Package)		5.0	10	–	5.0	–	2.5	5.0	–	6.0	
TTL–CMOS Mode		5.0	15	–	5.0	–	2.5	5.0	–	6.0	

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	Shifting Mode	V_{CC} Vdc	V_{DD} Vdc	Limits Min	Limits Typ	Limits Max	Units
Propagation Delay, High to Low	t_{PHL}	TTL–CMOS	5.0	10	–	120	–	ns
		$V_{DD} > V_{CC}$	5.0	15	–	120	–	
		CMOS–CMOS	5.0	10	–	100	–	
		$V_{DD} > V_{CC}$	5.0	15	–	120	–	
			10	15	–	50	–	
		CMOS–CMOS	10	5.0	–	160	–	
		$V_{CC} > V_{DD}$	15	5.0	–	160	–	
			15	10	–	160	–	
Propagation Delay, Low to High	t_{PHL}	TTL–CMOS	5.0	10	–	200	–	ns
		$V_{DD} > V_{CC}$	5.0	15	–	160	–	
		CMOS–CMOS	5.0	10	–	100	–	
		$V_{DD} > V_{CC}$	5.0	15	–	120	–	
			10	15	–	50	–	
		CMOS–CMOS	10	5.0	–	160	–	
		$V_{CC} > V_{DD}$	15	5.0	–	160	–	
			15	10	–	65	–	
Output Rise and Fall Time	t_{TLH}, t_{THL}	ALL	–	5.0	–	100	–	ns
			–	10	–	50	–	
			–	15	–	40	–	

FIGURE 1 – INPUT SWITCHPOINT CMOS to CMOS MODE

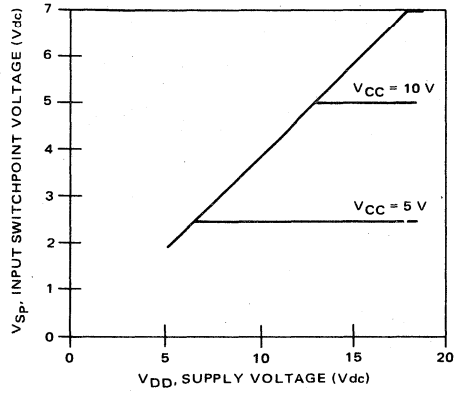


FIGURE 2 – INPUT SWITCHPOINT TTL to CMOS MODE

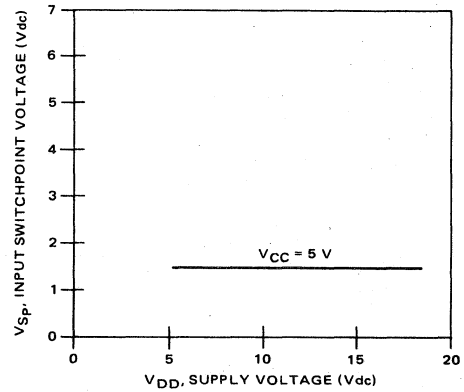


FIGURE 3 – OPERATING BOUNDARY CMOS to CMOS MODE

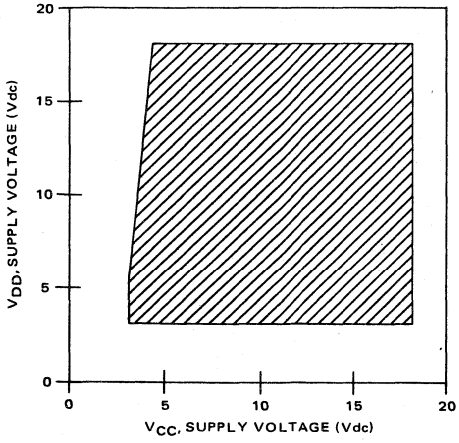
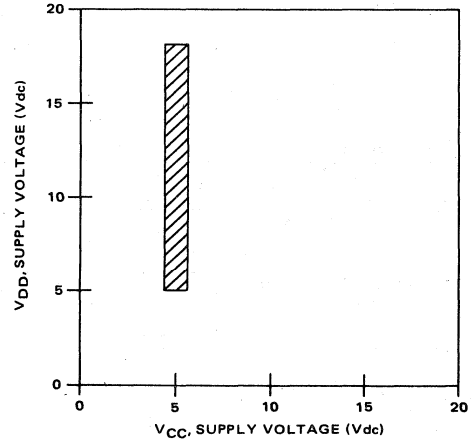


FIGURE 4 – OPERATING BOUNDARY TTL to CMOS MODE



MOTOROLA

MCM14505

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

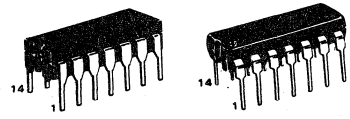
64-BIT (64 x 1) STATIC RANDOM ACCESS MEMORY

64-BIT STATIC RANDOM ACCESS MEMORY

The MCM14505 64-bit random access memory is fully decoded on the chip and organized as 64 one-bit words (64 X 1). Medium speed operation and micropower supply requirements make this device useful for scratch pad or buffer memory applications where power must be conserved or where battery operation is required.

When used with a battery backup, the MCM14505 can be utilized as an alterable read-only memory, allowing the battery to retain information in the memory when the system is powered down, and allowing the battery to charge when power is applied. The micropower requirements of this memory allow quiescent battery operation for great lengths of time without significant discharging.

- Quiescent Current = 50 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Read/Write Control Line
- Wired-OR Output Capability (3-State Output) for Memory Expansion
- Access Time = 180 ns typical at V_{DD} = 10 Vdc
- Write Cycle Time = 275 ns typical at V_{DD} = 10 Vdc
- Fully Buffered Low Capacitance Inputs
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

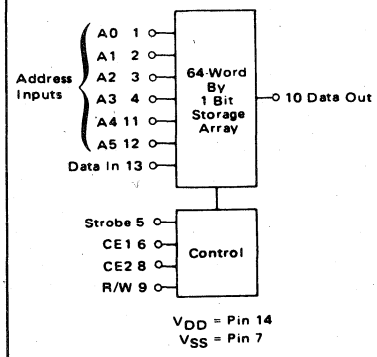
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Noise Immunity #	V_{NL}									Vdc
($\triangle V_{out} \leq$ 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq$ 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.3	–	0.25	0.35	–	0.18	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.9	–	0.75	1.2	–	0.50	–	
(V_{OL} = 1.5 Vdc)		15	2.2	–	1.7	4.5	–	1.2	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.2	–	0.15	0.35	–	0.1	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.6	–	0.5	1.2	–	0.4	–	
(V_{OL} = 1.5 Vdc)		15	3.9	–	0.75	4.5	–	0.6	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±1.0	–	±0.00001	±1.0	–	±14	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.050	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.100	10	–	300	
		15	–	20	–	0.150	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.050	50	–	375	µAdc
(Per Package)		10	–	100	–	0.100	100	–	750	
		15	–	200	–	0.150	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.28 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.56 µA/kHz) f + I_{DD}							
		15	I_T = (3.85 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (2.43 ns/pF) C_L + 58.5 ns		5.0	–	180	360	
t_{TLH} = (1.08 ns/pF) C_L + 36 ns		10	–	90	180	
t_{TLH} = (0.72 ns/pF) C_L + 39 ns		15	–	75	150	
Output Fall Time	t_{THL}					ns
t_{THL} = (2.16 ns/pF) C_L + 52 ns		5.0	–	160	320	
t_{THL} = (0.96 ns/pF) C_L + 32 ns		10	–	80	160	
t_{THL} = (0.69 ns/pF) C_L + 33 ns		15	–	65	130	
Propagation Delay Time	$t_{acc(R)}$					ns
Read Access Time						
$t_{acc(R)}$ = (1.4 ns/pF) C_L + 385 ns		5.0	–	455	750	
$t_{acc(R)}$ = (10.7 ns/pF) C_L + 175 ns		10	–	210	400	
$t_{acc(R)}$ = (0.5 ns/pF) C_L + 105 ns		15	–	130	300	
Strobe Down Time	t_{WL}					ns
		5.0	500	100	–	
		10	125	50	–	
		15	95	75	–	
Address Setup Time	t_{su}					ns
		5.0	300	-100	–	
		10	120	-40	–	
		15	90	-25	–	
Data Setup Time	$t_{su(D)}$					ns
		5.0	200	70	–	
		10	75	25	–	
		15	55	20	–	
Read Setup Time	$t_{su(R)}$					ns
		5.0	270	90	–	
		10	60	20	–	
		15	45	15	–	
Write Setup Time	$t_{su(W)}$					ns
		5.0	400	80	–	
		10	100	25	–	
		15	75	11	–	
Address Release Time	$t_{rel(R)}$					ns
		5.0	75	15	–	
		10	25	10	–	
		15	20	5.0	–	
Data Hold Time	$t_{h(D)}$					ns
		5.0	50	0	–	
		10	15	0	–	
		15	10	0	–	
Read Release Time	$t_{rel(R)}$					ns
		5.0	0	-90	–	
		10	0	-25	–	
		15	0	-10	–	
Write Release Time	$t_{rel(W)}$					ns
		5.0	0	5.0	–	
		10	0	10	–	
		15	0	30	–	
Read Cycle Time	$t_{cyc(R)}$					ns
		5.0	–	500	750	
		10	–	200	400	
		15	–	150	300	
Write Cycle Time	$t_{cyc(W)}$					ns
		5.0	–	440	700	
		10	–	275	550	
		15	–	200	415	
Output Disable Delay	t_{dis}					ns
(10% Output Change into 1.0 kΩ Load)		5.0	–	200	600	
		10	–	80	200	
		15	–	60	150	

*The formula is for the typical characteristics only.

FIGURE 1 – READ CYCLE TIMING DIAGRAM

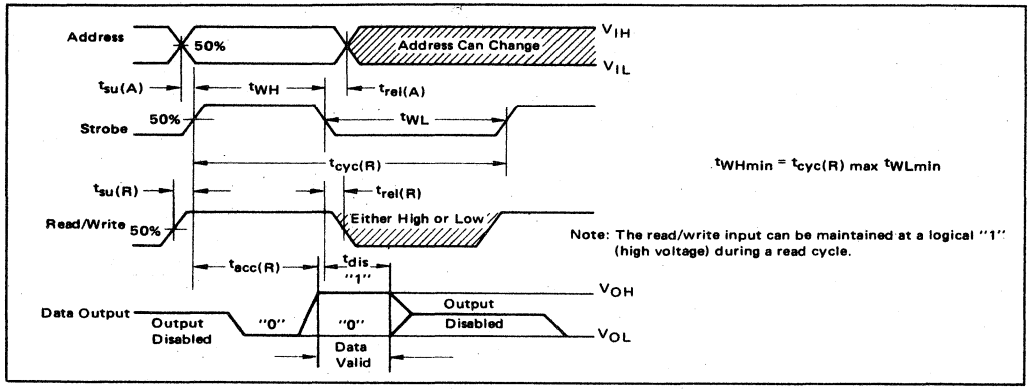


FIGURE 2 – WRITE CYCLE TIMING DIAGRAM

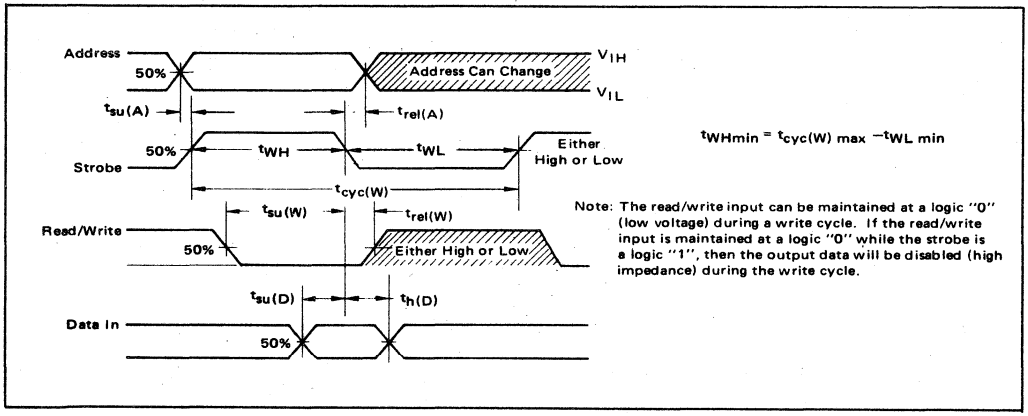


FIGURE 3 – MAXIMUM STROBE PULSE WIDTH versus TEMPERATURE

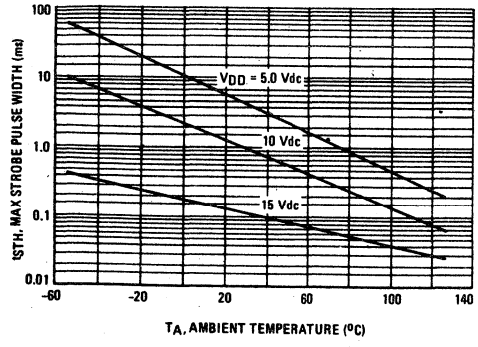


FIGURE 4 – TYPICAL READ ACCESS TIME versus LOAD CAPACITANCE

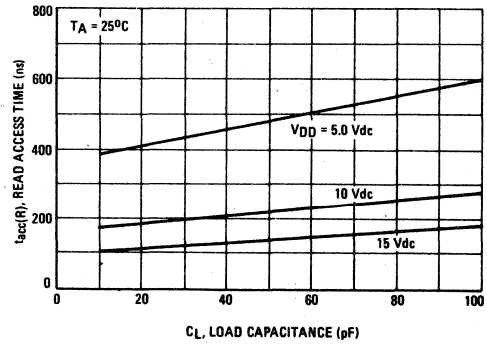
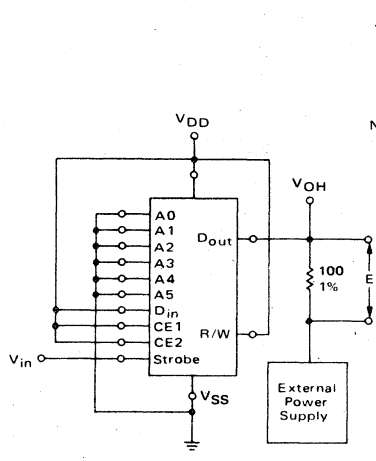
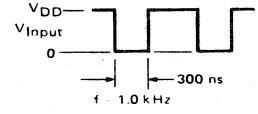


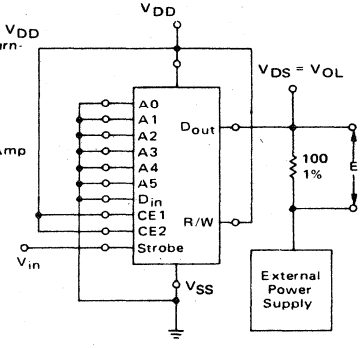
FIGURE 5 – TYPICAL OUTPUT SOURCE CAPABILITY versus TEMPERATURE

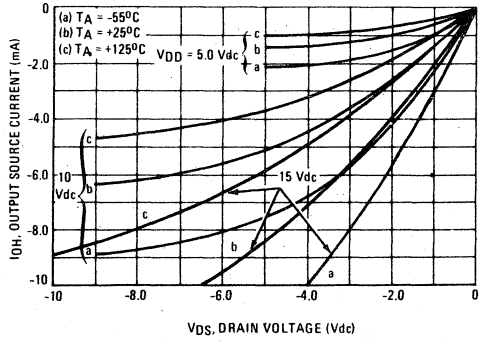




Notes:
1. Cycle R/W to ground and then to V_{DD} *prior to measurement to insure turn-on of the device under test.*
2. For the P-channel characteristics, $V_{DS} = V_{OH} - V_{DD}$.
3. For the N-channel characteristics, V_{DS} is measured directly.
4. For the drain current, $I_D = \frac{E}{100}$ Amp

FIGURE 6 – TYPICAL OUTPUT SINK CAPABILITY versus TEMPERATURE





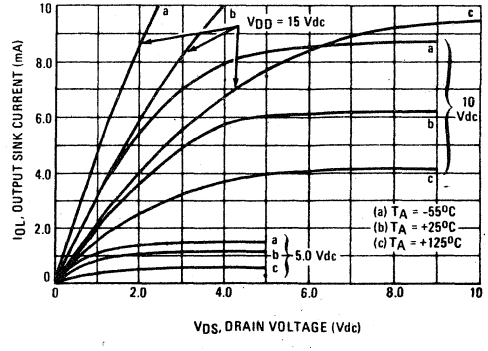
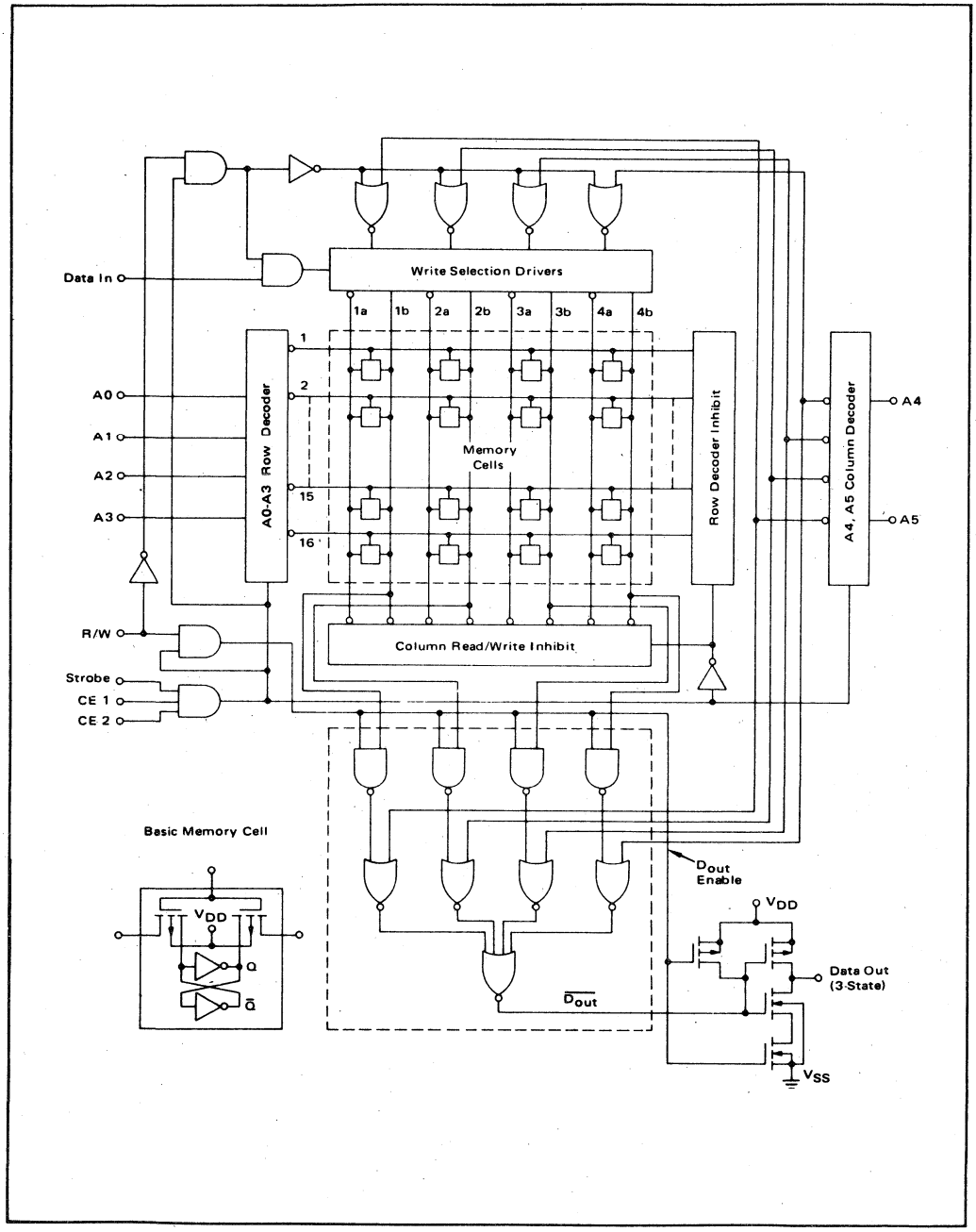


FIGURE 7 – FUNCTIONAL CIRCUIT DIAGRAM



OPERATING CHARACTERISTICS

In considering the operation of the MCM14505 CMOS memory, refer to the functional circuit diagram of Figure 7 and timing diagrams shown in Figures 1 and 2. The basic memory cell is a cross-coupled flip-flop consisting of two inverter gates and two P-channel devices for read/write control. The push-pull cell provides high speed as well as low power.

During a read cycle, when the strobe line is high the write selection drivers are disabled and the data from the selected row is available on columns 1b, 2b, 3b, and 4b. The A4 and A5 address bits are decoded to select output data from one of the four columns. The output data is available on the data output pin only when the strobe and read/write lines are high simultaneously and after the read access time, $t_{acc(R)}$, has occurred (see Figure 1). Note that the output is initially disabled and always goes to the logic "0" state (low voltage) before data is valid. The output is in the high-impedance state (disabled) when the strobe line or the R/W line is in the low state. The memory is strobed for reading or writing only when the strobe, CE1, and CE2 are high simultaneously. The R/W line can be a dc voltage during a read or write cycle and need not be pulsed, as shown in the timing diagrams. For this case the R/W line should be a logic "1" (high) for reading and a logic "0" for writing.

When the strobe line is high, the column read/write inhibit gates and the row decoder inhibit gates are disabled, the selected row is in the low state, and the unselected 15 rows retain their logic "1" level due to the row capacitance that exists when the row decoder inhibit gates are disabled. This capacitive storage mechanism requires a maximum strobe width (see Figure 3) equal to the junction reverse bias RC time constant. When the strobe is returned to a logic "0" the rows are forced to V_{DD} by the row decoder inhibit gates (pullup devices). Similarly the column read/write inhibit gates (pulldown devices) force the column lines to a logic "0" state.

Two column lines are associated with each memory cell in order to write into the cell. The write selection drivers are enabled when the R/W line is a logic "0" and the strobe line is a logic "1". The input data is written into the column selected by the column decoder. For instance, if a "1" is to be written in the memory cell associated with row 1 and column 1, then row 1 would be enabled (logic "0") while column 1b is forced high and column 1a is forced low by the write selection drivers. If a logic "0" is to be written into the cell, then column 1a is forced high and 1b is forced low. The data that is retained in the memory cell is the data that was present on the data input pin at the moment the strobe goes low when R/W is low, or when R/W goes high when the strobe is high.

APPLICATIONS INFORMATION

Figure 8 shows a 256-word by n-bit static RAM memory system The outputs of four MCM14505 devices are tied together to form 256 words by 1 bit. Additional bits are attained by paralleling the inputs in groups of four. Memories of larger words can be attained by decoding the most significant bits of the address and ANDing them with the strobe input.

Fan-in and fan-out of the memory is limited only by speed requirements. The extremely low input and output leakage current (100 nA maximum) keep the output voltage levels from changing significantly as more outputs are tied together. With the output levels independent of fan-out, most of the power supply range is available as logic swing, regardless of the number of units wired together. As a result, high noise immunity is maintained under all conditions.

Power dissipation is 0.1 μW per bit at a 1.0-kHz rate for a 5.0-volt power supply, while the static power dissipation is 2.0 nW per bit. This low power allows non-volatile information storage when the memory is powered by a small standby battery.

Figure 9 shows an optional standby power supply circuit for making a CMOS memory "non-volatile". When the usual power fails, a battery is used to sustain operation or maintain stored information. While normal power supply voltage is present, the battery is trickle-charged through a resistor which sets the charging rate. V_B is the sustaining voltage, and V^+ is the ordinary voltage from a power supply. V_{DD} connects to the power pin on the memory. Low-leakage diodes are recommended to conserve battery power.

The memory system shown in Figure 8 can be interfaced directly with the other devices in the McMOS family. No external components are required.

At the inputs to the CMOS memory, TTL devices can interface directly if an open-collector logic gate such as the MC7407 is used as shown in Figure 10. Driver circuits are not required since the input capacitance is low (4.0 to 6.0 pF). The address, data, and read/write inputs do not need to be fast since they can be changed for the duration when the strobe pulse is low, t_{STL} (see Figures 1 and 2). For high-speed operation, a push-pull driver should be used if more than five strobe inputs must be driven at one time. One circuit of the type shown in Figure 10 can be used for every ten strobe inputs.

Figures 11, 12, and 13 show methods of interfacing the memory output to TTL logic at various memory voltages. If a V_{DD} of 5.0 volts is used for slow-speed, low-power applications, one transistor and one resistor must be used (Figure 11). The MCM14505AL will drive one low-power TTL gate directly.

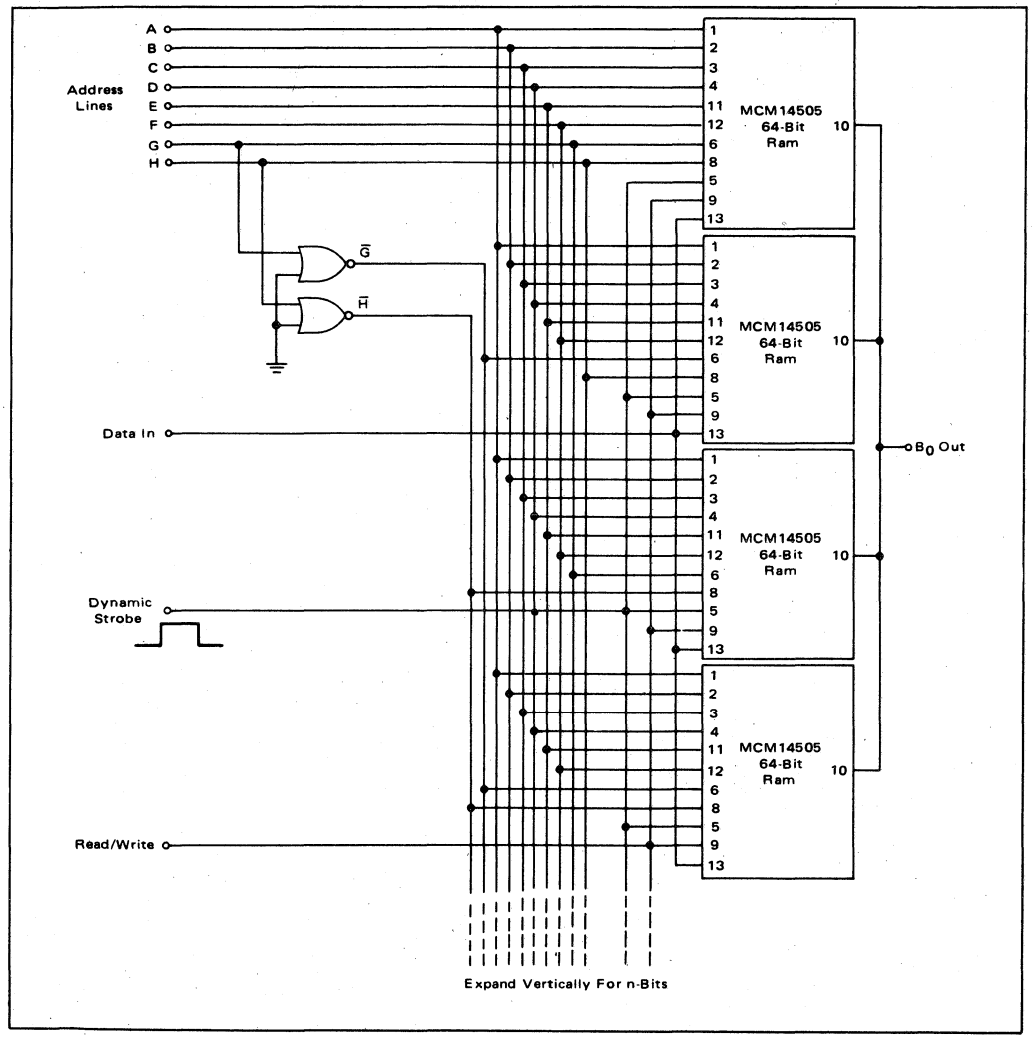
If a V_{DD} of 10 volts is used, the output of the memory device can fan out to two low-power TTL gates (Figure 12a) or to a discrete transistor (Figure 12b). The discrete transistor circuit provides higher speed and/or high fan-out. A pulldown resistor at the base of the transistor is not needed for fast turn-off because of the push-pull output of the memory. Turn-on time of the transistor is much faster in Figure 12b since the voltage rise is only 0.75 volt. The low output capacitance of the MCM14505 means that several outputs can be wire-ORed without significantly degrading performance. The read access time is increased by only 20 ns typically for 16 outputs tied together when Figure 12b is used.

Five low-power TTL gates can be driven from the memory output if a V_{DD} of 15 volts is used (Figure 13a). Figure 13b shows the interface if a discrete transistor is used. The 1.0 kilohm resistor in the base is required to insure that not more than 10 mA flows through the output as listed in the maximum ratings. If a 2.0 kilohm collector resistor is used (fan-out = 3), the turn-on time of the transistor is only slightly faster than in the circuit shown in Figure 12b due to the lower output impedance when V_{DD} = 15 volts. The voltage at the memory data output has to rise to only 1.3 volts to insure driving a fan-out of three TTL devices.

If a 510-ohm collector resistor is used, 20 TTL loads may be driven. The read access time is increased about 20 ns when four memory outputs are tied together since the output voltage must rise to 3.7 volts before the transistor can sink the full I_{OL} for a fan-out of 20 TTL devices. Almost any NPN transistor with a minimum beta of 15 can be used for the interface shown in Figures 11, 12 and 13.

The high source current from the push-pull output stage of the MCM14505 makes for a simpler interface circuit since a low source current memory requires a differential comparator to achieve high-speed operation.

FIGURE 8 – CMOS 256-WORD BY n-BIT STATIC READ/WRITE MEMORY



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

FIGURE 9 – STAND BY BATTERY CIRCUIT

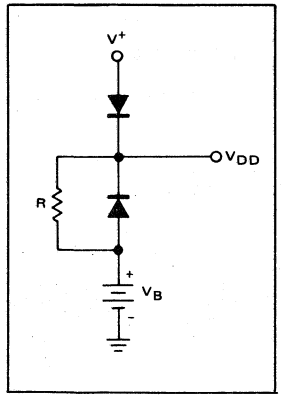


FIGURE 10 – TTL TO CMOS INTERFACE

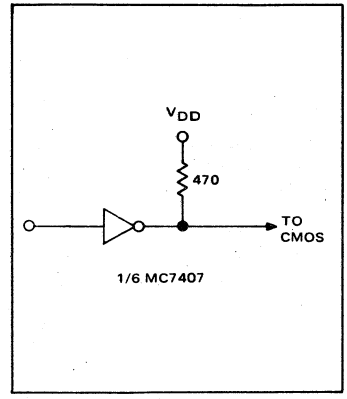


FIGURE 11 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 5.0 V

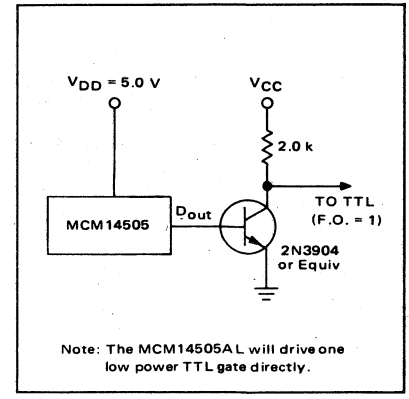


FIGURE 12 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 10 V

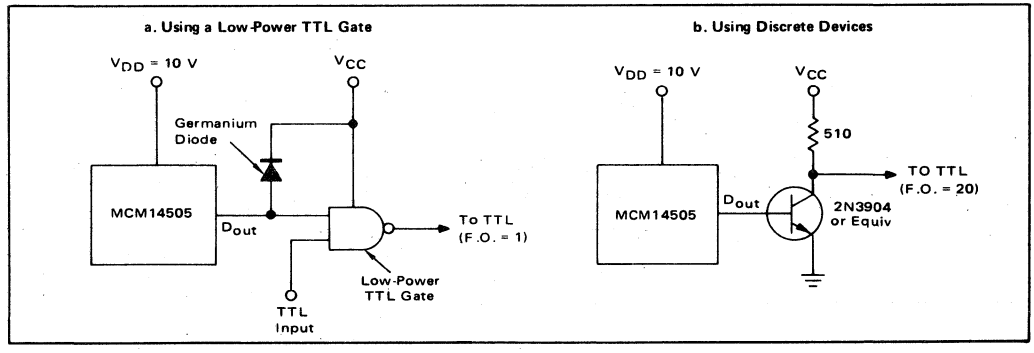
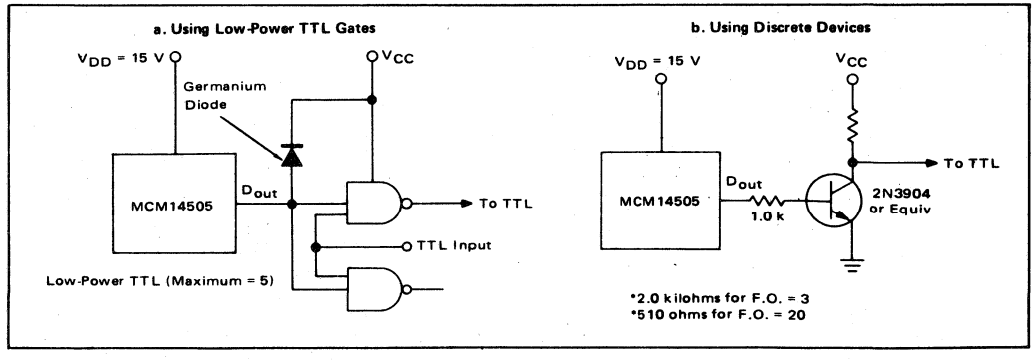


FIGURE 13 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 15 V



MOTOROLA

MC14506B

CMOS SSI

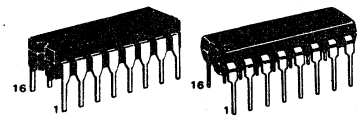
(LOW-POWER COMPLEMENTARY MOS)

DUAL EXPANDABLE AND-OR-INVERT GATE

DUAL 2-WIDE, 2-INPUT EXPANDABLE AND-OR-INVERT GATE

The MC14506B is an expandable AND-OR-INVERT gate with inhibit and 3-state output. The expand option allows cascading with any other gate, which may be carried as far as desired as long as the propagation delay added with each gate is considered. For example, the second AOI gate in this device may be used to expand the first gate, giving an expanded 4-wide, 2-input AOI gate. This device is useful in data control and digital multiplexing applications.

- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- 3-State Output
- Separate Inhibit Line
- Diode Protection on All Inputs
- Supply Voltage RAnge = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

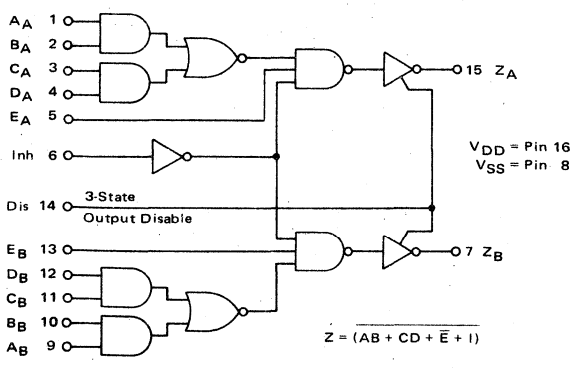
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

LOGIC DIAGRAM



TRUTH TABLE

A	B	C	D	E	INHIBIT	DISABLE	Z
0	0	0	0	1	0	0	1
0	X	0	X	1	0	0	1
0	X	X	0	1	0	0	1
X	0	0	X	1	0	0	1
X	0	X	0	1	0	0	1
1	1	X	X	X	X	0	0
X	X	1	1	X	X	0	0
X	X	X	X	0	X	0	0
X	X	X	X	X	1	0	0
X	X	X	X	X	X	1	High Impedance

X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.6 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.1 µA/kHz) f + I_{DD}							
		15	I_T = (1.7 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Data Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 210 ns		5.0	–	295	580	
t_{PLH} = (0.66 ns/pF) C_L + 77 ns		10	–	110	225	
t_{PLH} = (0.5 ns/pF) C_L + 50 ns		15	–	75	180	
t_{PHL} = (1.7 ns/pF) C_L + 185 ns	t_{PHL}	5.0	–	270	480	ns
t_{PHL} = (0.66 ns/pF) C_L + 62 ns		10	–	95	175	
t_{PHL} = (0.5 ns/pF) C_L + 40 ns		15	–	65	140	
Expand Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 95 ns		5.0	–	180	430	
t_{PLH} = (0.66 ns/pF) C_L + 42 ns		10	–	75	160	
t_{PLH} = (0.5 ns/pF) C_L + 25 ns		15	–	50	125	
t_{PHL} = (1.7 ns/pF) C_L + 115 ns	t_{PHL}	5.0	–	200	330	ns
t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	–	80	110	
t_{PHL} = (0.5 ns/pF) C_L + 30 ns		15	–	55	90	
Inhibit Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 135 ns		5.0	–	220	500	
t_{PLH} = (0.66 ns/pF) C_L + 67 ns		10	–	100	225	
t_{PLH} = (0.5 ns/pF) C_L + 40 ns		15	–	65	160	
t_{PHL} = (1.7 ns/pF) C_L + 145 ns	t_{PHL}	5.0	–	230	400	ns
t_{PHL} = (0.66 ns/pF) C_L + 62 ns		10	–	95	175	
t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	150	
3-State Propagation Delay Time						
"1" to High Impedance	t_{PHZ}	5.0	–	60	150	ns
		10	–	45	110	
		15	–	35	90	
"0" to High Impedance	t_{PLZ}	5.0	–	90	225	ns
		10	–	55	140	
		15	–	40	100	
High Impedance to "1"	t_{PZH}	5.0	–	110	300	ns
		10	–	50	125	
		15	–	40	100	
High Impedance to "0"	t_{PZL}	5.0	–	170	425	ns
		10	–	70	175	
		15	–	50	125	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

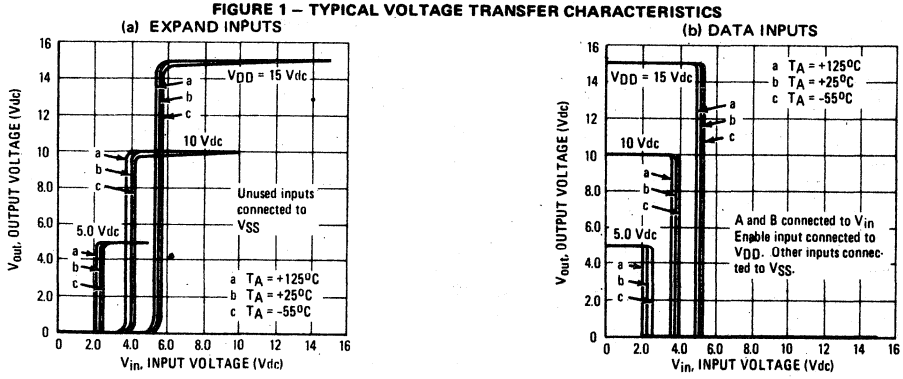


FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

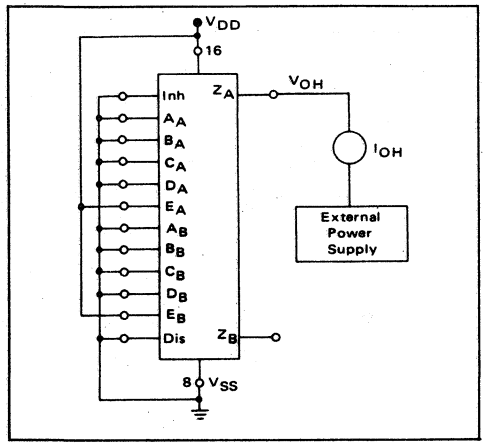


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

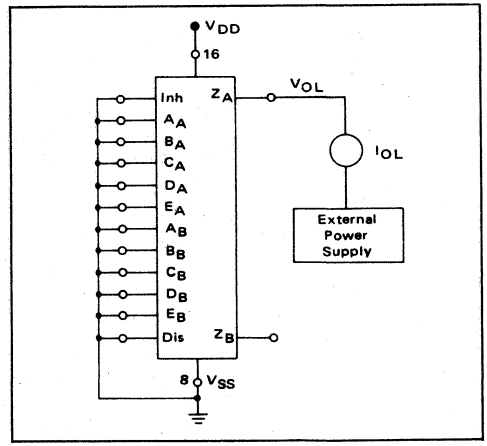


FIGURE 4 – 3-STATE LEAKAGE CURRENT TEST CIRCUIT

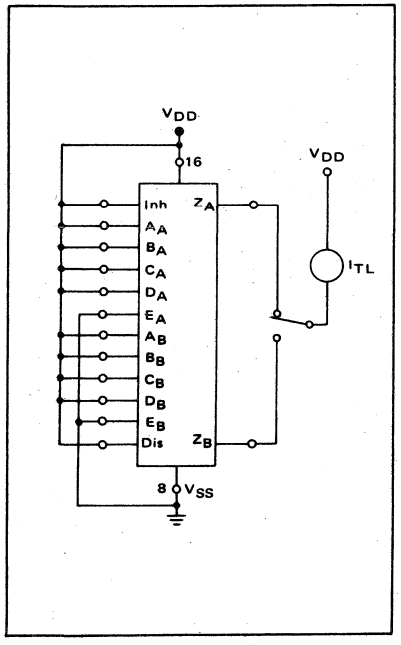


FIGURE 5 – TYPICAL POWER DISSIPATION TEST CIRCUIT

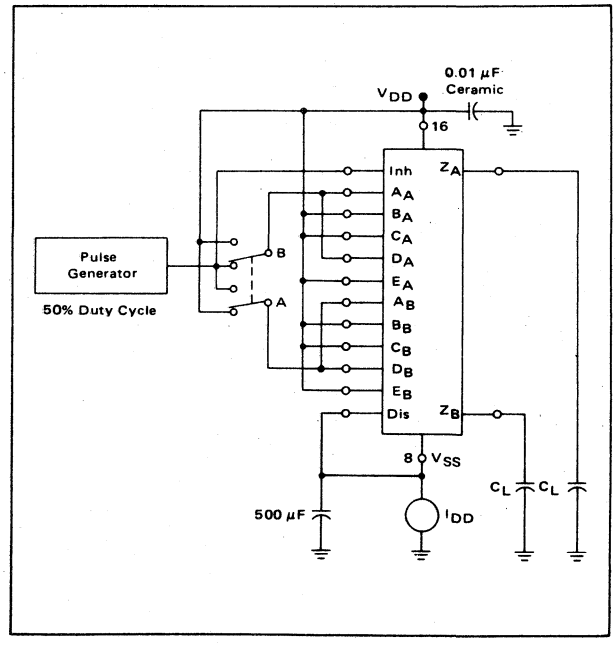


FIGURE 6 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(Data Inputs)

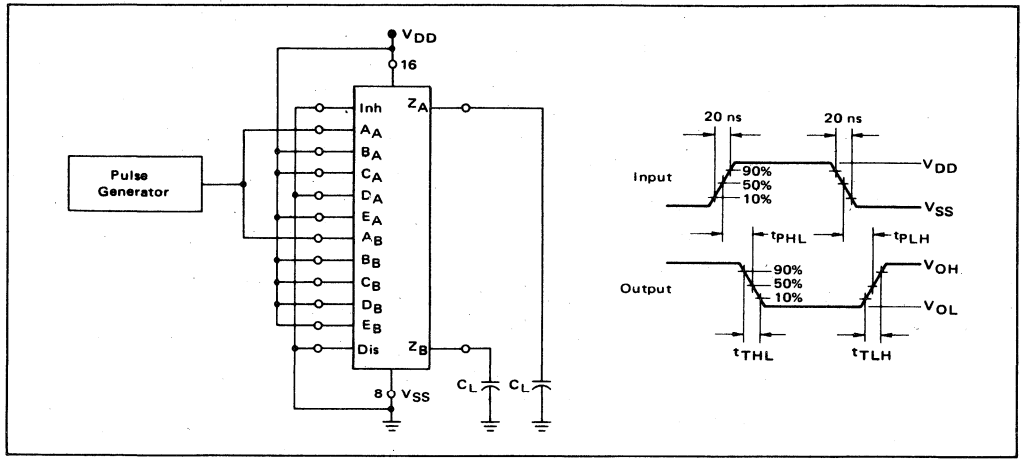
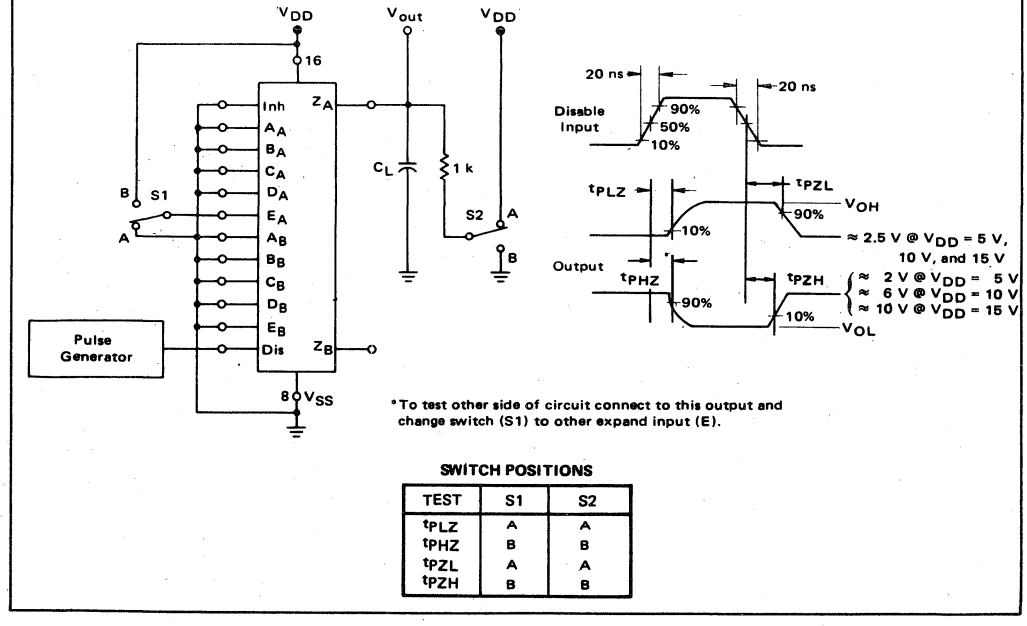


FIGURE 7 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(For 3-State Output)



*To test other side of circuit connect to this output and change switch (S1) to other expand input (E).

SWITCH POSITIONS

TEST	S1	S2
t_{PLZ}	A	A
t_{PHZ}	B	B
t_{PZL}	A	A
t_{PZH}	B	B

MOTOROLA

MC14507

QUAD EXCLUSIVE "OR" GATE

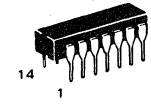
The MC14507AL/CL quad exclusive OR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

- Quiescent Power Dissipation = 6.0 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14507AL)
  3.0 Vdc to 16 Vdc (MC14507CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-For-Pin Compatible with 4030 Type

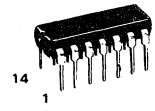
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD EXCLUSIVE "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

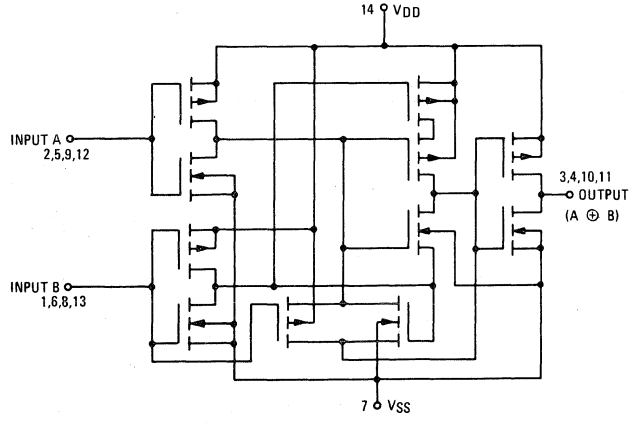
Rating		Symbol	Value	Unit
DC Supply Voltage	–MC14507AL –MC14507CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	–MC14507AL –MC14507CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

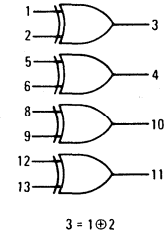
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

CIRCUIT SCHEMATIC

(1/4 OF DEVICE SHOWN, BUT ALL PIN NUMBERS INDICATED)



LOGIC DIAGRAM
POSITIVE LOGIC



3 = 1⊕2

V_{DD} = Pin 14
V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}# Min	T_{low}# Max	25°C Min	25°C Typ	25°C Max	T_{high}# Min	T_{high}# Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	–	–	0	–	–	–	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	–	–	–	15	–	–	–	
Noise Immunity	V_{NL}									Vdc
($\Delta V_{out} \leq 1.5$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 3.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 4.5$ Vdc)		15	–	–	–	6.75	–	–	–	
($\Delta V_{out} \leq 1.5$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 3.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 4.5$ Vdc)		15	–	–	–	6.75	–	–	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–	–	–	-3.5	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	–	–	–	7.8	–	–	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	–	–	–	-3.5	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	–	–	–	7.8	–	–	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q									mW
		5.0	–	0.00025	–	0.000006	0.00025	–	0.015	
		10	–	0.001	–	0.000028	0.001	–	0.06	
		15	–	–	–	0.0001		–	–	
Quiescent Dissipation (CL/CP Device)	P_Q									mW
		5.0	–	0.00025	–	0.000006	0.00025	–	0.075	
		10	–	0.001	–	0.000028	0.001	–	0.3	
		15	–	–	–	0.0001	–	–	–	
Power Dissipation *† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (0.7\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (2.8\ mW/MHz)\ f + P_Q$							
		15	$P_D = (5.0\ mW/MHz)\ f + P_Q$							

#T_{low} = -55°C for MC14507AL, -40°C for MC14507CL/CP.
T_{high} = +125°C for MC14507AL, +85°C for MC14507CL/CP.

†For dissipation at different external load capacitance (C_L) refer to corresponding formula:

$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF) V_{DD}^2 f$

where: P_T, P_D in mW (Per Gate), C_L in pF, V_{DD} in Vdc, and f in MHz.

*The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS** (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	AL Device Typ	AL Device Max	CL/CP Device Typ	CL/CP Device Max	Unit
Output Rise Time*	t_r						ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	70	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	35	110	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	25	–	25	–	
Output Fall Time*	t_f						ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	70	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	35	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	–	25	–	
Propagation Delay Time*	t_{PLH}, t_{PHL}						ns
t_{PLH}, t_{PHL} = (2.1 ns/pF) C_L + 69 ns		5.0	100	200	100	300	
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 27 ns		10	40	90	40	130	
t_{PLH}, t_{PHL} = (0.67 ns/pF) C_L + 20 ns		15	30	–	30	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

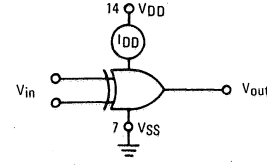


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

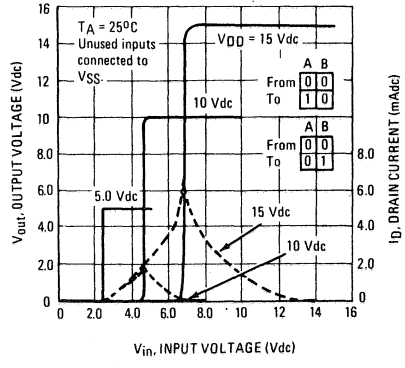


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

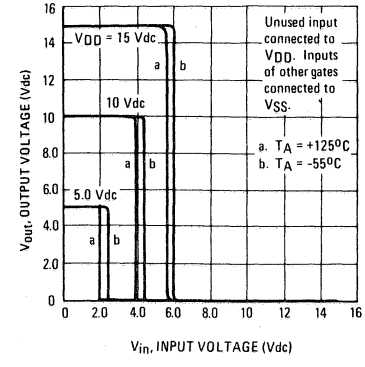


FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

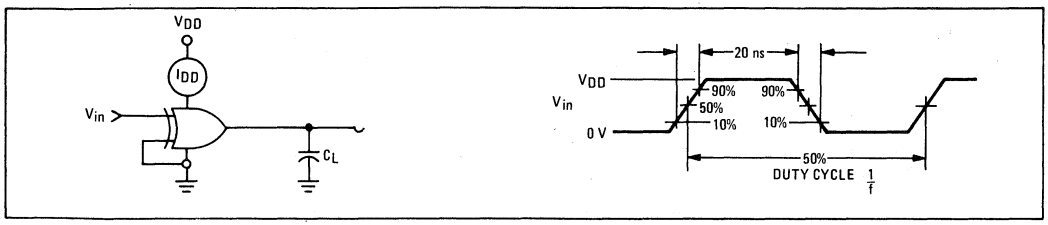
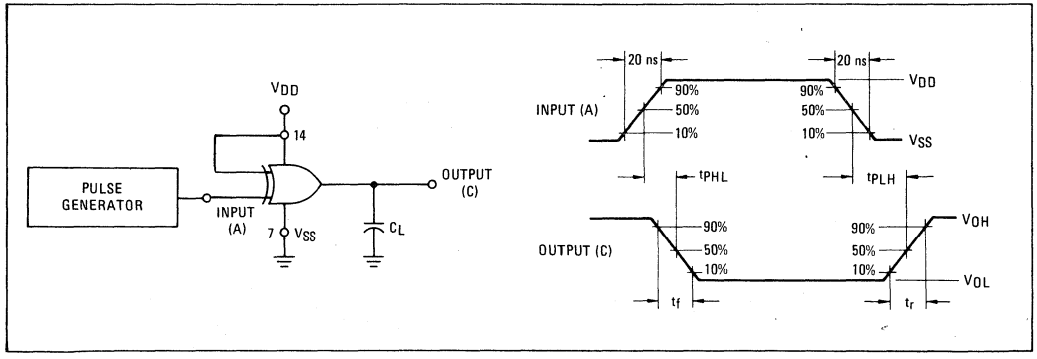


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MOTOROLA

MC14508B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

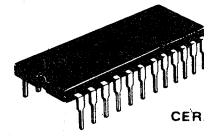
DUAL 4-BIT LATCH

DUAL 4-BIT LATCH

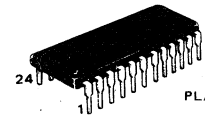
The MC14508B dual 4-bit latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The part consists of two identical, independent 4-bit latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high impedance state and allow the devices to be used in time sharing bus line applications.

These complementary MOS latches find primary use in buffer storage, holding register, or general digital logic functions where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- 3-State Output
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

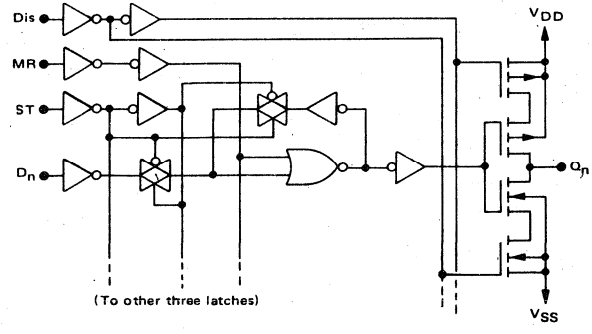
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

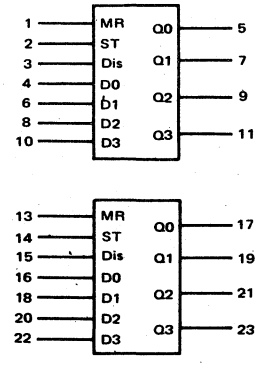
MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1	0	0	0
0	0	0	X	X	X	X	Latched			
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X	High Impedance			

X = Don't Care

CIRCUIT DIAGRAM



BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	**0.005**	5.0	–	150	µAdc
		10	–	10	–	**0.010**	10	–	300	
		15	–	20	–	**0.015**	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	**0.005**	20	–	150	µAdc
		10	–	40	–	**0.010**	40	–	300	
		15	–	80	–	**0.015**	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.46 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.91 µA/kHz) f + I_{DD}							
		15	I_T = (4.37 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 8 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Types	Max	
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Master Reset Pulse Width	$t_{WH(R)}$	5.0	200	100	–	ns
		10	100	50	–	
		15	70	35	–	
Strobe Pulse Width	$t_{WH(S)}$	5.0	140	70	–	ns
		10	70	35	–	
		15	40	20	–	
Setup Time	t_{su}	5.0	50	25	–	ns
		10	20	10	–	
		15	10	5.0	–	
Hold Time	t_h	5.0	0	0	–	ns
		10	0	0	–	
		15	0	0	–	
3-State Propagetion Delay Time	t_{PHZ}					ns
Output "1" to High Impedance						
t_{PHZ} = (0.49 ns/pF) C_L + 60.5 ns		5.0	–	85	170	
t_{PHZ} = (0.29 ns/pF) C_L + 35.5 ns		10	–	50	100	
t_{PHZ} = (0.19 ns/pF) C_L + 25.5 ns		15	–	35	70	
Output "0" to High Impedance	t_{PLZ}					ns
t_{PLZ} = 0.32 ns/pF) C_L + 49 ns		5.0	–	65	130	
t_{PLZ} = (0.29 ns/pF) C_L + 25.5 ns		10	–	40	80	
t_{PLZ} = (0.28 ns/pF) C_L + 16 ns		15	–	30	60	
High Impedance to "1" Level	t_{PZH}					ns
t_{PZH} = (0.41 ns/pF) C_L + 64.5 ns		5.0	–	85	170	
t_{PZH} = (0.31 ns/pF) C_L + 34.5 ns		10	–	50	100	
t_{PZH} = (0.30 ns/pF) C_L + 20 ns		15	–	35	70	
High Impedance to "0" Level	t_{PZL}					ns
t_{PZL} = (0.49 ns/pF) C_L + 60.5 ns		5.0	–	85	170	
t_{PZL} = (0.29 ns/pF) C_L + 35.5 ns		10	–	50	100	
t_{PZL} = (0.19 ns/pF) C_L + 25.5 ns		15	–	35	70	

*The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – AC WAVEFORMS

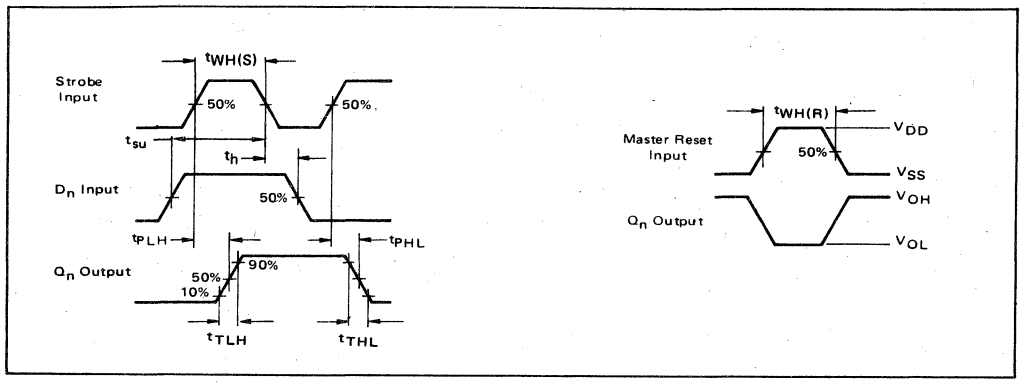
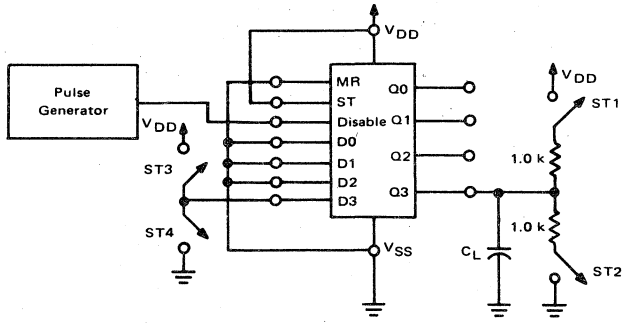
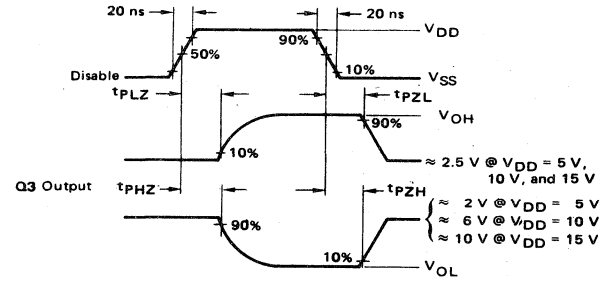


FIGURE 2 – 3-STATE AC TEST CIRCUIT AND WAVEFORMS



TEST	ST1	ST2	ST3	ST4
t_{PHZ}	OPEN	CLOSE	CLOSE	OPEN
t_{PLZ}	CLOSE	OPEN	OPEN	CLOSE
t_{PZL}	CLOSE	OPEN	OPEN	CLOSE
t_{PZH}	OPEN	CLOSE	CLOSE	OPEN

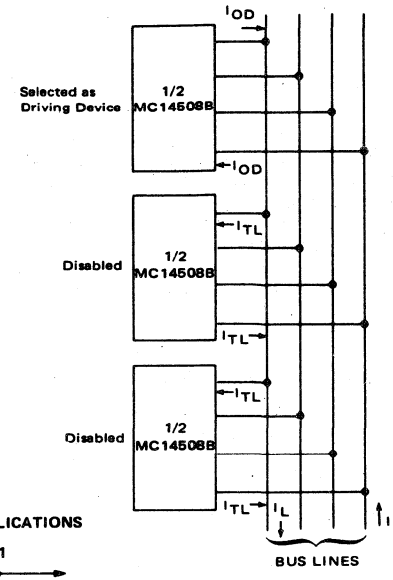


3-STATE MODE OF OPERATION

The MC14508B can be used in bussed systems as shown. The output terminals of N 4-bit latches can be directly wired to a bus line, and to one of the 4-bit latches selected. The selected latch controls the logic state of the bus line, and the remaining (N-1) 4-bit latches are disabled into a high impedance "off" state. The number of latches, N, which may be connected to a bus line is determined from the output drive current, I_{OD}, the 3-state or disabled output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs) and can be calculated by the following:

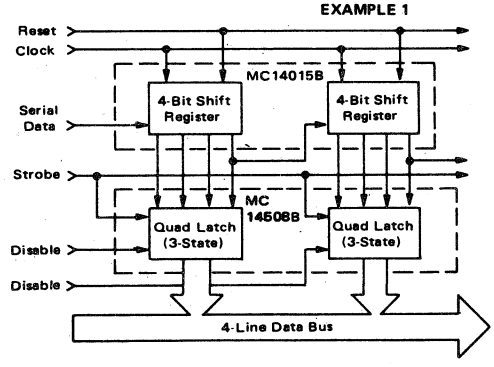
$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the bus line.

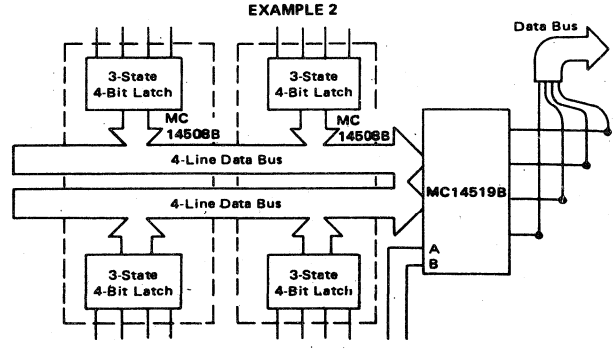


TYPICAL 3–STATE APPLICATIONS

EXAMPLE 1



EXAMPLE 2



MOTOROLA

MC14510B

BCD UP/DOWN COUNTER

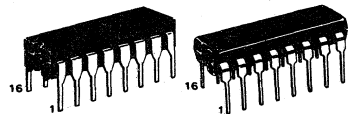
The MC14510B BCD up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide type T flip-flop capability. The counter can be cleared by applying a high level on the Reset line. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Quiescent Current = 5.0 nA/package typical @ 5.0 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance — 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design — Count Occurs on Positive Going Edge of Clock
- 5.0-MHz Counting Rate
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD UP/DOWN COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

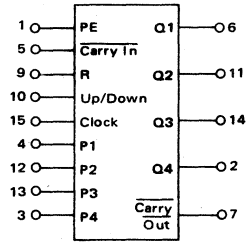
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L +15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Clock to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns		5.0	–	180	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	–	80	160	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Preset or Reset to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Preset or Reset ot $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
Clock Pulse Width	t_{WH}	5.0	350	200	–	ns
		10	170	100	–	
		15	140	75	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Preset or Reset Removal Time**	t_{rem}	5.0	650	325	–	ns
		10	230	115	–	
		15	180	90	–	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
$\overline{\text{Carry In}}$ Setup Time	t_{su}	5.0	200	130	–	ns
		10	120	60	–	
		15	100	50	–	
Up/Down Setup Time	t_{su}	5.0	500	250	–	ns
		10	200	100	–	
		15	175	75	–	
Preset Enable Pulse Width	t_{WH}	5.0	200	100	–	ns
		10	100	50	–	
		15	80	40	–	

*The formula given is for the typical characteristics only.

**The Preset or Reset Signal must be low prior to a positive-going transition of the clock.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

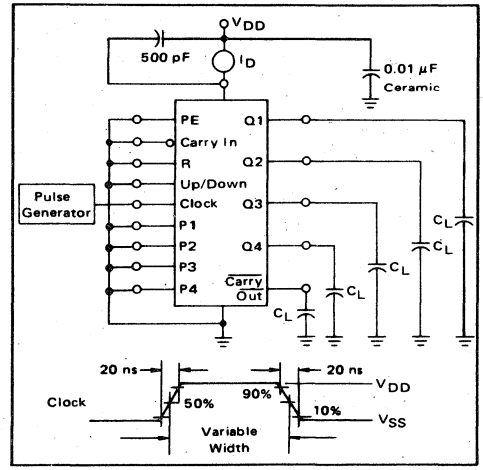
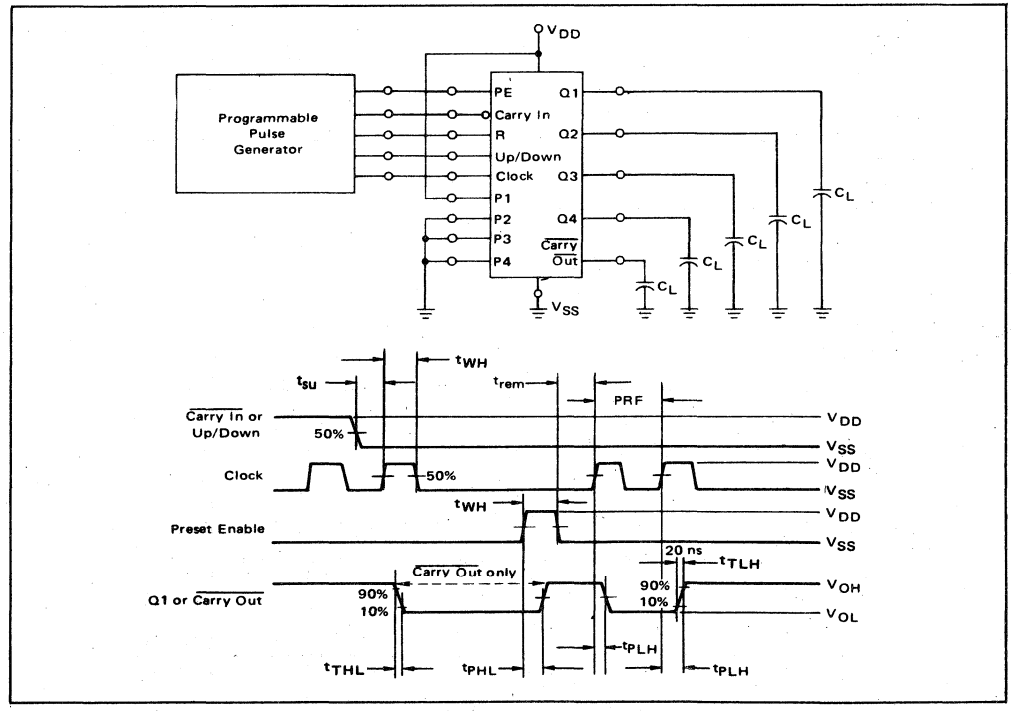
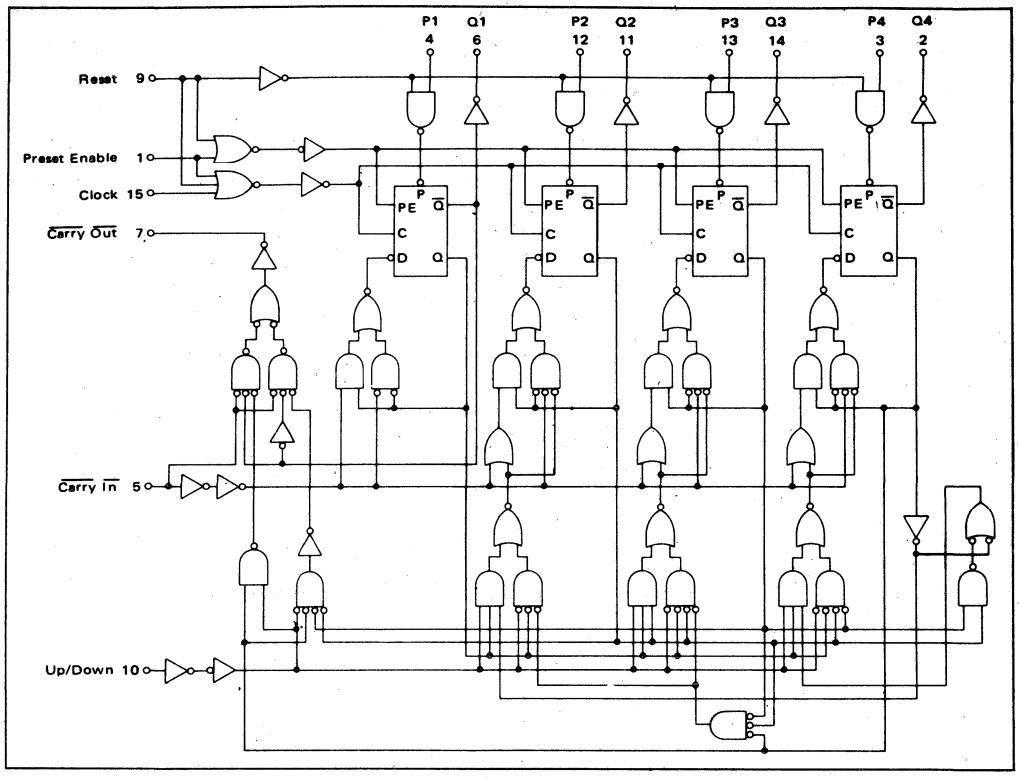


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAM



TIMING DIAGRAM

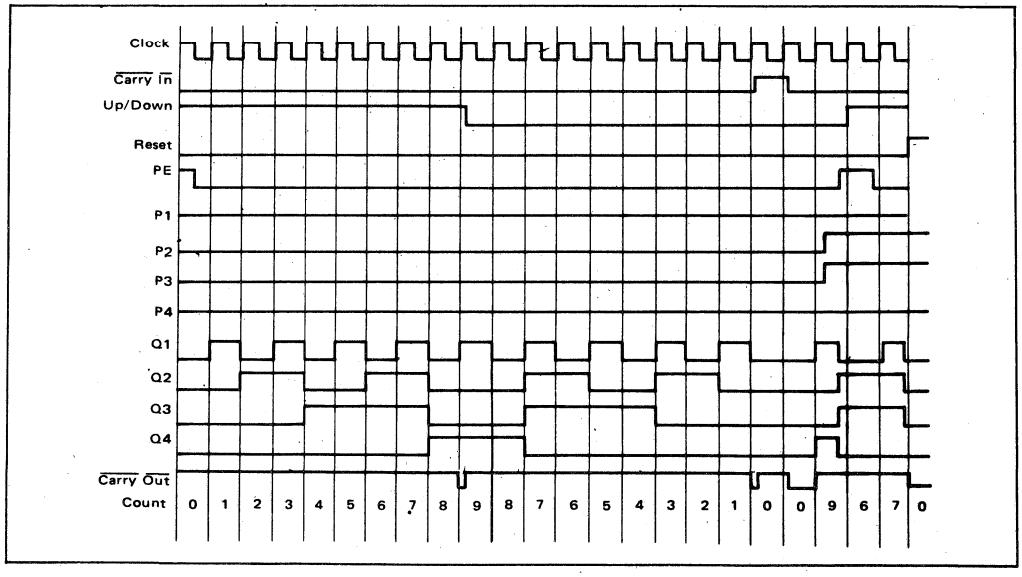


FIGURE 3 – PRESETTABLE CASCADED UP/DOWN COUNTER

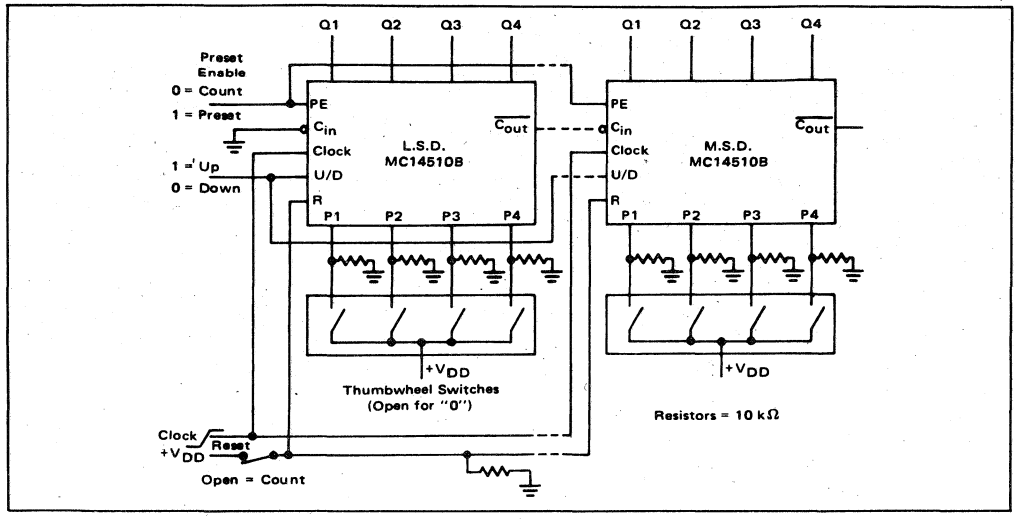
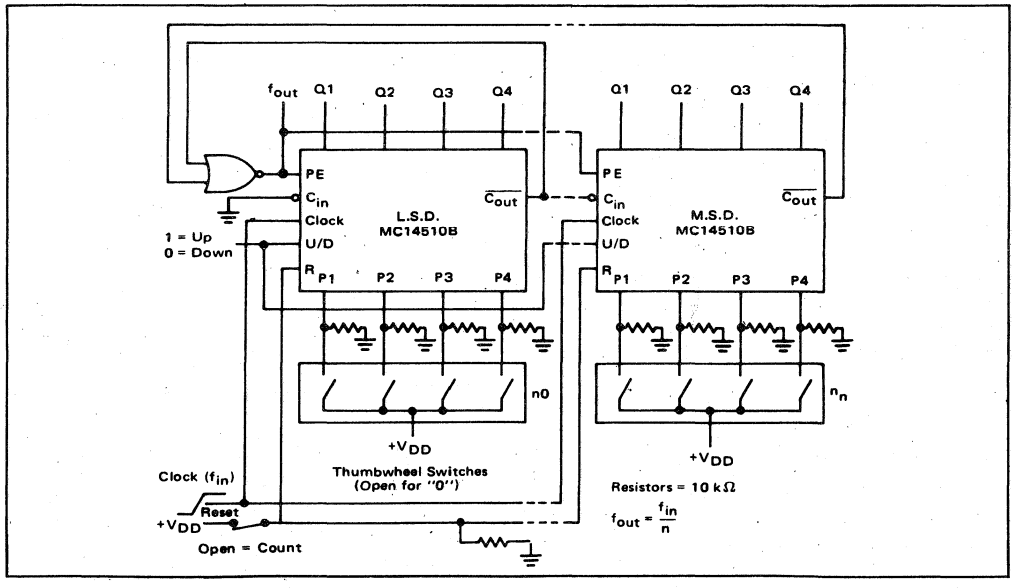


FIGURE 4 – PROGRAMMABLE CASCADED FREQUENCY DIVIDER



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14511B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14511B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

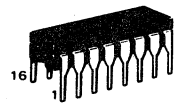
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

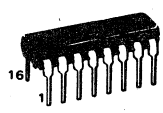
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER



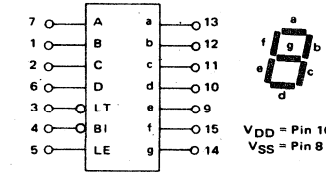
L SUFFIX
CERAMIC PACKAGE
CASE 620



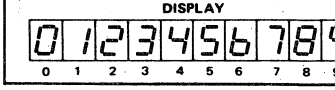
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



DISPLAY



MAXIMUM RATINGS (Voltages referenced to V_{SS}).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	
Maximum Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output ‡	P_{OHmax}	50	mW

‡ $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occure if V_{in} and V_{out} is not constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				*				*

X = Don't Care
*Depends upon the BCD code previously applied when LE = 0

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.1	–	4.1	4.57	–	4.1	–	Vdc
V_{in} = 0 or V_{DD}		10	9.1	–	9.1	9.58	–	9.1	–	
		15	14.1	–	14.1	14.59	–	14.1	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.8 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 8.8 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.8 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
(V_O = 0.5 or 3.8 Vdc) "1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 8.8 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.8 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Voltage (AL Device)	V_{OH}									Vdc
(I_{OH} = 0 mAdc) Source		5.0	4.10	–	4.10	4.57	–	4.1	–	
(I_{OH} = 5.0 mAdc)			–	–	–	4.24	–	–	–	
(I_{OH} = 10 mAdc)			3.90	–	3.90	4.12	–	3.5	–	
(I_{OH} = 15 mAdc)			–	–	–	3.94	–	–	–	
(I_{OH} = 20 mAdc)			3.40	–	3.40	3.75	–	3.0	–	
(I_{OH} = 25 mAdc)			–	–	–	3.54	–	–	–	
(I_{OH} = 0 mAdc)		10	9.10	–	9.10	9.58	–	9.1	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	9.26	–	–	–	
(I_{OH} = 10 mAdc)			9.00	–	9.00	9.17	–	8.6	–	
(I_{OH} = 15 mAdc)			–	–	–	9.04	–	–	–	
(I_{OH} = 20 mAdc)			8.60	–	8.60	8.90	–	8.2	–	
(I_{OH} = 25 mAdc)			–	–	–	8.75	–	–	–	
(I_{OH} = 0 mAdc)		15	14.1	–	14.1	14.59	–	14.1	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	14.27	–	–	–	
(I_{OH} = 10 mAdc)			14.0	–	14.0	14.18	–	13.6	–	
(I_{OH} = 15 mAdc)			–	–	–	14.07	–	–	–	
(I_{OH} = 20 mAdc)			13.6	–	13.6	13.95	–	13.2	–	
(I_{OH} = 25 mAdc)			–	–	–	13.80	–	–	–	
Output Drive Voltage (CL/CP Device)	V_{OH}									Vdc
(I_{OH} = 0 mAdc) Source		5.0	4.10	–	4.10	4.57	–	4.1	–	
(I_{OH} = 5.0 mAdc)			–	–	–	4.24	–	–	–	
(I_{OH} = 10 mAdc)			3.60	–	3.60	4.12	–	3.3	–	
(I_{OH} = 15 mAdc)			–	–	–	3.94	–	–	–	
(I_{OH} = 20 mAdc)			2.80	–	2.80	3.75	–	2.5	–	
(I_{OH} = 25 mAdc)			–	–	–	3.54	–	–	–	
(I_{OH} = 0 mAdc)		10	9.10	–	9.10	9.58	–	9.1	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	9.26	–	–	–	
(I_{OH} = 10 mAdc)			8.75	–	8.75	9.17	–	8.45	–	
(I_{OH} = 15 mAdc)			–	–	–	9.04	–	–	–	
(I_{OH} = 20 mAdc)			8.10	–	8.10	8.90	–	7.8	–	
(I_{OH} = 25 mAdc)			–	–	–	8.75	–	–	–	
(I_{OH} = 0 mAdc)		15	14.1	–	14.1	14.59	–	14.1	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	14.27	–	–	–	
(I_{OH} = 10 mAdc)			13.75	–	13.75	14.18	–	13.45	–	
(I_{OH} = 15 mAdc)			–	–	–	14.07	–	–	–	
(I_{OH} = 20 mAdc)			13.1	–	13.1	13.95	–	12.8	–	
(I_{OH} = 25 mAdc)			–	–	–	13.80	–	–	–	
Output Drive Current (AL Device)	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	

(Continued)

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.9 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.8 μA/kHz) f + I_{DD}							
		15	I_T = (5.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.5 ns/pF) C_L + 50 ns		5.0	–	40	80	
t_{TLH} = (0.75 ns/pF) C_L + 37.5 ns		10	–	30	60	
t_{TLH} = (0.55 ns/pF) C_L + 37.5 ns		15	–	25	50	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 50 ns		5.0	–	125	250	
t_{THL} = (0.75 ns/pF) C_L + 37.5 ns		10	–	75	150	
t_{THL} = (0.55 ns/pF) C_L + 37.5 ns		15	–	65	130	
Data Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.40 ns/pF) C_L + 620 ns		5.0	–	640	1280	
t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns		10	–	250	500	
t_{PLH} = (0.20 ns/pF) C_L + 165 ns		15	–	175	350	
t_{PHL} = (1.3 ns/pF) C_L + 655 ns	t_{PHL}	5.0	–	720	1440	ns
t_{PHL} = (0.60 ns/pF) C_L + 260 ns		10	–	290	580	
t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns		15	–	200	400	
Blank Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.30 ns/pF) C_L + 305 ns		5.0	–	600	750	
t_{PLH} = (0.25 ns/pF) C_L + 117.5 ns		10	–	200	300	
t_{PLH} = (0.15 ns/pF) C_L + 92.5 ns		15	–	150	220	
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns	t_{PHL}	5.0	–	485	970	ns
t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns		10	–	200	400	
t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns		15	–	160	320	
Lamp Test Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns		5.0	–	313	625	
t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns		10	–	125	250	
t_{PLH} = (0.20 ns/pF) C_L + 80 ns		15	–	90	180	
t_{PHL} = (1.3 ns/pF) C_L + 248 ns	t_{PHL}	5.0	–	313	625	ns
t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns		10	–	125	250	
t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns		15	–	90	180	
Setup Time	t_{su}	5.0	180	90	–	ns
		10	76	38	–	
		15	40	20	–	
Hold Time	t_h	5.0	0	-90	–	ns
		10	0	-38	–	
		15	0	-20	–	
Latch Enable Pulse Width	t_{WL}	5.0	520	260	–	ns
		10	220	110	–	
		15	130	65	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

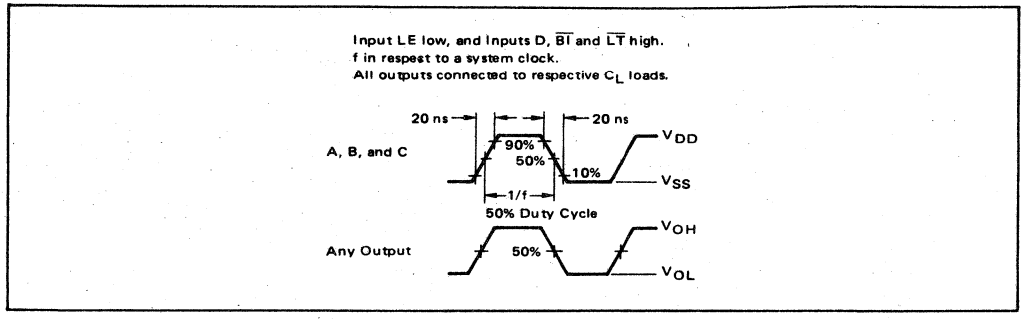
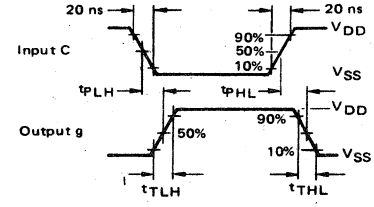
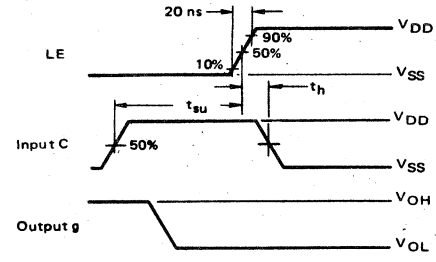


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS

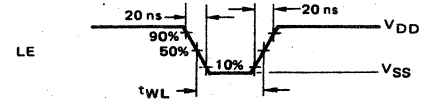
(a) Inputs D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



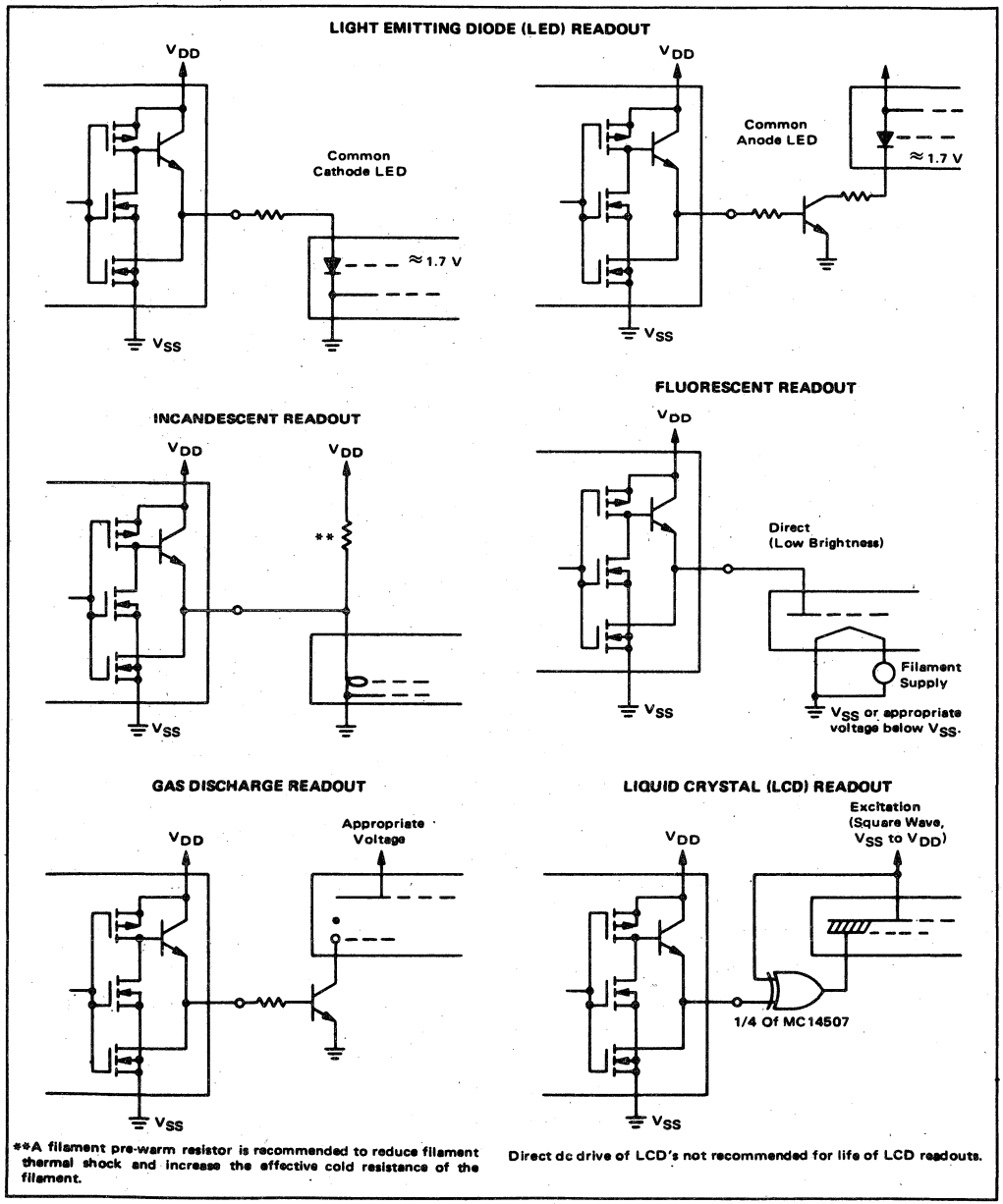
(b) Input D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



(c) Data DCBA strobed into latches.



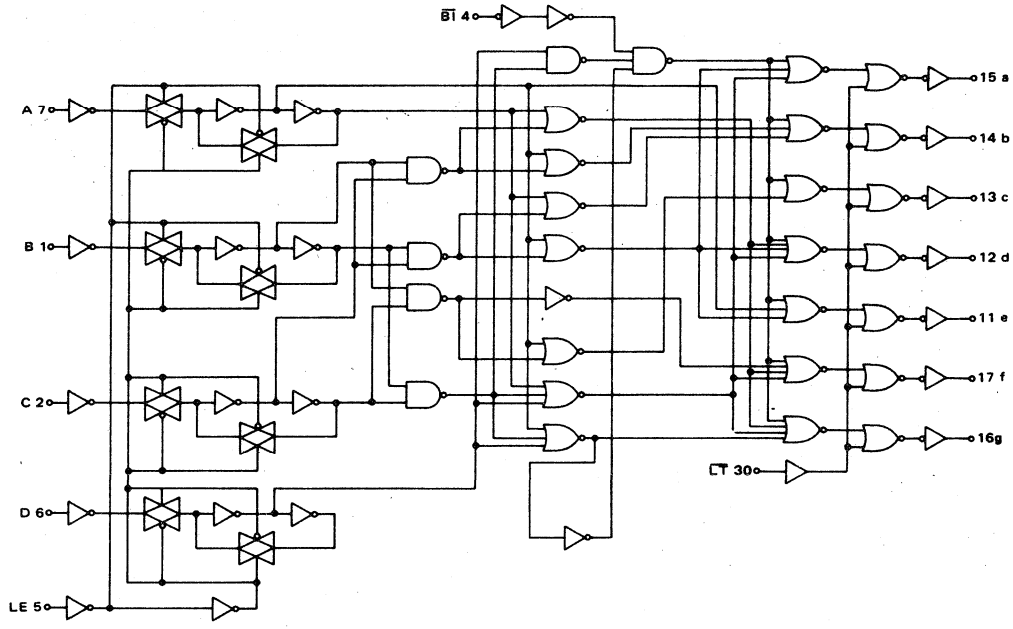
CONNECTIONS TO VARIOUS DISPLAY READOUTS



**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LCD's not recommended for life of LCD readouts.

LOGIC DIAGRAM



MOTOROLA

MC14512B

8-CHANNEL DATA SELECTOR

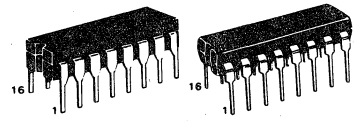
The MC14512B is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- High Fanout > 50
- Single Supply Operation – Positive or Negative
- 3-State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-CHANNEL DATA SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

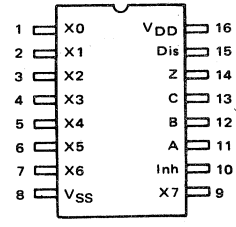
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
φ	φ	φ	1	0	0
φ	φ	φ	φ	1	High Impedance

φ = Don't Care

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.8\ \mu A/kHz)f + I_{DD}$							µAdc
		10	$I_T = (1.6\ \mu A/kHz)f + I_{DD}$							
		15	$I_T = (2.4\ \mu A/kHz)f + I_{DD}$							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3}(C_L - 50)\ V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types		Unit
			Typ	Max	
Output Rise Time	t_{TLH}				ns
t_{TLH} = (3.0 ns/pF) C_L + 25 ns		5.0	225	360	
t_{TLH} = (1.5 ns/pF) C_L + 12 ns		10	110	180	
t_{TLH} = (1.1 ns/pF) C_L + 8 ns		15	80	130	
Output Fall Time	t_{THL}				ns
t_{THL} = (1.5 ns/pF) C_L + 47 ns		5.0	130	200	
t_{THL} = (0.75 ns/pF) C_L + 24 ns		10	65	100	
t_{THL} = (0.55 ns/pF) C_L + 17 ns		15	50	80	
Turn-Off Delay Time	t_{PLH}				ns
t_{PLH} = (0.9 ns/pF) C_L + 211 ns		5.0	330	650	
t_{PLH} = (0.3 ns/pF) C_L + 70 ns		10	125	250	
t_{PLH} = (0.23 ns/pF) C_L + 54 ns		15	85	170	
Turn-On Delay Time	t_{PHL}				ns
t_{PHL} = (2.7 ns/pF) C_L + 184 ns		5.0	330	650	
t_{PHL} = (0.9 ns/pF C_L + 61 ns		10	125	250	
t_{PHL} = (0.68 ns/pF) C_L + 47 ns		15	85	170	
3-State Output Delay Times	t_{PHZ}, t_{PLZ},	5.0	60	150	ns
"1" or "0" to High Z, and	t_{PZH}, t_{PZL}	10	35	100	
High Z to "1" or "0"		15	30	75	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

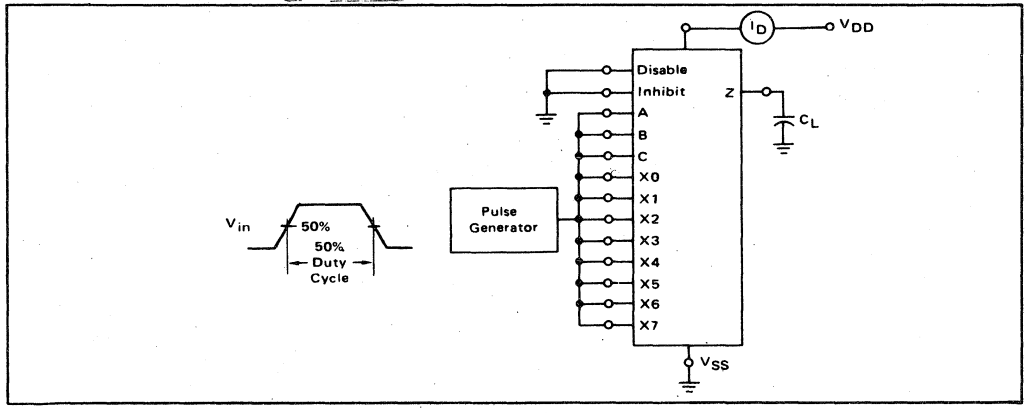


FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS

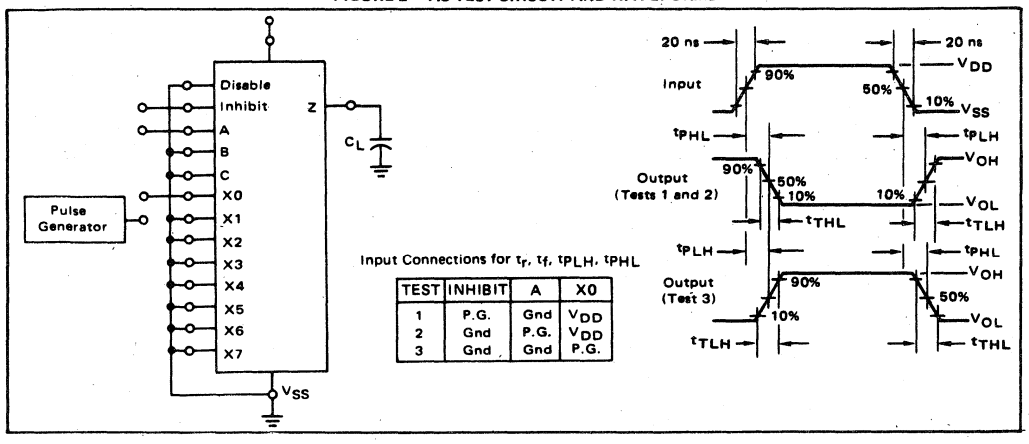
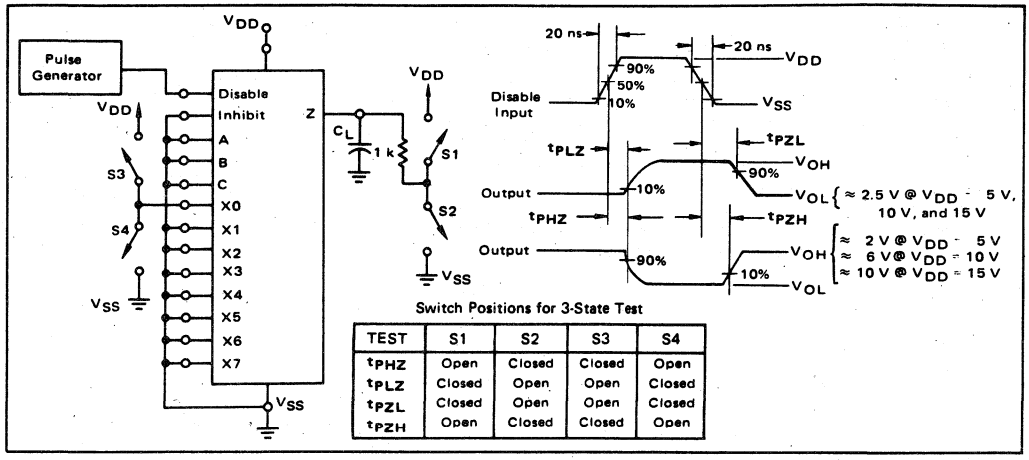


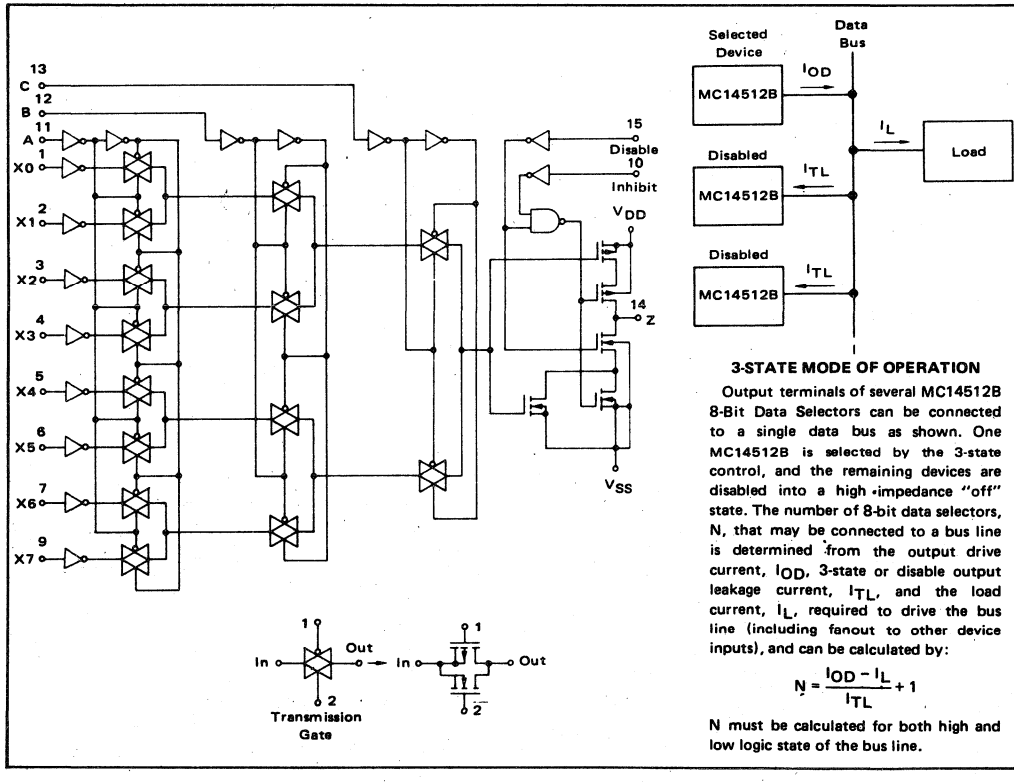
FIGURE 3 – 3-STATE AC TEST CIRCUIT AND WAVEFORM



Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

LOGIC DIAGRAM



3-STATE MODE OF OPERATION

Output terminals of several MC14512B 8-Bit Data Selectors can be connected to a single data bus as shown. One MC14512B is selected by the 3-state control, and the remaining devices are disabled into a high-impedance "off" state. The number of 8-bit data selectors, N, that may be connected to a bus line is determined from the output drive current, I_{OD}, 3-state or disable output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs), and can be calculated by:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic state of the bus line.

MOTOROLA

MC14513B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14513B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. The Ripple Blanking Input (RBI) and Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Logic Circuit Power Dissipation
- High-current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Binary Input
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Capability
- Adds Ripple Blanking In, Ripple Blanking Out to MC14511B
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	
Maximum Continuous Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output ‡	P_{OHmax}	50	mW

‡ $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} is not constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

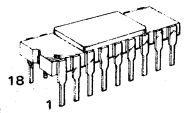
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (see Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

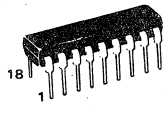
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER WITH RIPPLE BLANKING



L SUFFIX
CERAMIC PACKAGE
CASE 680

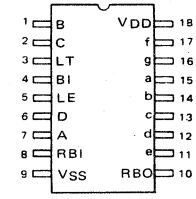


P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT





DISPLAY



TRUTH TABLE

INPUTS								OUTPUTS								
RBI	LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	RBO	a	b	c	d	e	f	g	DISPLAY
X	X	X	0	X	X	X	X	≠	1	1	1	1	1	1	1	8
X	X	0	1	X	X	X	X	≠	0	0	0	0	0	0	0	Blank
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	0	1	1	0	0	0	0	0	1	1	1	1	1	1	0	0
X	0	1	1	0	0	0	1	0	0	1	1	0	0	0	0	1
X	0	1	1	0	0	1	0	0	1	1	0	1	1	0	1	2
X	0	1	1	0	0	1	1	0	1	1	1	1	0	0	1	3
X	0	1	1	0	1	0	0	0	0	1	1	0	0	1	1	4
X	0	1	1	0	1	0	1	0	1	0	1	1	0	1	1	5
X	0	1	1	0	1	1	0	0	1	0	1	1	1	1	1	6
X	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	7
X	0	1	1	1	0	0	0	0	1	1	1	1	1	1	1	8
X	0	1	1	1	0	0	1	0	1	1	1	1	0	1	1	9
X	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	1	1	1	X	X	X	X	≠				*				*

X Don't Care
≠ RBO = RBI ($\overline{BCBA}$), indicated by other rows of table.
* Depends upon the BCD code previously applied when LE = 0.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage — Segment Outputs	V_{OL}									Vdc
"0" Level		5.0	–	0.05	–	0	0.05	–	0.05	
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.1	–	4.1	5.0	–	4.1	–	Vdc
V_{in} = 0 or V_{DD}		10	9.1	–	9.1	10	–	9.1	–	
		15	14.1	–	14.1	15	–	14.1	–	
Output Voltage — RBO Output	V_{OL}									Vdc
"0" Level		5.0	–	0.05	–	0	0.05	–	0.05	
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.8 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 8.8 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.8 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
(V_O = 0.5 or 3.8 Vdc) "1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 8.8 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.8 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Voltage — Segments (AL Device)	V_{OH}									Vdc
(I_{OH} = 0 mAdc) Source:		5.0	4.10	–	4.10	4.57	–	4.1	–	
(I_{OH} = 5.0 mAdc)			–	–	–	4.24	–	–	–	
(I_{OH} = 10 mAdc)			3.90	–	3.90	4.12	–	3.5	–	
(I_{OH} = 15 mAdc)			–	–	–	3.94	–	–	–	
(I_{OH} = 20 mAdc)			3.40	–	3.40	3.75	–	3.0	–	
(I_{OH} = 25 mAdc)			–	–	–	3.54	–	–	–	
(I_{OH} = 0 mAdc)		10	9.10	–	9.10	9.58	–	9.1	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	9.26	–	–	–	
(I_{OH} = 10 mAdc)			9.00	–	9.00	9.17	–	8.6	–	
(I_{OH} = 15 mAdc)			–	–	–	9.04	–	–	–	
(I_{OH} = 20 mAdc)			8.60	–	8.60	8.90	–	8.2	–	
(I_{OH} = 25 mAdc)			–	–	–	8.75	–	–	–	
(I_{OH} = 0 mAdc)		15	14.1	–	14.1	14.59	–	14.1	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	14.27	–	–	–	
(I_{OH} = 10 mAdc)			14.0	–	14.0	14.18	–	13.6	–	
(I_{OH} = 15 mAdc)			–	–	–	14.07	–	–	–	
(I_{OH} = 20 mAdc)			13.6	–	13.6	13.95	–	13.2	–	
(I_{OH} = 25 mAdc)			–	–	–	13.80	–	–	–	
Output Drive Voltage — Segments (CL/CP Device)	V_{OH}									Vdc
(I_{OH} = 0 mAdc) Source:		5.0	4.10	–	4.10	4.57	–	4.1	–	
(I_{OH} = 5.0 mAdc)			–	–	–	4.24	–	–	–	
(I_{OH} = 10 mAdc)			3.60	–	3.60	4.12	–	3.3	–	
(I_{OH} = 15 mAdc)			–	–	–	3.94	–	–	–	
(I_{OH} = 20 mAdc)			2.80	–	2.80	3.75	–	2.5	–	
(I_{OH} = 25 mAdc)			–	–	–	3.54	–	–	–	
(I_{OH} = 0 mAdc)		10	9.10	–	9.10	9.58	–	9.1	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	9.26	–	–	–	
(I_{OH} = 10 mAdc)			8.75	–	8.75	9.17	–	8.45	–	
(I_{OH} = 15 mAdc)			–	–	–	9.04	–	–	–	
(I_{OH} = 20 mAdc)			8.10	–	8.10	8.90	–	7.8	–	
(I_{OH} = 25 mAdc)			–	–	–	8.75	–	–	–	
(I_{OH} = 0 mAdc)		15	14.1	–	14.1	14.59	–	14.1	–	Vdc
(I_{OH} = 5.0 mAdc)			–	–	–	14.27	–	–	–	
(I_{OH} = 10 mAdc)			13.75	–	13.75	14.18	–	13.45	–	
(I_{OH} = 15 mAdc)			–	–	–	14.07	–	–	–	
(I_{OH} = 20 mAdc)			13.1	–	13.1	13.95	–	12.8	–	
(I_{OH} = 25 mAdc)			–	–	–	13.80	–	–	–	

ELECTRICAL CHARACTERISTICS (Continued)

	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Drive Current — RBO Output (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.40	–	-0.32	-0.64	–	-0.22	–	
(V_{OH} = 9.5 Vdc)		10	-0.21	–	-0.17	-0.34	–	-0.12	–	
(V_{OH} = 13.5 Vdc)		15	-0.81	–	-0.66	-1.3	–	-0.46	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.18	–	0.15	0.29	–	0.10	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.47	–	0.38	0.75	–	0.26	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	2.9	–	1.0	–	
Output Drive Current — RBO Output (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.25	–	-0.21	-0.64	–	-0.17	–	
(V_{OH} = 9.5 Vdc)		10	-0.13	–	-0.11	-0.34	–	-0.092	–	
(V_{OH} = 13.5 Vdc)		15	-0.52	–	-0.44	-1.3	–	-0.36	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.12	–	0.098	0.29	–	0.080	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.30	–	0.25	0.75	–	0.21	–	
(V_{OL} = 1.5 Vdc)		15	1.2	–	0.98	2.9	–	0.80	–	
Output Drive Current — Segments (AL Device)	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current — Segments (CL/CP Device)	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Pet Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Pet Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.9 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.8 μA/kHz) f + I_{DD}							
		15	I_T = (5.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +25°C for CL/CP Device.

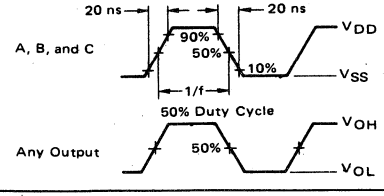
Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

† To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

** The formulas given are for the typical characteristics only at 25°C.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

Input LE and RBI low, and Inputs D, $\overline{BI}$ and $\overline{LT}$ high.
f in respect to a system clock.
All outputs connected to respective C_L loads.



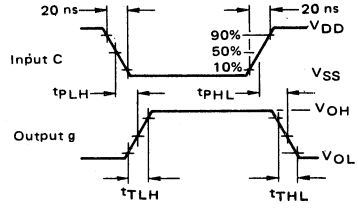
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise Time – Segment Outputs	t_{TLH}					ns
		5.0	–	40	80	
		10	–	30	60	
		15	–	25	50	
Output Rise Time – RBO Output	t_{TLH}					ns
		5.0	–	480	960	
		10	–	240	480	
		15	–	190	380	
Output Fall Time – Segment Outputs	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 50 ns		5.0	–	125	250	
t_{THL} = (0.75 ns/pF) C_L + 37.5 ns		10	–	75	150	
t_{THL} = (0.55 ns/pF) C_L + 37.5 ns		15	–	65	130	
Output Fall Time – RBO Outputs	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 50 ns		5.0	–	270	540	
t_{THL} = (0.75 ns/pF) C_L + 37.5 ns		10	–	135	270	
t_{THL} = (0.55 ns/pF) C_L + 37.5 ns		15	–	110	220	
Propagation Delay Time – A, B, C, D Inputs	t_{PLH}					ns
t_{PLH} = (0.40 ns/pF) C_L + 620 ns		5.0	–	640	1280	
t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns		10	–	250	500	
t_{PLH} = (0.20 ns/pF) C_L + 165 ns		15	–	175	350	
t_{PHL} = (1.3 ns/pF) C_L + 655 ns	t_{PHL}	5.0	–	720	1440	ns
t_{PHL} = (0.60 ns/pF) C_L + 260 ns		10	–	290	580	
t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns		15	–	200	400	
Propagation Delay Time – RBI Input	t_{PLH}					ns
t_{PLH} = (0.30 ns/pF) C_L + 305 ns		5.0	–	600	750	
t_{PLH} = (0.25 ns/pF) C_L + 117.5 ns		10	–	200	300	
t_{PLH} = (0.15 ns/pF) C_L + 92.5 ns		15	–	150	220	
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns	t_{PHL}	5.0	–	485	970	ns
t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns		10	–	200	400	
t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns		15	–	160	320	
Propagation Delay Time – BI Input	t_{PLH}					ns
t_{PLH} = (0.3 ns/pF) C_L + 305 ns		5.0	–	600	750	
t_{PLH} = (0.25 ns/pF) C_L + 117.5 ns		10	–	200	300	
t_{PLH} = (0.15 ns/pF) C_L + 92.5 ns		15	–	150	220	
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns	t_{PHL}	5.0	–	485	970	ns
t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns		10	–	200	400	
t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns		15	–	160	320	
Propagation Delay Time – LT Input	t_{PLH}					ns
t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns		5.0	–	313	625	
t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns		10	–	125	250	
t_{PLH} = (0.20 ns/pF) C_L + 80 ns		15	–	90	180	
t_{PHL} = (1.3 ns/pF) C_L + 248 ns	t_{PHL}	5.0	–	313	625	ns
t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns		10	–	125	250	
t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns		15	–	90	180	
Minimum Setup Time	t_{su}	5.0	–	90	180	ns
		10	–	38	76	
		15	–	20	40	
Minimum Hold Time	t_h	5.0	–	-90	0	ns
		10	–	-38	0	
		15	–	-20	0	
Minimum Latch Enable Pulse Width	$t_{WL(LE)}$	5.0	–	260	520	ns
		10	–	110	220	
		15	–	65	130	

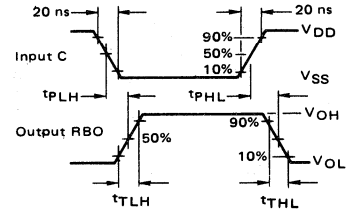
*The formula given is for the typical characteristics only.

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS

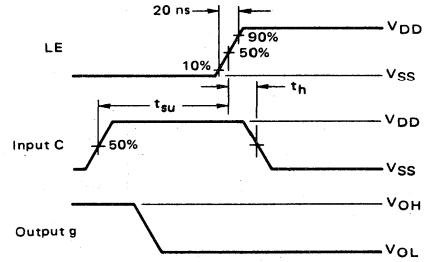
a. Data Propagation Delay: Inputs RBI, D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



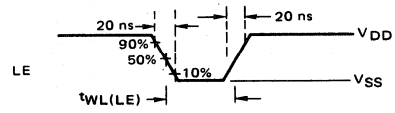
b. Inputs A, B, D and LE low, and Inputs RBI, $\overline{BI}$ and $\overline{LT}$ high.



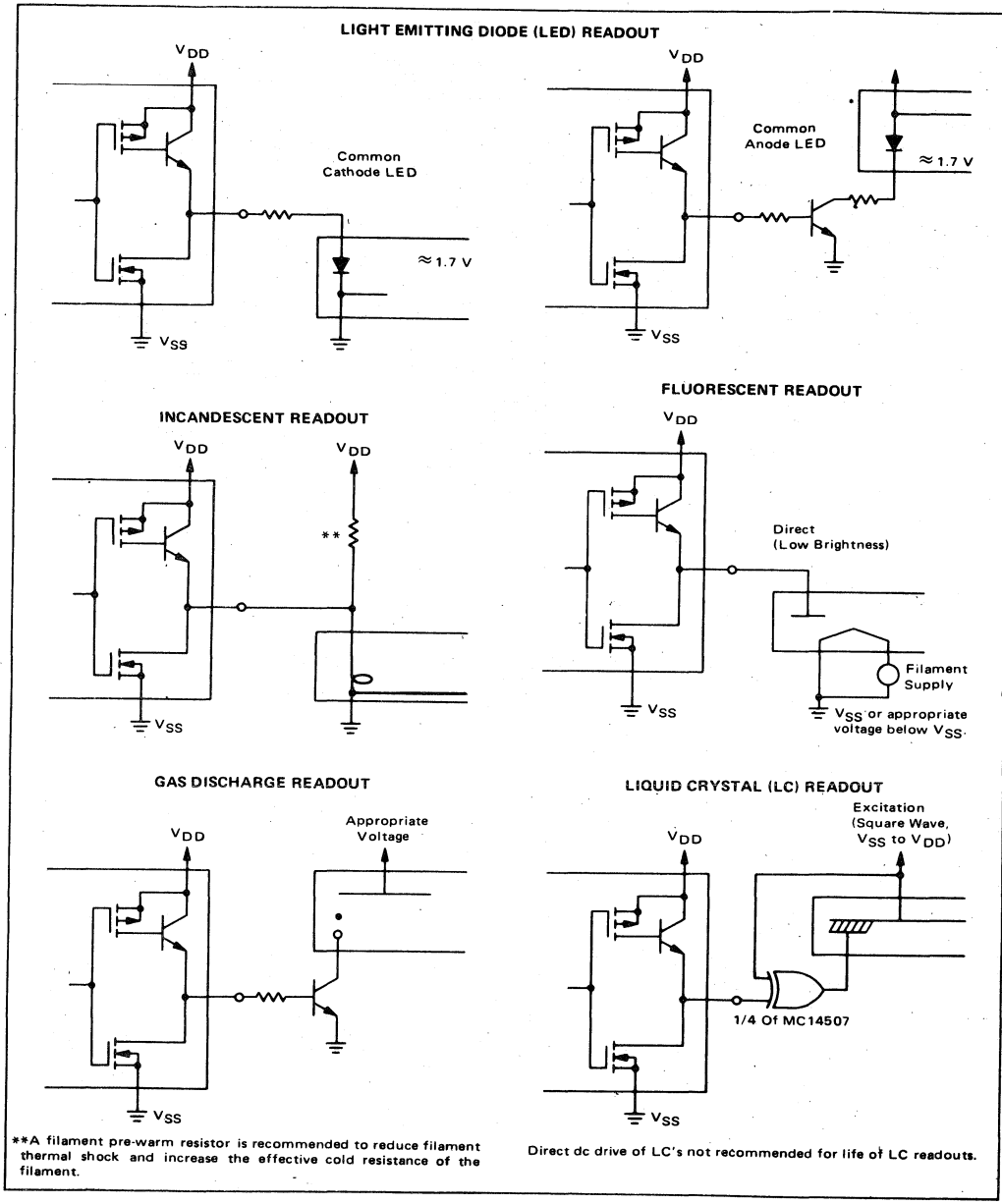
c. Setup and Hold Times: Input RBI and D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



d. Pulse Width: Data DCBA strobed into latches.



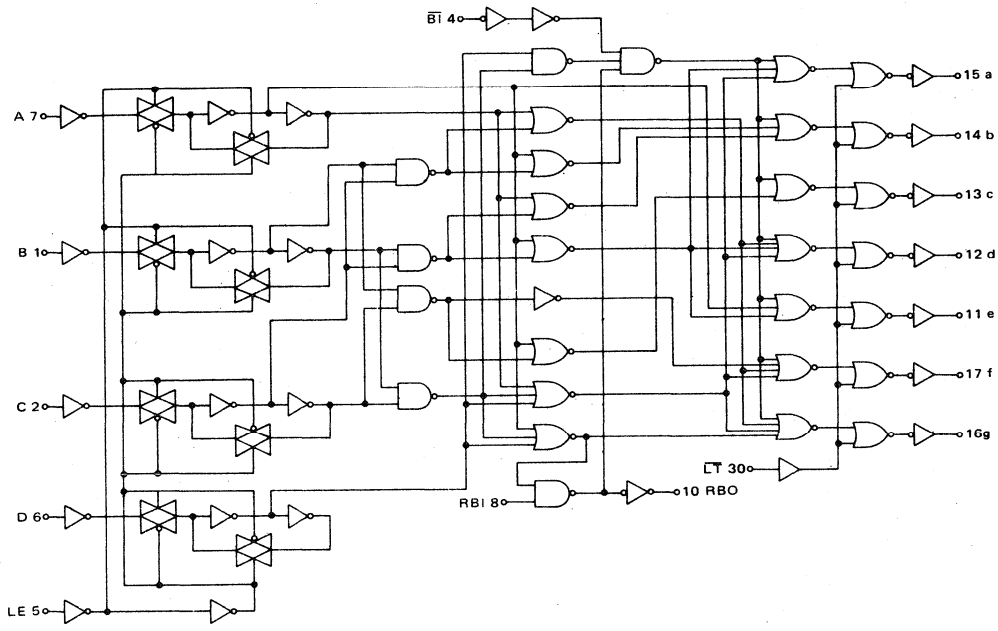
CONNECTIONS TO VARIOUS DISPLAY READOUTS



**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

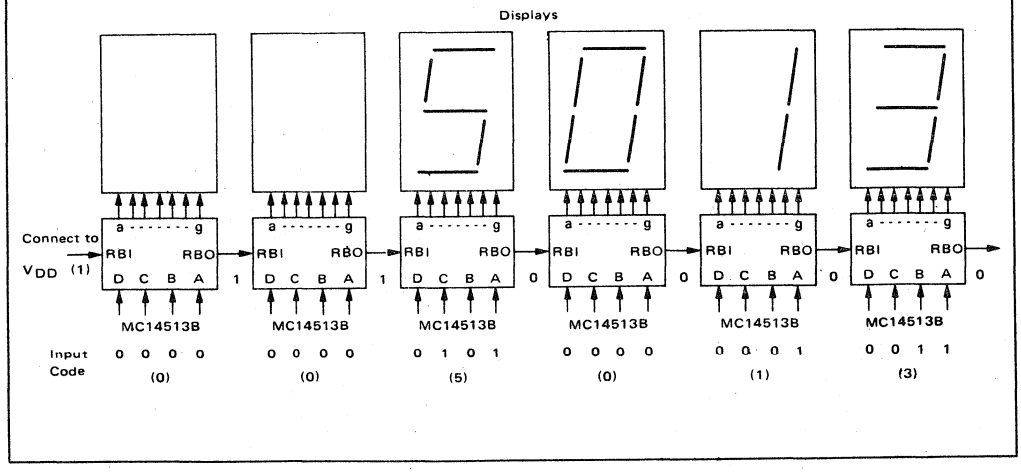
Direct dc drive of LC's not recommended for life of LC readouts.

LOGIC DIAGRAM



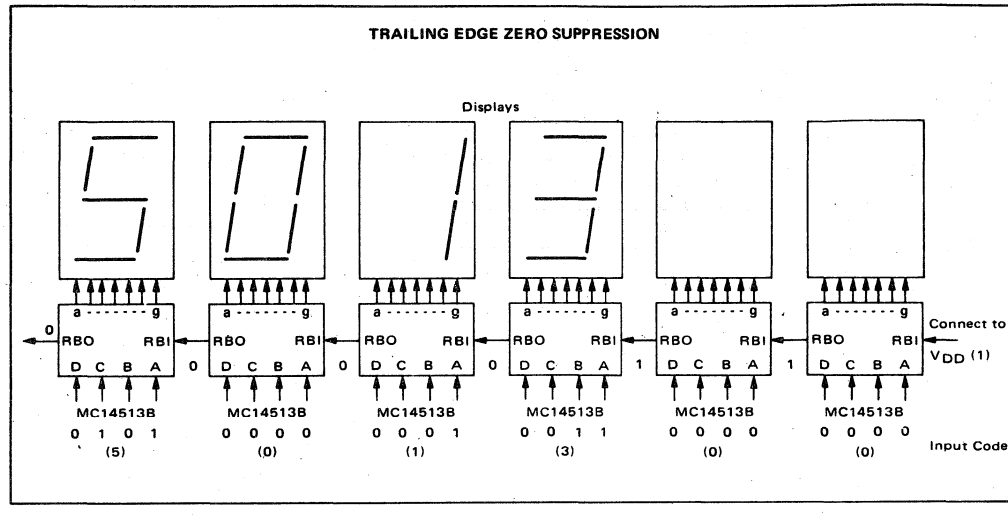
TYPICAL APPLICATIONS FOR RIPPLE BLANKING

LEADING EDGE ZERO SUPPRESSION



TYPICAL APPLICATIONS FOR RIPPLE BLANKING (Cont)

TRAILING EDGE ZERO SUPPRESSION



MOTOROLA

MC14514B
MC14515B

4-BIT LATCH/4-TO-16 LINE DECODER

The MC14514B and MC14515B are two output options of a 4 to 16 line decoder with latched inputs. The MC14514B (output active high option) presents a logical "1" at the selected output, whereas the MC14515B (output active low option) presents a logical "0" at the selected output. The latches are R-S type flip-flops which hold the last input data presented prior to the strobe transition from "1" to "0". These high and low options of a 4-bit latch/4 to 16 line decoder are constructed with N-channel and P-channel enhancement mode devices in a single monolithic structure. The latches are R-S type flip-flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

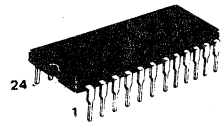
These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 5.0 nA package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Single Supply Operation – Positive or Negative
- Input Impedance = 10^{12} ohms typical

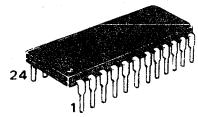
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT LATCH/4-TO-16 LINE DECODER



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

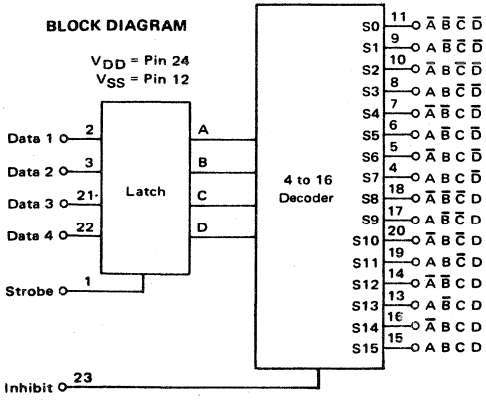
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DATA INPUTS D	C	B	A	SELECTED OUTPUT MC14514 = Logic "1" MC14515 = Logic "0"
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, MC14514 All Outputs = 1, MC14515

X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.35 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.70 µA/kHz) f + I_{DD}							
		15	I_T = (4.05 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
Inhibit Propagation Delay Times	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	150	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Setup Time	t_{su}					ns
		5.0	250	125	–	
		10	100	50	–	
		15	75	38	–	
Strobe Pulse Width	t_{WH}					ns
		5.0	350	175	–	
		10	100	50	–	
		15	75	38	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – DRAIN CHARACTERISTICS TEST CIRCUIT

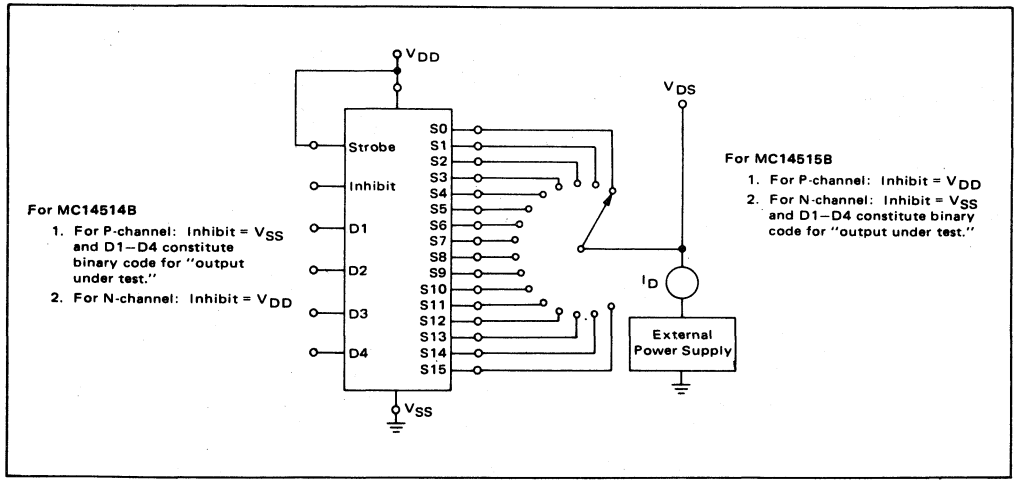


FIGURE 2 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

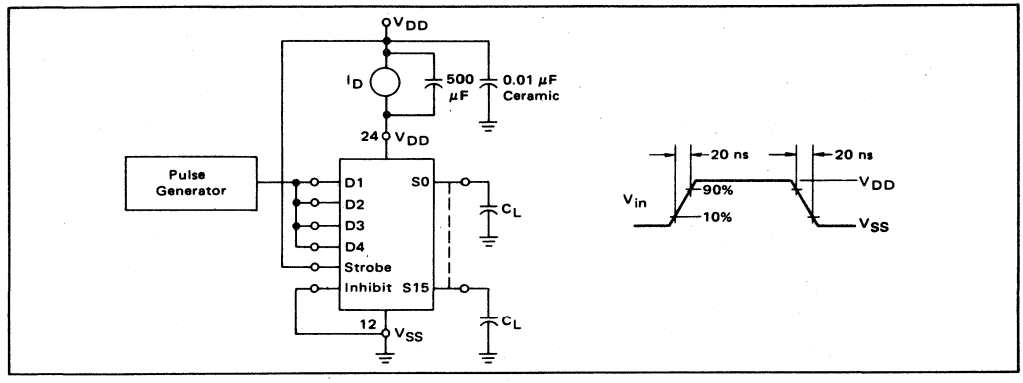
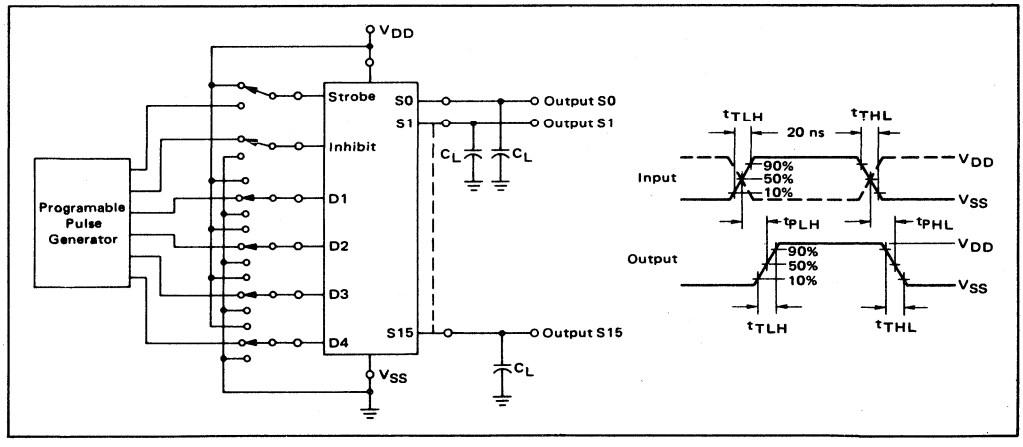
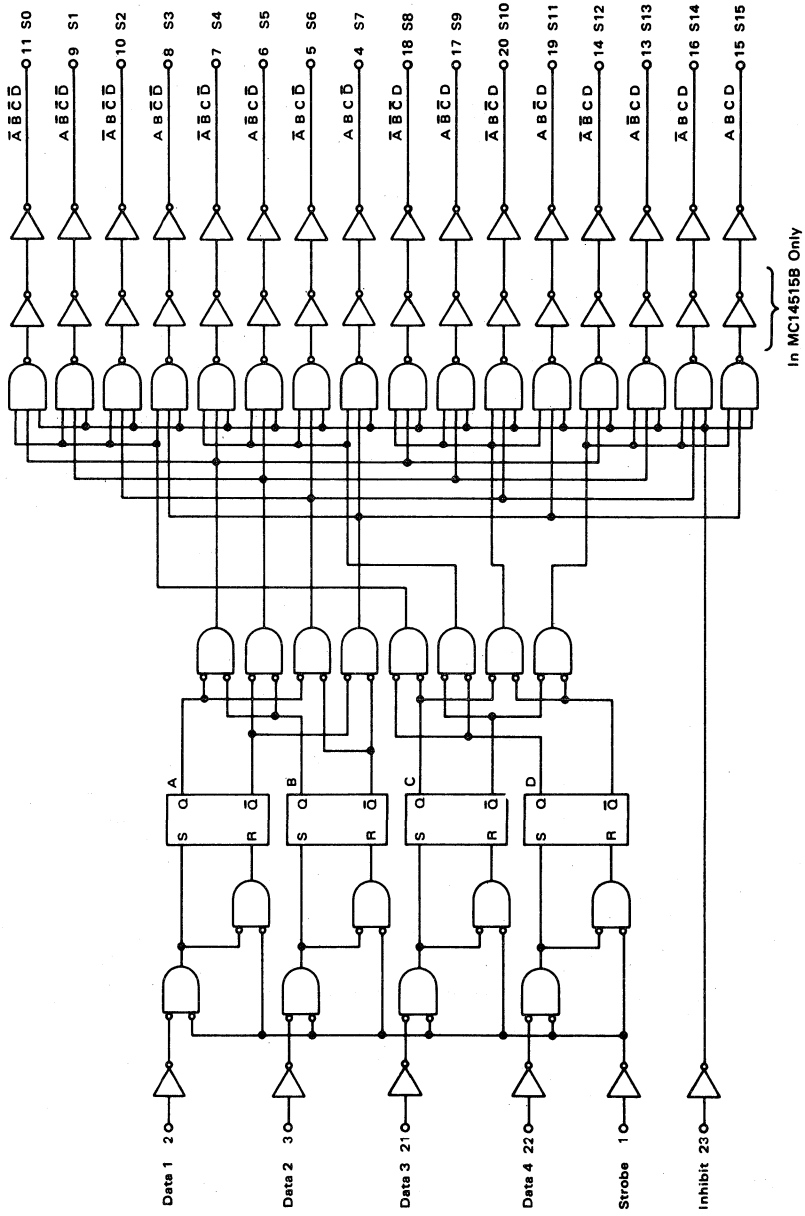


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAM



COMPLEX DATA ROUTING

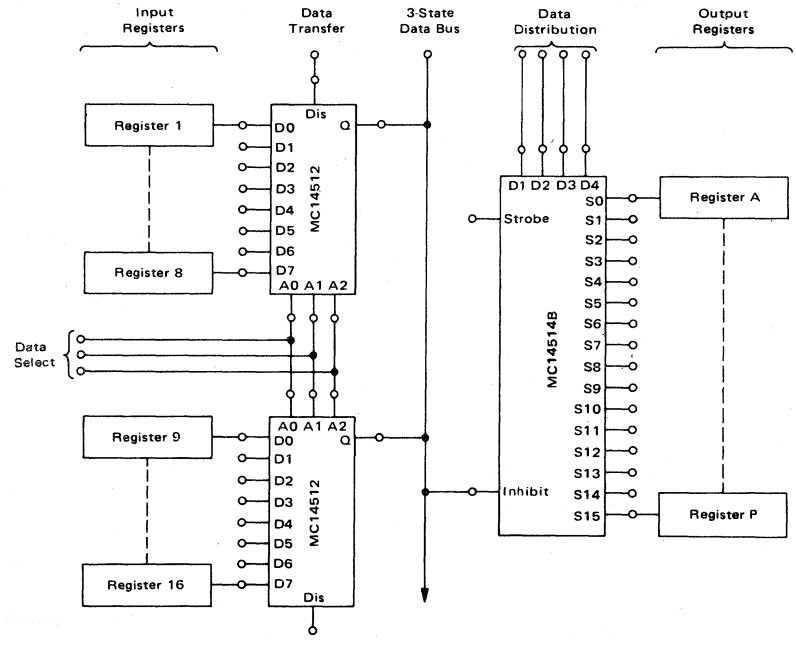
Two MC14512 eight-channel data selectors are used here with the MC14514B four-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3-state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3-state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-state bus is redistributed by the MC14514B four-bit latch/decoder. Using the four-bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

DATA ROUTING SYSTEM



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14516B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

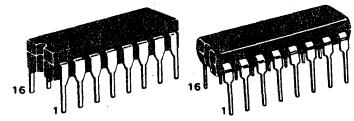
BINARY UP/DOWN COUNTER

BINARY UP/DOWN COUNTER

The MC14516B is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This complementary MOS circuit finds primary use where low power dissipation and/or high noise immunity is desired.

This binary presettable up/down counter may be used as a counting/frequency synthesizer, in A/D and D/A conversion, for up/down counting, for magnitude and sign generation, and for difference counting.

- Quiescent Current = 5.0nA/package typical @ 5.0 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance — 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design — Count Occurs on Positive Going Edge of Clock
- 5.0-MHz Counting Rate
- Single Pin Reset
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



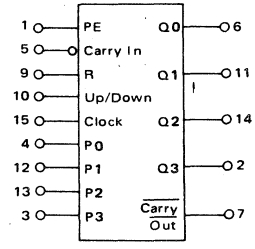
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.2 µA/kHz) f + I_{DD}							
		15	I_T = (1.7 µA/kHz) f + I_{DD}							

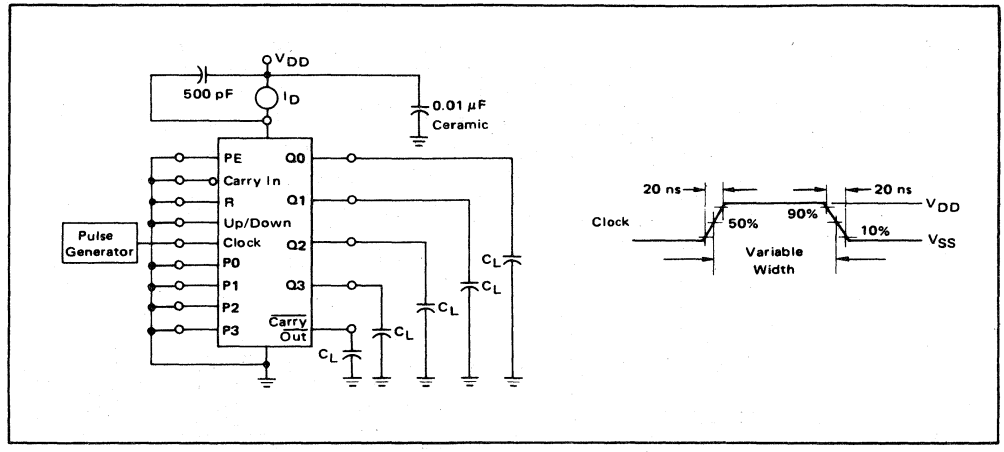
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

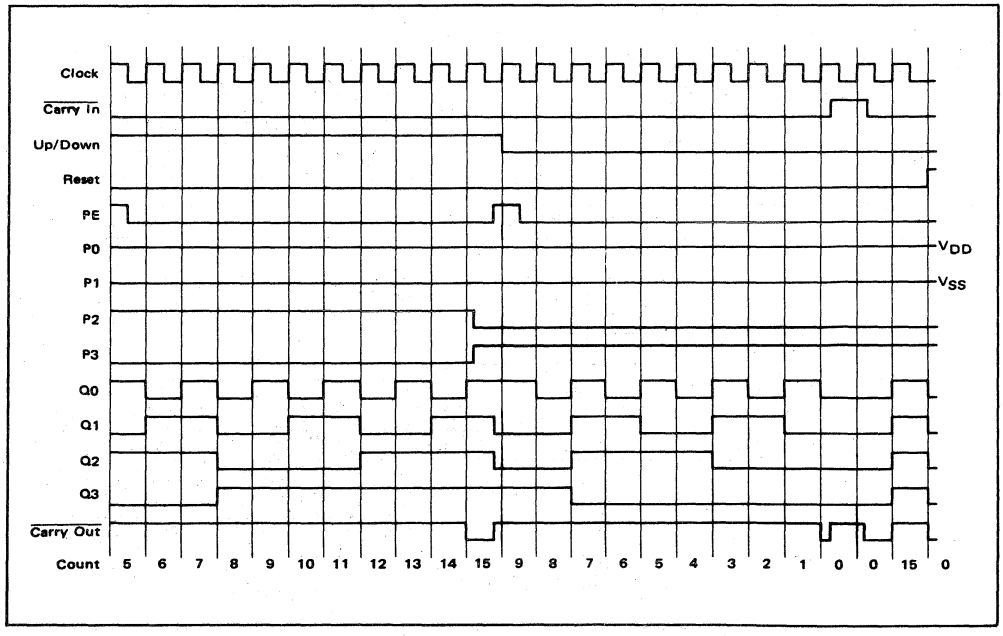
Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Clock to Carry Out	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Carry In to Carry Out	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns		5.0	–	180	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 74 ns		10	–	80	160	
t_{PLH}, t_{PHL} = 0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Preset or Reset to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Preset or Reset to Carry Out	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
Clock Pulse Width	t_{WH}	5.0	350	200	–	ns
		10	170	100	–	
		15	140	75	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Preset or Reset Removal Time **	t_{rem}	5.0	650	325	–	ns
		10	230	115	–	
		15	180	90	–	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
$\overline{\text{Carry In}}$ Setup Time	t_{su}	5.0	260	130	–	ns
		10	120	60	–	
		15	100	50	–	
Up/Down Setup Time	t_{su}	5.0	500	250	–	ns
		10	200	100	–	
		15	150	75	–	
Preset Enable Pulse Width	t_{WH}	5.0	200	100	–	ns
		10	100	50	–	
		15	80	40	–	

*The formula given is for the typical characteristics only.
**The Preset or Reset signal must be low prior to a positive-going transition of the clock.

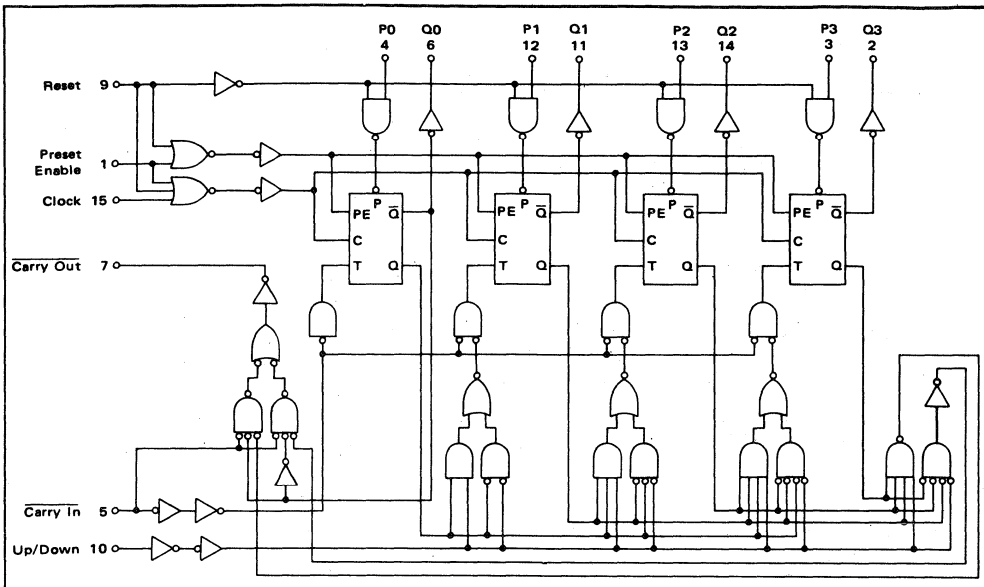
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



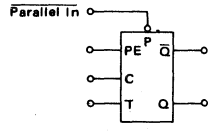
TIMING DIAGRAM



LOGIC DIAGRAM



TOGGLE FLIP-FLOP



FLIP-FLOP FUNCTIONAL TRUTH TABLE

PRESET ENABLE	CLOCK	T	Q_{n+1}
1	X	X	Parallel In
0	↑	0	Q_n
0	↑	1	$\overline{Q}_n$
0	↓	X	Q_n

X = Don't Care

FIGURE 2 – SWITCHING TIME WAVEFORMS

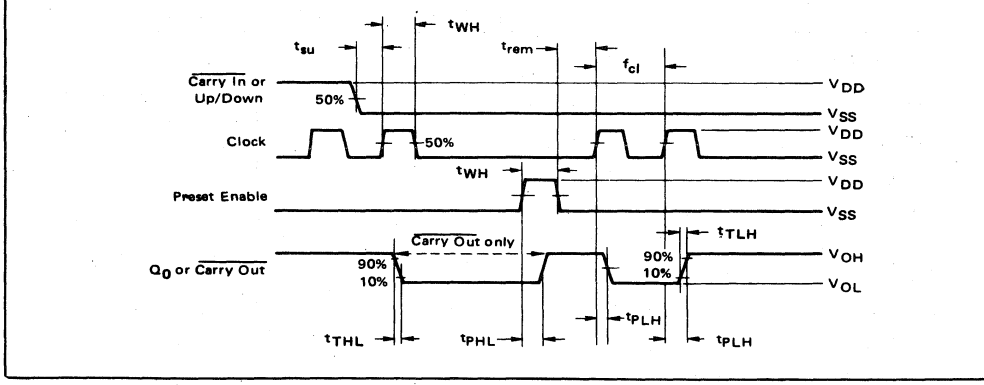


FIGURE 3 – PRESETTABLE CASCADED UP/DOWN COUNTER

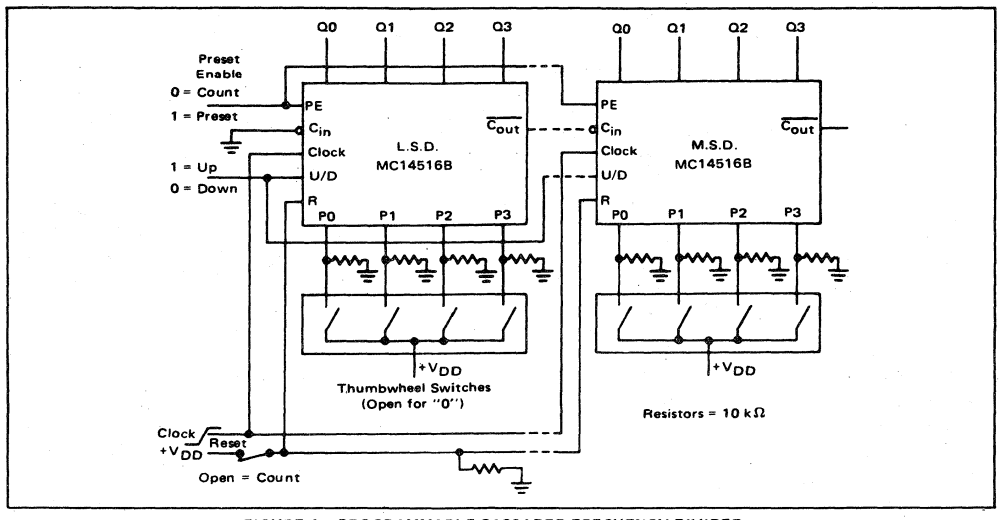
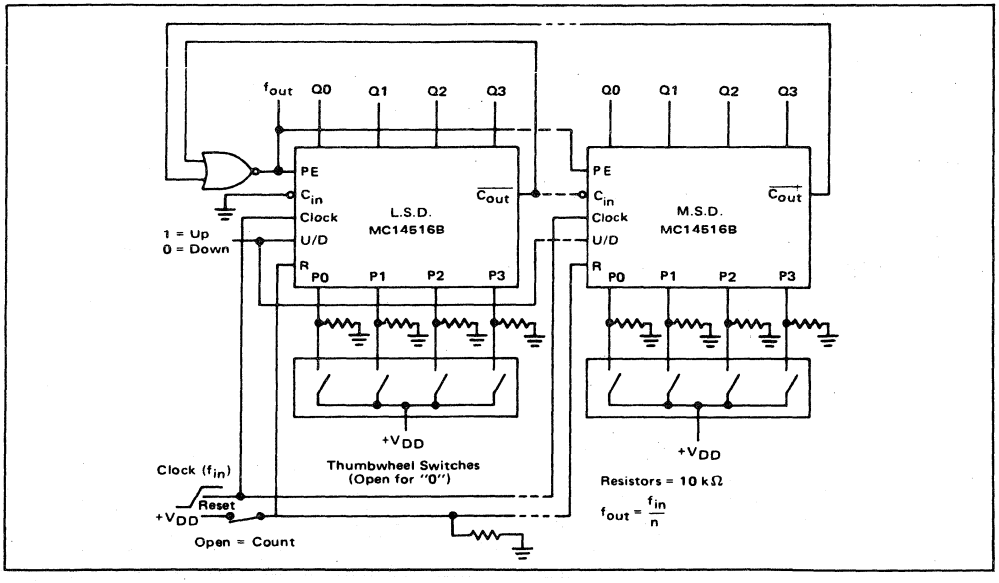


FIGURE 4 – PROGRAMMABLE CASCADED FREQUENCY DIVIDER



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14517B

CMOS LSI

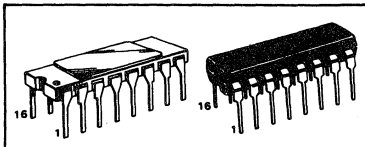
(LOW-POWER COMPLEMENTARY MOS)

DUAL 64-BIT STATIC SHIFT REGISTER

DUAL 64-BIT STATIC SHIFT REGISTER

The MC14517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Quiescent Current = 10 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- 6.7 MHz Operation @ V_{DD} = 10 Vdc
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3-State Output at 64th-Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



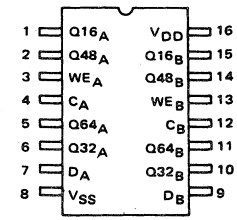
L SUFFIX
CERAMIC PACKAGE
CASE 690

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FUNCTIONAL TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	16-BIT TAP	32-BIT TAP	48-BIT TAP	64-BIT TAP
0	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
↗	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
↗	1	Data entered into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 33-Bit	Data at tap entered into 49-Bit	High Impedance
↘	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
↘	1	X	High Impedance	High Impedance	High Impedance	High Impedance

X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (4.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (8.8 µA/kHz) f + I_{DD}							
		15	I_T = (13.7 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 390 ns	t_{PHL}	5.0	–	475	770	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 177 ns		10	–	210	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	–	140	215	
Clock Pulse Width	t_{WH}	5.0	330	170	–	ns
		10	125	75	–	
		15	100	60	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	6.7	4.0	
		15	–	8.3	5.3	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0				–
		10		**See Note		
		15				
Data to Clock Setup Time	t_{su}	5.0	0	-40	–	ns
		10	10	-15	–	
		15	15	0	–	
Data to Clock Hold Time	t_h	5.0	150	75	–	ns
		10	75	25	–	
		15	35	10	–	
Write Enable to Clock Setup Time	t_{su}	5.0	400	170	–	ns
		10	200	65	–	
		15	110	50	–	
Write Enable to Clock Release Time	t_{rel}	5.0	380	160	–	ns
		10	180	55	–	
		15	100	40	–	

*The formula given is for the typical characteristics only.

**When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

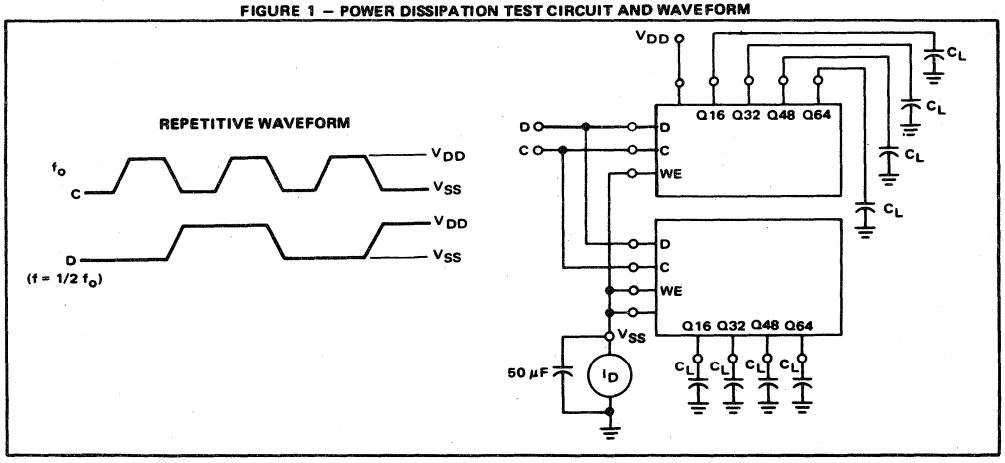
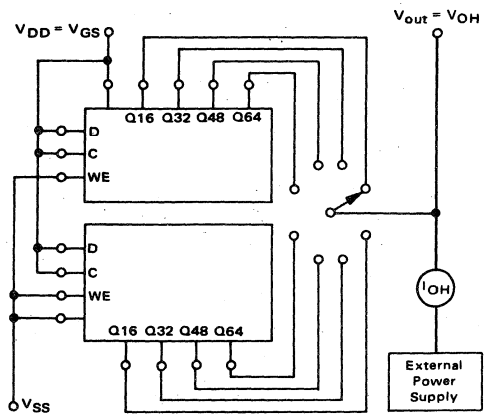
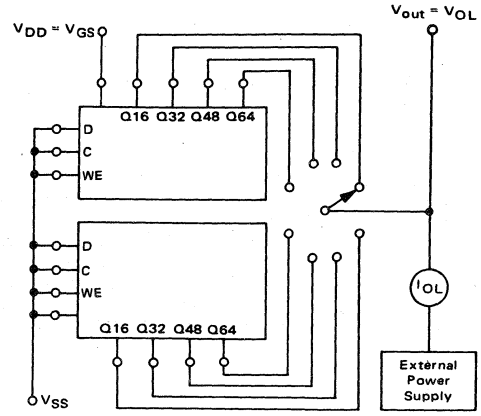


FIGURE 2 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT



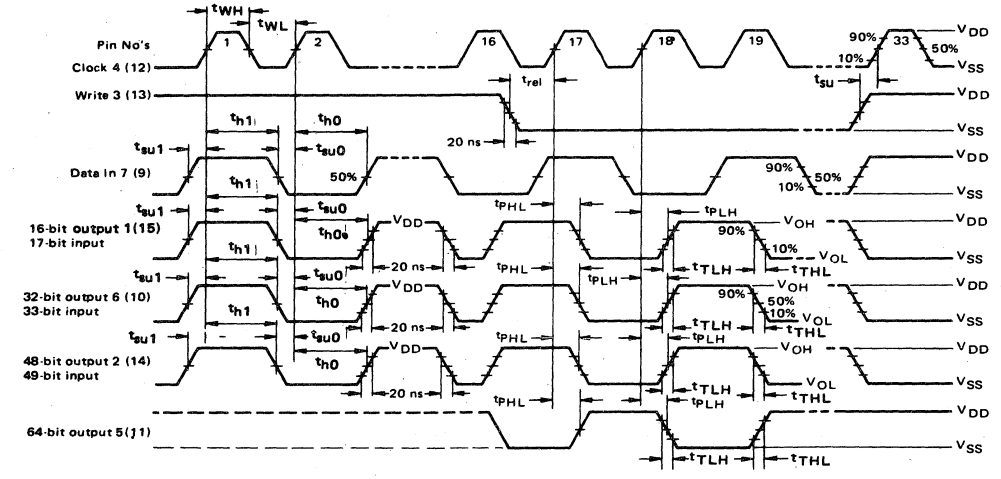
(Output being tested should be in the high-logic state).

FIGURE 3 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT

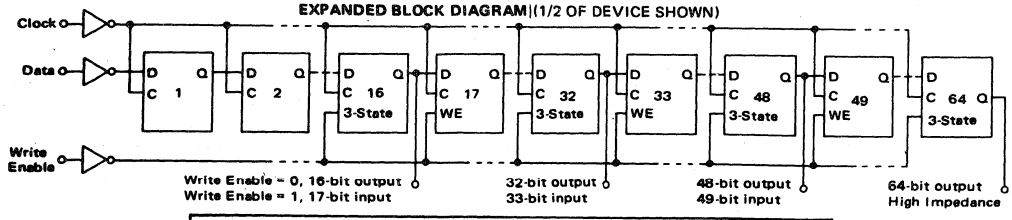


(Output being tested should be in the low-logic state).

FIGURE 4 – AC TEST WAVEFORMS



EXPANDED BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14518B
MC14520B

CMOS MSI

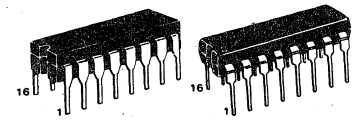
(LOW-POWER COMPLEMENTARY MOS)

DUAL BCD UP COUNTER
(MC14518B)
DUAL BINARY UP COUNTER
(MC14520B)

DUAL UP COUNTERS

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



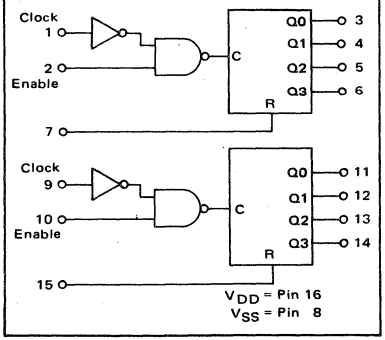
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.6	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.6 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.2 µA/kHz) f + I_{DD}							
		15	I_T = (1.7 µA/kHz) f + I_{DD}							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q/Enable to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	115	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	80	160	
Reset to Q						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	330	650	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	130	230	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 95 ns		15	–	90	170	
Clock Pulse Width	t_{WH}	5.0	200	100	–	ns
	t_{WL}	10	100	50	–	
		15	70	35	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.5	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Clock or Enable Rise and Fall Time	t_{THL}, t_{TLH}	5.0	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
Enable Pulse Width	$t_{WH(E)}$	5.0	440	220	–	ns
		10	200	100	–	
		15	140	70	–	
Reset Pulse Width	$t_{WH(R)}$	5.0	250	125	–	ns
		10	110	55	–	
		15	80	40	–	

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

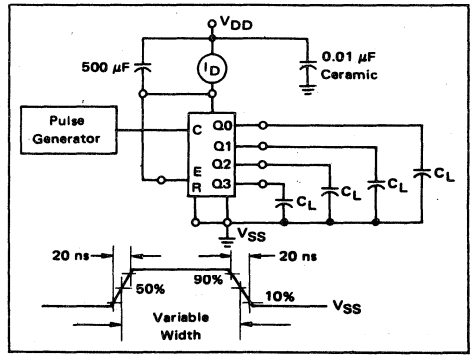


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

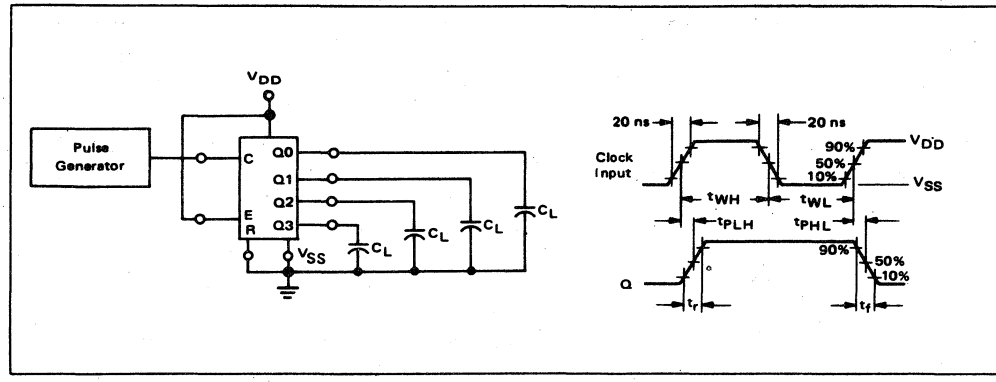


FIGURE 3 – TIMING DIAGRAM

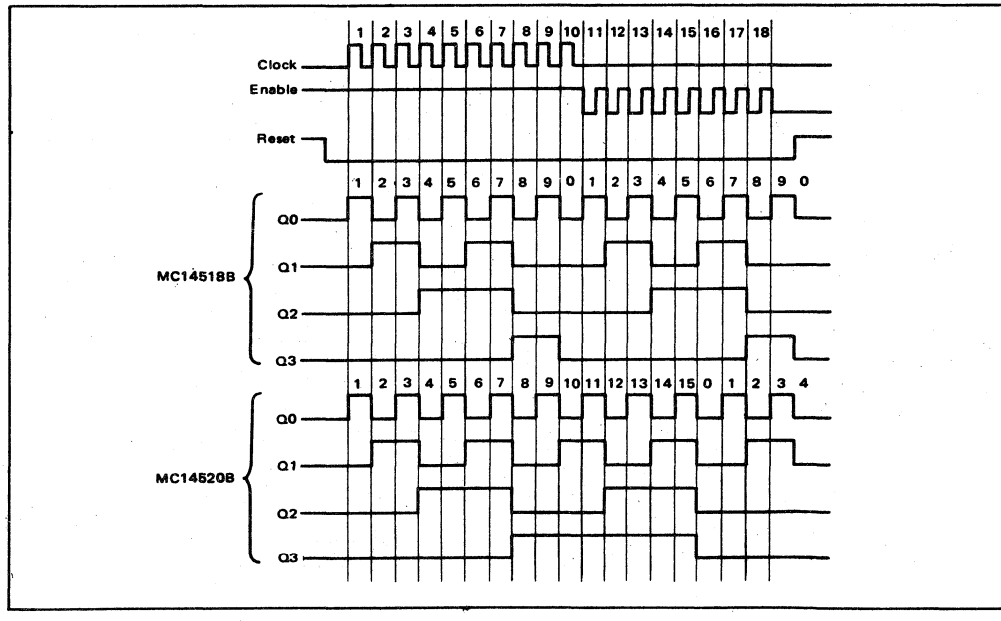


FIGURE 4 – DECADE COUNTER (MC14518B) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)

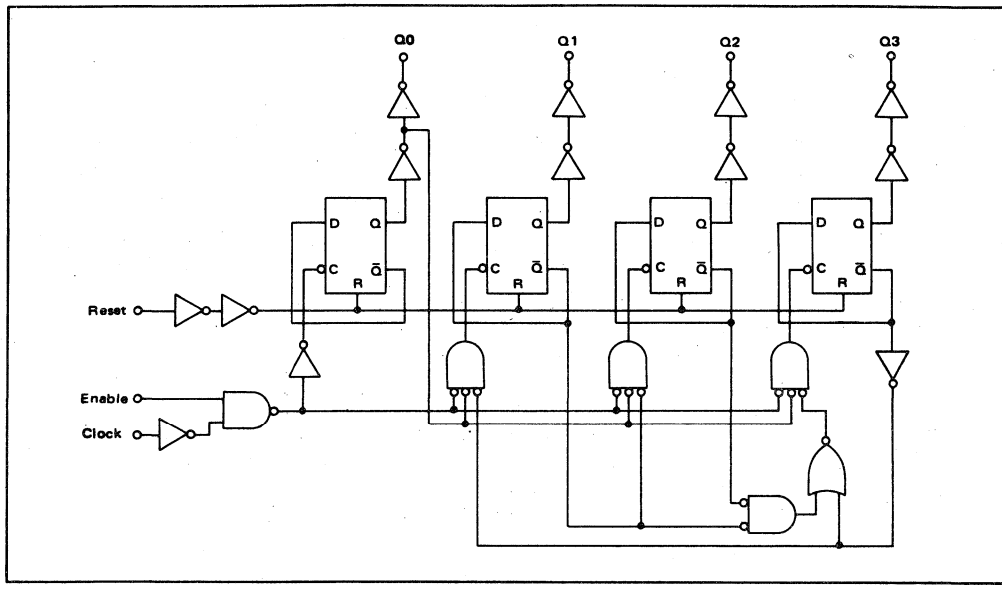
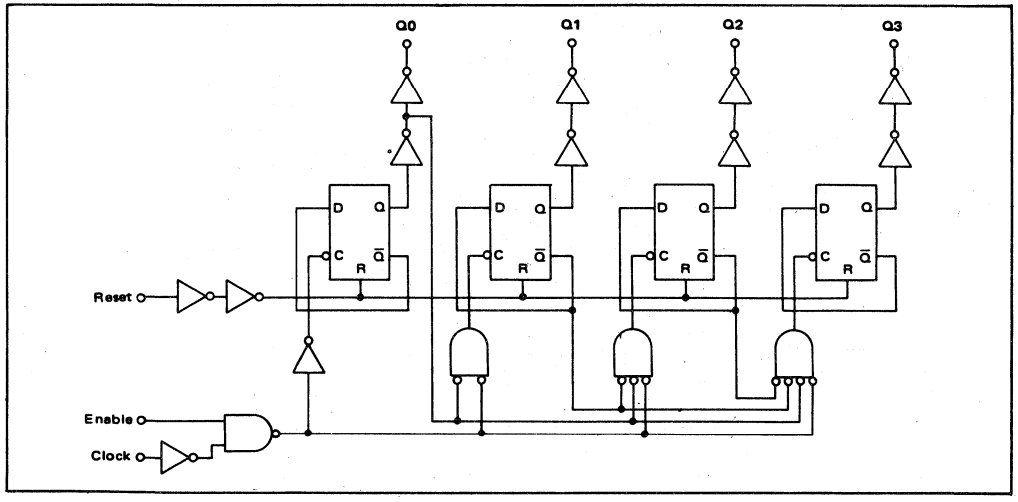


FIGURE 5 – BINARY COUNTER (MC14520B) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)



MOTOROLA

MC14519B

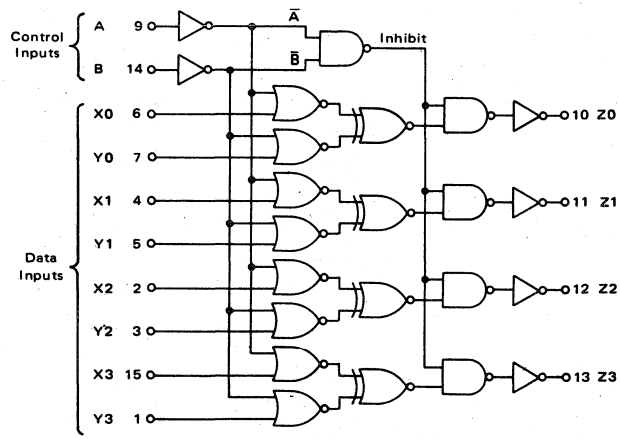
4-BIT AND/OR SELECTOR
or
QUAD 2-CHANNEL DATA SELECTOR
or
QUAD EXCLUSIVE "NOR" GATE

The MC14519B is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device exemplifies the design versatility of McMOS logic structure. This part provides three functions in one package; a 4-Bit AND/OR Selector, a Quad 2-Channel Data Selector, or a Quad Exclusive NOR Gate.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Plug-In Replacement for CD4019 in Most Applications

LOGIC DIAGRAM
(Positive Logic)

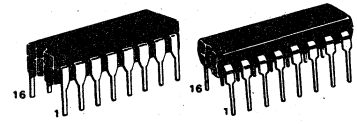


V_{DD} = Pin 16
V_{SS} = Pin 8

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT AND/OR SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

TRUTH TABLE

CONTROL INPUTS		OUTPUT
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \circledcirc Y_n$

Note:
$X_n \circledcirc Y_n$ means X_n (Exclusive-NOR) Y_n

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.4 µA/kHz) f + I_{DD}							
		15	I_T = (3.6 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 165 hs		5.0	–	250	500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 82		10	–	115	225	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	165	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

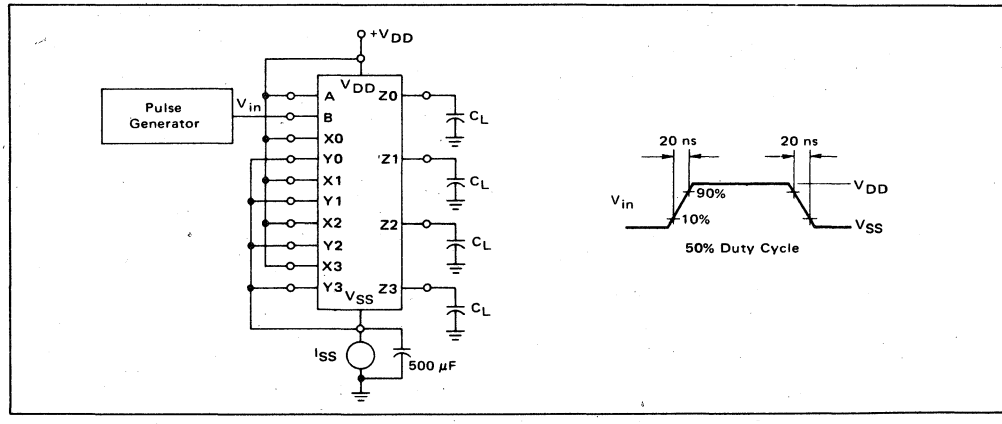
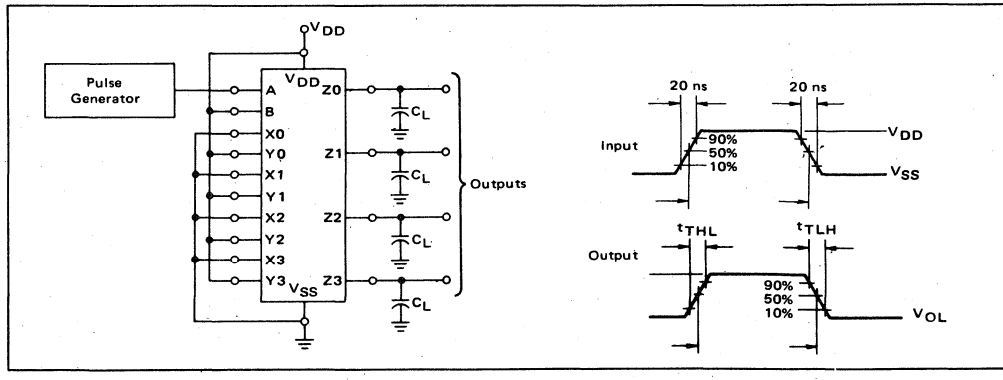
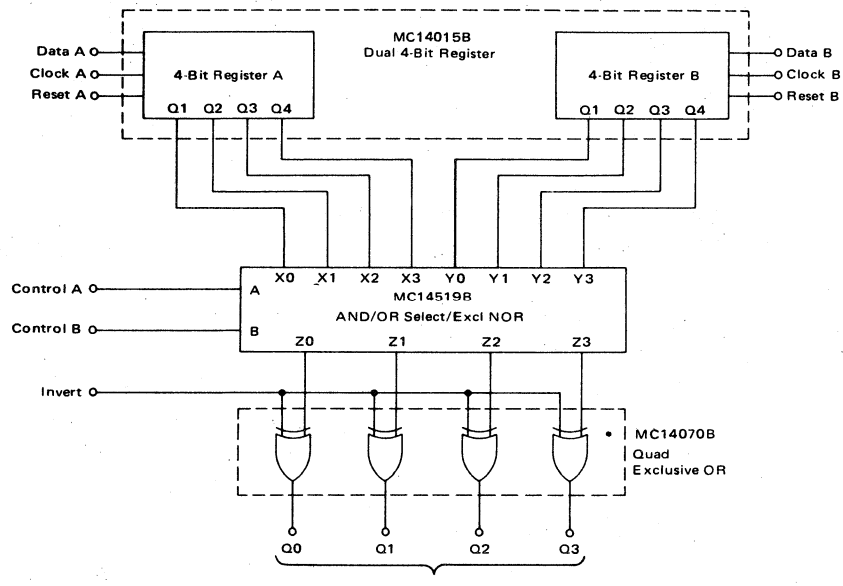


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TYPICAL CIRCUIT APPLICATIONS

DATA REGISTER SELECTION COMPARISON



CONVERSION TABLE

OPERATION CODE			OUTPUT				FUNCTION
A	B	INV	Q0	Q1	Q2	Q3	
0	0	0	0	0	0	0	Inhibit, all zeros
0	0	1	1	1	1	1	Inhibit, all ones
1	0	0	X0	X1	X2	X3	Control A
1	0	1	$\overline{X0}$	$\overline{X1}$	$\overline{X2}$	$\overline{X3}$	Control A and Invert
0	1	0	Y0	Y1	Y2	Y3	Control B
0	1	1	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	Control B and Invert
1	1	0	X0 ⊙ Y0	X1 ⊙ Y1	X2 ⊙ Y2	X3 ⊙ Y3	Exclusive NOR
1	1	1	X0 ⊕ Y0	X1 ⊕ Y1	X2 ⊕ Y2	X3 ⊕ Y3	Exclusive OR

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14520B

FOR COMPLETE DATA
SEE MC14518B

CMOS MSI

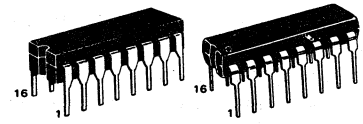
(LOW-POWER COMPLEMENTARY MOS)

DUAL BCD UP COUNTER
(MC14518B)
DUAL BINARY UP COUNTER
(MC14520B)

DUAL UP COUNTERS

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



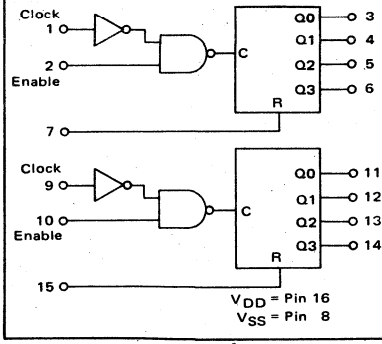
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14521B

CMOS MSI

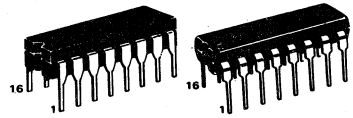
(LOW-POWER COMPLEMENTARY MOS)

24-STAGE FREQUENCY DIVIDER

24-STAGE FREQUENCY DIVIDER

The MC14521B consists of a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently this part will count up to 2^{24} = 16,777,216. The count advances on the negative going edge of the clock. The outputs of the last seven-stages are available for added flexibility.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- $f_{(max)}$ = 9.0 MHz typical @ V_{DD} = 10V
- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- V_{DD}' and V_{SS}' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low-Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.



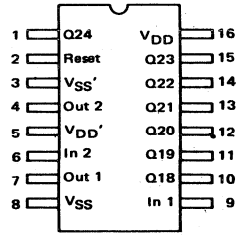
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

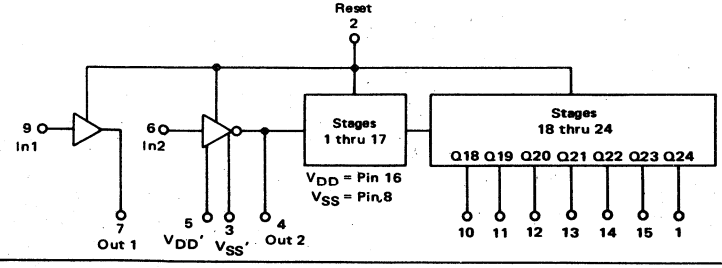
PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



OUTPUT	COUNT CAPACITY
Q18	2^{18} = 262,144
Q19	2^{19} = 524,288
Q20	2^{20} = 1,048,576
Q21	2^{21} = 2.097,152
Q22	2^{22} = 4,194,304
Q23	2^{23} = 8,388,608
Q24	2^{24} = 16,777,216

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.42 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.85 μA/kHz) f + I_{DD}							
		15	I_T = (1.4 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

SWITCHING CHARACTERISTICS* (IC_L = 50 pF' T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{TLH}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	110	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					μs
Clock to Q18						
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 4415 ns		5.0	–	4.5	9.0	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 1667 ns		10	–	1.7	3.5	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 1275 ns		15	–	1.3	2.7	
Clock to Q24						μs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns		5.0	–	6.0	12	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2167 ns		10	–	2.2	4.5	
t_{PHL}, t_{PHL} = (0.5 ns/pF) C_L + 1675 ns		15	–	1.7	3.5	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 1215 ns		5.0	–	1300	2600	
t_{PHL} = (0.66 ns/pF) C_L + 467 ns		10	–	500	1000	
t_{PHL} = (0.5 ns/pF) C_L + 350 ns		15	–	375	750	
Clock Pulse Width	$t_{WH(cl)}$	5.0	385	140	–	ns
		10	150	55	–	
		15	120	40	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.5	2.0	MHz
		10	–	9.0	5.0	
		15	–	12	6.5	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
Reset Pulse Width	$t_{WH(R)}$	5.0	1400	700	–	ns
		10	600	300	–	
		15	450	225	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

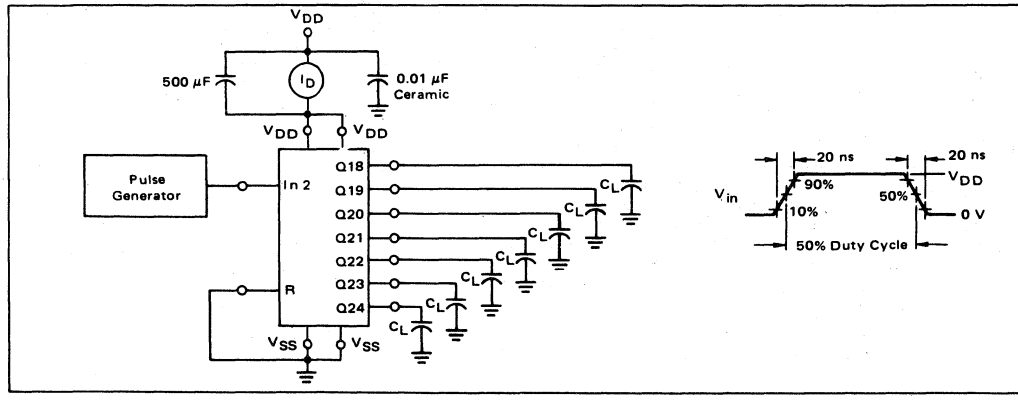


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

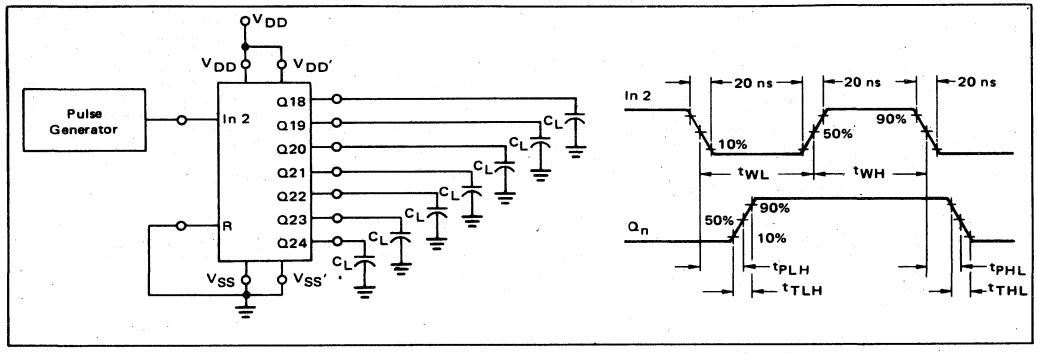
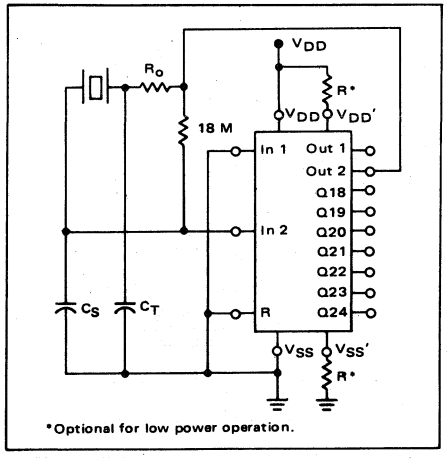


FIGURE 3 – CRYSTAL OSCILLATOR CIRCUIT



*Optional for low power operation.

FIGURE 4 – TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

CHARACTERISTIC	500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Equivalent Resistance, R_S	1.0	6.2	kΩ
External Resistor/Capacitor Values			
R_o	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Change as a Function of V_{DD} (T_A = 25°C)			
V_{DD} Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V_{DD} Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature (V_{DD} = 10 V)			
T_A Change from -55°C to +25°C			
MC14521 only	-4.0	-2.0	ppm
Complete Oscillator*	+100	+120	ppm
T_A Change from +25°C to +125°C			
MC14521 only	-2.0	-2.0	ppm
Complete Oscillator*	-160	-560	ppm

*Complete oscillator includes crystal, capacitors, and resistors.

FIGURE 5 – RC OSCILLATOR STABILITY

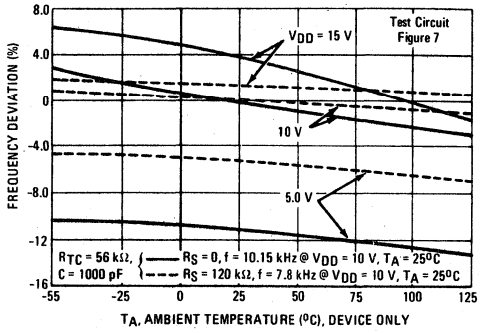


FIGURE 6 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C

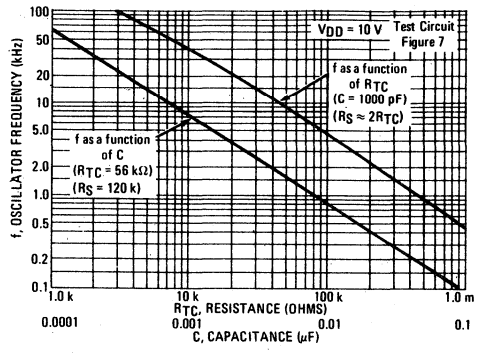


FIGURE 7 – RC OSCILLATOR CIRCUIT

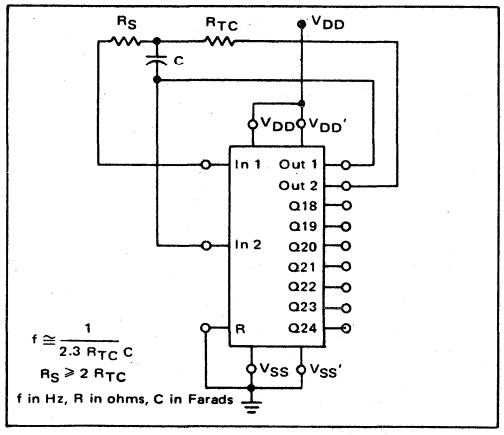
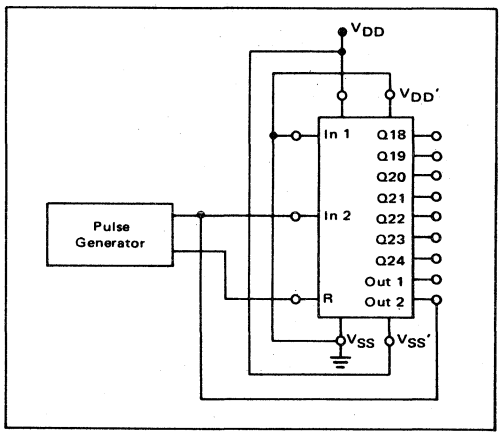


FIGURE 8 – FUNCTIONAL TEST CIRCUIT

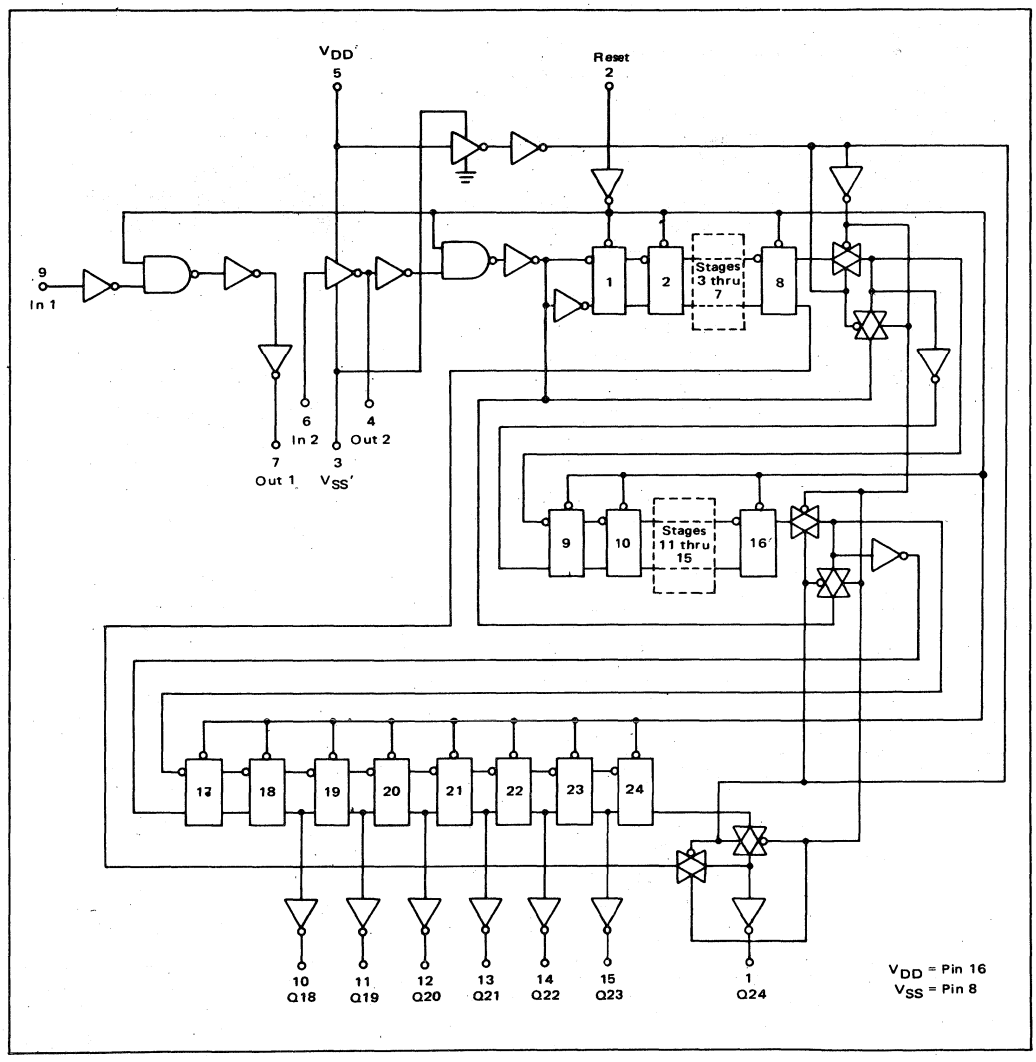


FUNCTIONAL TEST SEQUENCE

A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections, and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all "1" state to an all "0" state.

INPUTS		OUTPUTS				COMMENTS
Reset	In 2	Out 2	V_{SS}'	V_{DD}'	Q18 thru Q24	
1	0	0	V_{DD}	Gnd	0	Counter is in three 8-stage sections in parallel mode Counter is reset. In 2 and Out 2 are connected together
0	1	1				First "0" to "1" transition on In 2, Out 2 node.
	0	0				255 "0" to "1" transitions are clocked into this In 2, Out 2 node.
	1	1				
	–	–				
	–	–				
	–	–				
	1	1			1	The 255th "0" to "1" transition.
	0	0			1	
	0	0	Gnd		1	
	1	0		V_{DD}	1	Counter converted back to 24-stages in series mode.
	1				1	Out 2 converts back to an output.
	0				0	Counter ripples from an all "1" state to an all "0" stage.

LOGIC DIAGRAM



MOTOROLA

MC14522B
MC14526B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

BCD – MC14522B
Binary – MC14526B

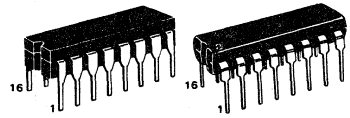
PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

The MC14522B BCD counter and the MC14526B binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure.

These devices are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Clock Inhibit input allows disabling of the pulse counting function.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds.
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition of Clock Inhibit
- 5.0 MHz Counting Rate
- Asynchronous Preset Enable
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

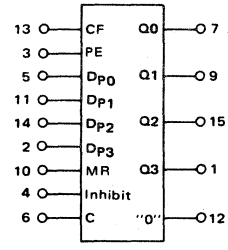
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLES

BOTH TYPES

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
↓	0	0	0	Count-1
X	1	0	0	No Count
1	↓	0	0	Count-1
X	X	1	0	Preset
X	X	X	1	Reset

MC14522B

Count	Output Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC14526B

Count	Output Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.7 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.4 µA/kHz) f + I_{DD}							
		15	I_T = (5.1 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 9.5 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	8ρ	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Q Outputs						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	–	160	320	
"0" Output						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 155 ns		5.0	–	240	480	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	100	200	
Minimum Clock Pulse Width	$t_{WH(cl)}$	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	
Maximum Clock Pulse Frequency	f_{cl}	5.0	–	2.0	1.5	MHz
		10	–	5.0	3.0	
		15	–	6.6	4.0	
Maximum Clock or Inhibit Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	15	
		15	–	–	15	
Hold Time	t_h	5.0	150	75	–	ns
		10	50	25	–	
		15	40	20	–	
Minimum Preset Enable Pulse Width	$t_{WH(PE)}$	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	
Minimum Master Reset Pulse Width	$t_{WH(R)}$	5.0	350	175	–	ns
		10	250	125	–	
		15	200	100	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

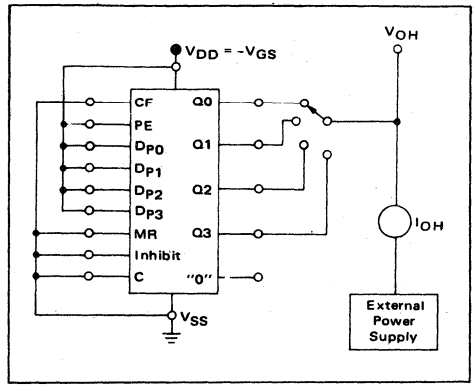


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

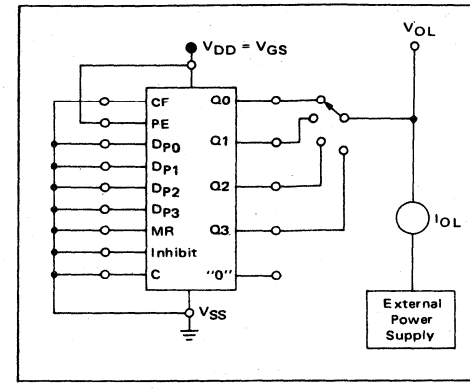


FIGURE 3 – POWER DISSIPATION

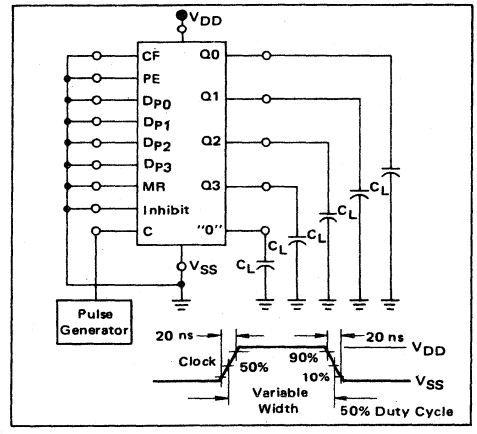


FIGURE 4 – AC TEST CIRCUITS

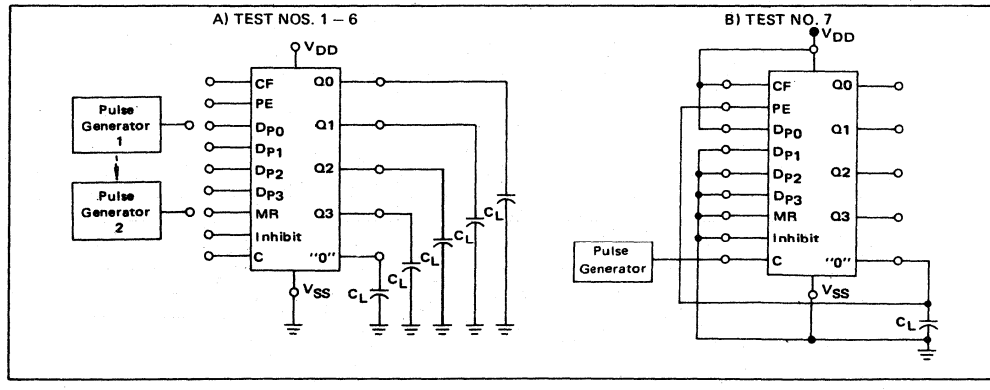
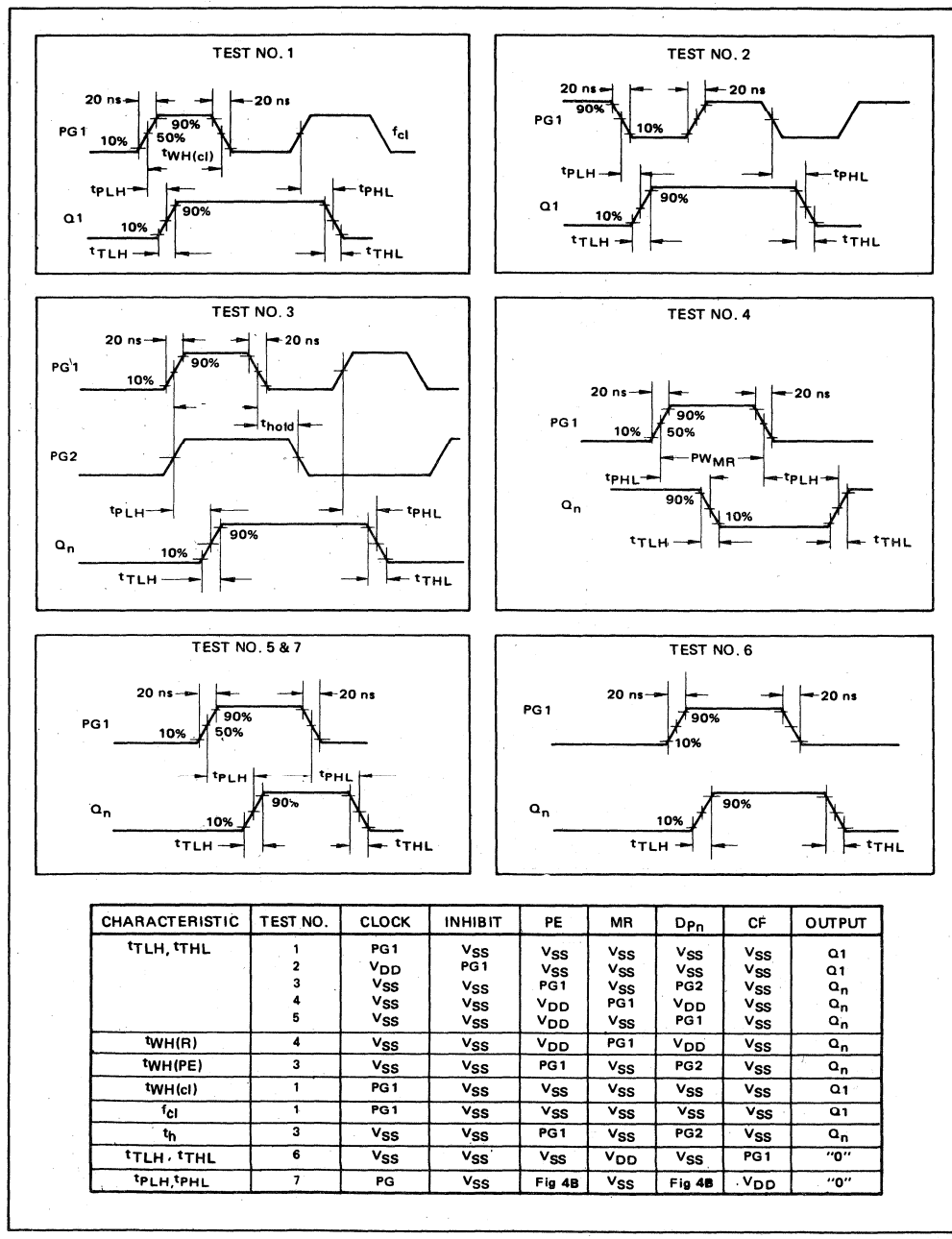


FIGURE 5 – AC TEST CONNECTIONS AND WAVEFORMS



CHARACTERISTIC	TEST NO.	CLOCK	INHIBIT	PE	MR	D_{Pn}	CF	OUTPUT
t_{TLH}, t_{THL}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	2	V_{DD}	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
	5	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	V_{SS}	Q_n
$t_{WH(R)}$	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
$t_{WH(PE)}$	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
$t_{WH(cl)}$	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
f_{cl}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
t_h	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
t_{TLH}, t_{THL}	6	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	"0"
t_{PLH}, t_{PHL}	7	PG	V_{SS}	Fig 4B	V_{SS}	Fig 4B	V_{DD}	"0"

FIGURE 6 – MC14522B LOGIC DIAGRAM (BCD Divide-by-N Counter)

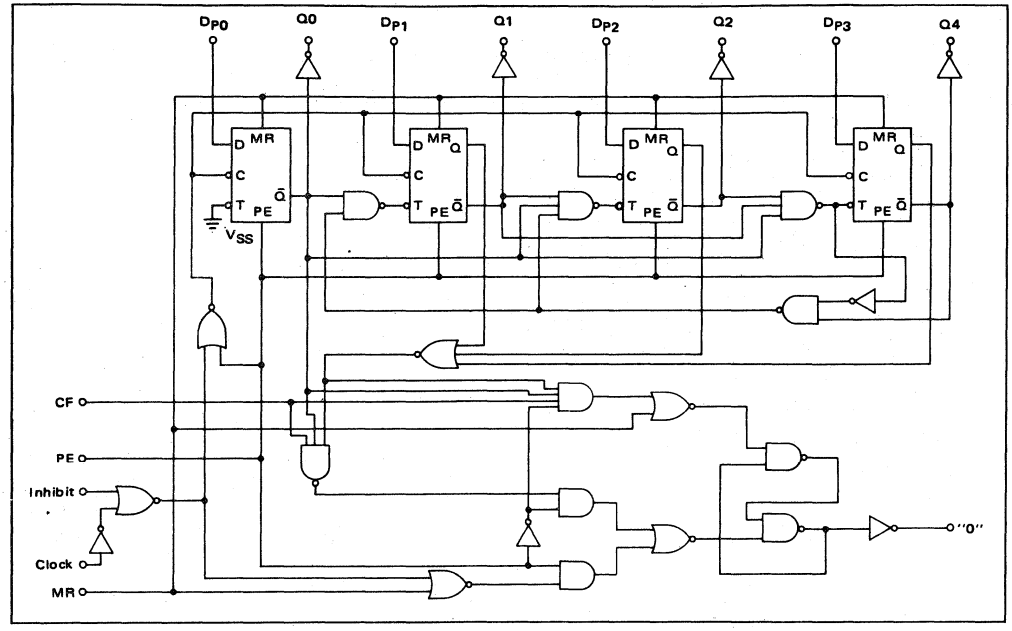


FIGURE 7 – MC14526B LOGIC DIAGRAM (Binary Divide-by-N Counter)

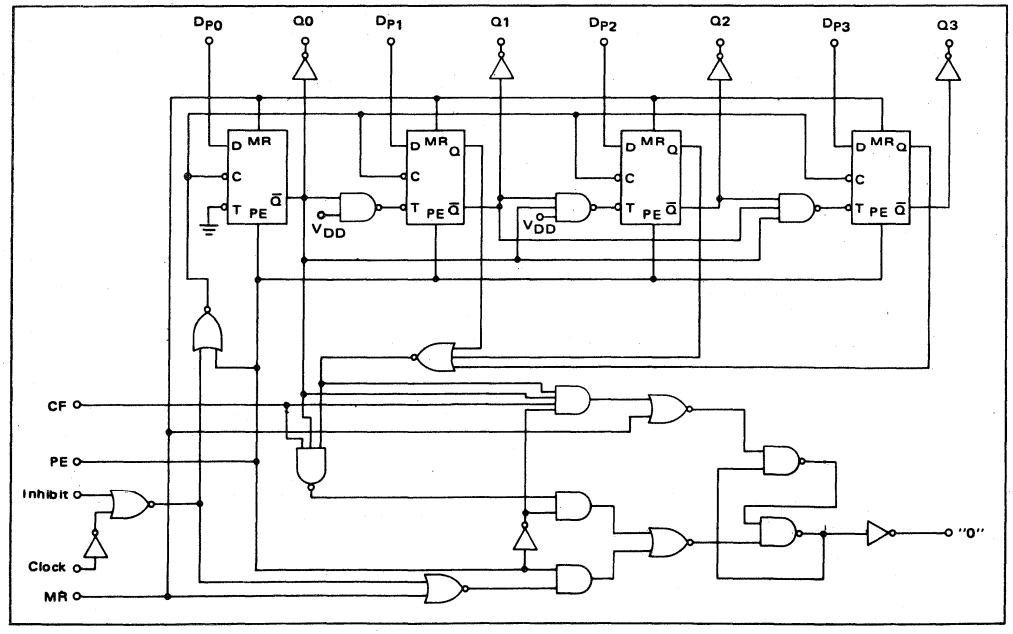
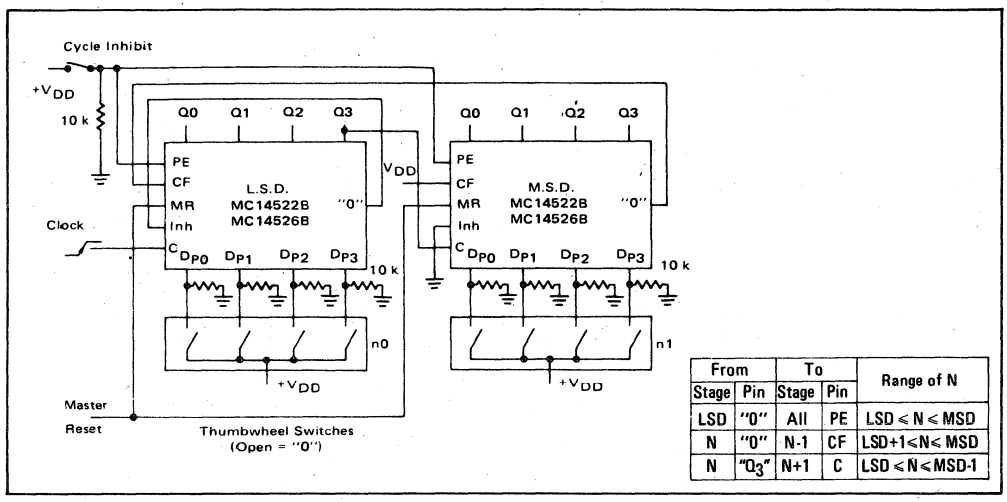
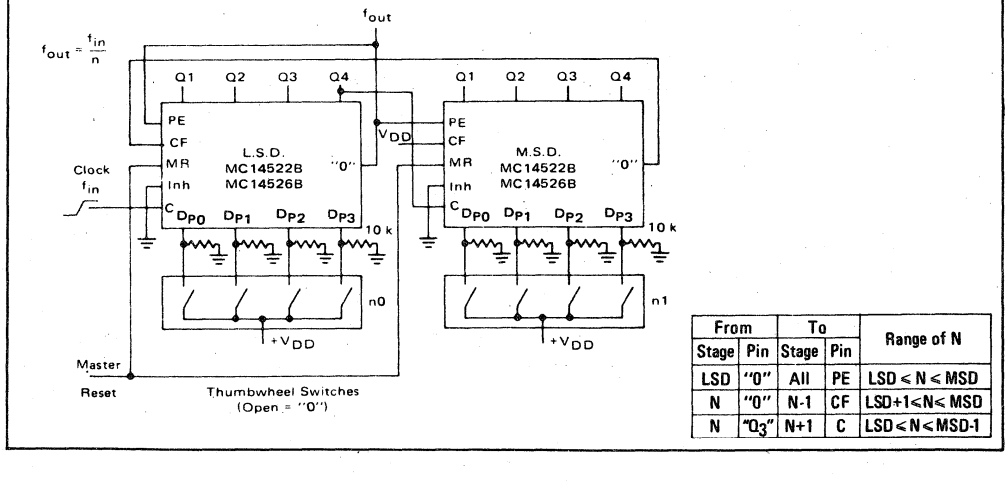


FIGURE 8 – 2-STAGE PROGRAMMABLE DOWN COUNTER
(One Cycle)



From		To		Range of N
Stage	Pin	Stage	Pin	
LSD	"0"	All	PE	LSD ≤ N ≤ MSD
N	"0"	N-1	CF	LSD+1≤N≤ MSD
N	"Q_3"	N+1	C	LSD ≤ N≤MSD-1

FIGURE 9 – 2-STAGE PROGRAMMABLE FREQUENCY DIVIDER



From		To		Range of N
Stage	Pin	Stage	Pin	
LSD	"0"	All	PE	LSD ≤ N ≤ MSD
N	"0"	N-1	CF	LSD+1≤N≤ MSD
N	"Q_3"	N+1	C	LSD≤N≤MSD-1

MOTOROLA

MCM14524

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

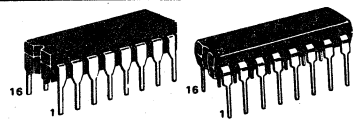
1024-BIT
(256 x 4)
READ ONLY MEMORY

1024-BIT READ ONLY MEMORY

The MCM14524 is a complementary MOS mask programmable Read Only Memory (ROM). This device is ordered as a factory special with its unique pattern specified by the user.

This ROM is organized in a 256 x 4-bit pattern. The contents of a specified address (< A0, A1, A2, A3, A4, A5, A6, A7 >) will appear at the four data outputs (B0, B1, B2, B3) following the negative going edge of the clock. When the clock goes high, the data present at the output will be latched. The memory Enable may be taken low asynchronously, forcing the data outputs low and resetting the output latches. This device finds application wherever low power or high noise immunity is a design consideration.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- Quiescent Current – 10 nA/package typical @ 5 Vdc
- Single Supply Operation – Either Positive or Negative
- Memory Enable Allows Expansion
- Output Latches Provide a Useful Storage Register
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.



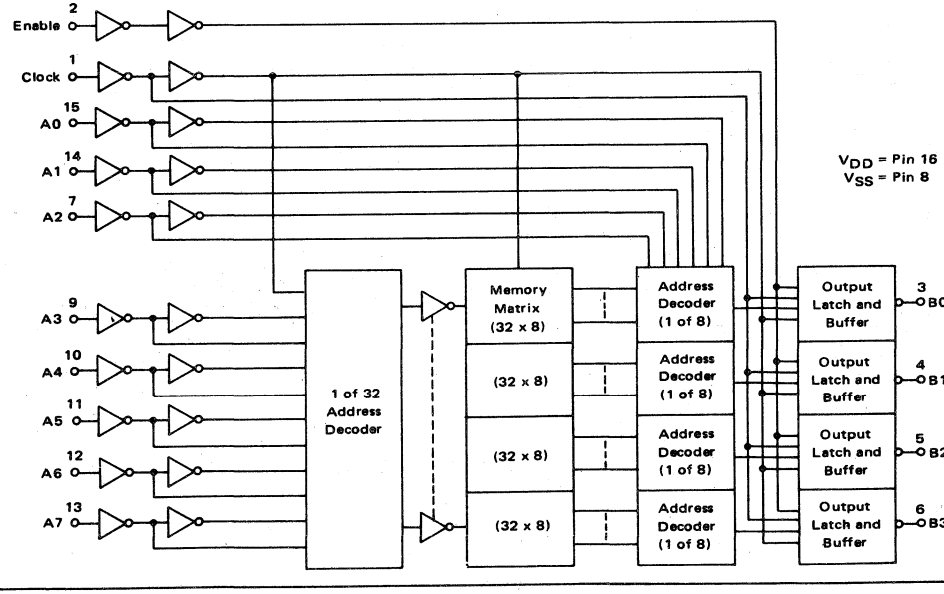
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.01	–	0	0.01	–	0.05	
"1" Level	V_{OH}	5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.99	–	14.99	15	–	14.95	–	
Noise Immunity #	V_{NL}									Vdc
(V_{out} ≤ 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
(V_{out} ≤ 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
(V_{out} ≤ 1.5 Vdc)		15	3.75	–	3.75	6.75	–	3.75	–	
(V_{out} ≥ 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≥ 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} ≥ 1.5 Vdc)		15	3.65	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7		-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	**±1.0**	–	±0.00001	**±1.0**	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.6\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (3.2\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (4.8\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50)\ V_{DD} f$$

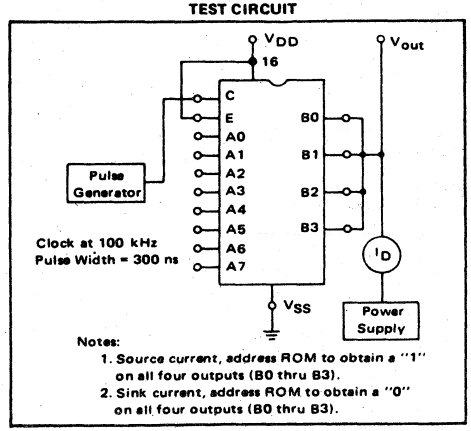
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH}, t_{THL} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH}, t_{THL} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Clock Read Access Delay Time	t_{acc_C}					ns
t_{acc_C} = (1.7 ns/pF) C_L + 1265 ns		5.0	–	1350	4000	
t_{acc_C} = (0.66 ns/pF) C_L + 517 ns		10	–	550	1600	
t_{acc_C} = (0.5 ns/pF) C_L + 325 ns		15	–	350	1200	
Enable Access Delay Time	$t_{acc_{En}}$					ns
$t_{acc_{En}}$ = (1.7 ns/pF) C_L + 160 ns		5.0	–	245	615	
$t_{acc_{En}}$ = (0.66 ns/pF) C_L + 77 ns		10	–	110	265	
$t_{acc_{En}}$ = (0.5 ns/pF) C_L + 50 ns		15	–	75	190	
Clock Pulse Width*	t_{WH}	5.0	450	150	–	ns
		10	165	55	–	
		15	125	35	–	
	t_{WL}	5.0	3600	1200	–	ns
		10	1425	475	–	
		15	1070	300	–	
Maximum Low Clock Pulse Width#	t_{WL}	5.0	2.0	10	–	ms
		10	0.9	3.0	–	
		15	0.1	0.3	–	
Address Setup-Time	$t_{su(A)}$	5.0	0	0	–	ns
		10	0	0	–	
		15	0	0	–	
Address Hold Time	$t_{h(A)}$	5.0	0	0	–	ns
		10	0	0	–	
		15	0	0	–	
Clock to Enable Setup Time	$t_{su(cl)}$	5.0	4275	1425	–	ns
		10	1725	575	–	
		15	1295	400	–	
Clock to Enable Hold Time	$t_{h(cl)}$	5.0	150	0	–	ns
		10	75	0	–	
		15	55	0	–	

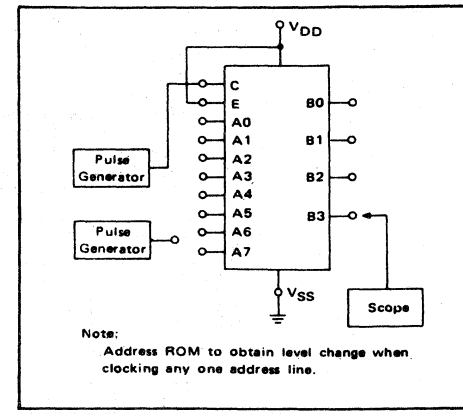
*The clock can remain high indefinitely with the data remaining latched.
#If clock stays low too long, the dynamically stored data will leak off and will have to be recalled.

FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



Notes:
1. Source current, address ROM to obtain a "1" on all four outputs (B0 thru B3).
2. Sink current, address ROM to obtain a "0" on all four outputs (B0 thru B3).

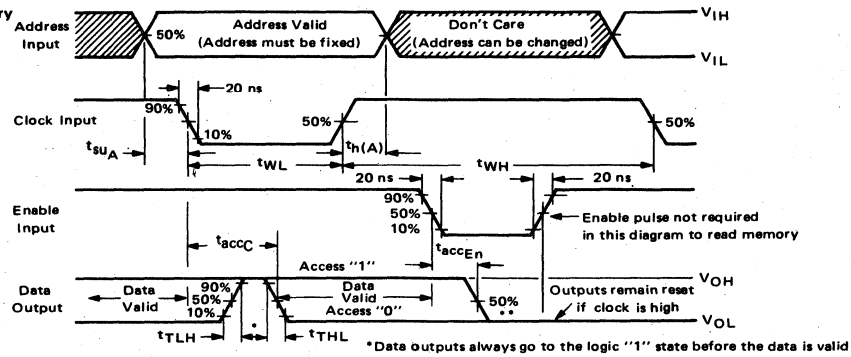
FIGURE 2 – SWITCHING TIME TEST CIRCUIT
(Refer to timing diagram)



Note:
Address ROM to obtain level change when clocking any one address line.

MEMORY READ CYCLE TIMING DIAGRAMS

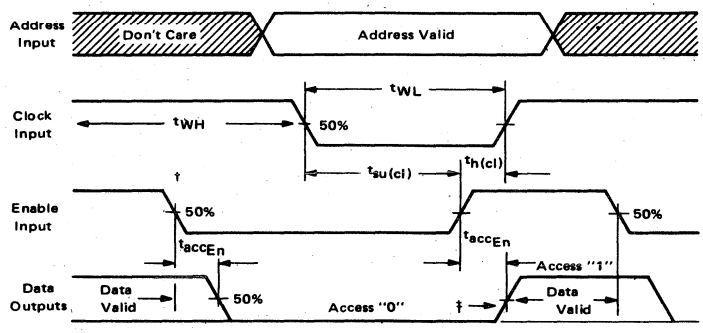
a) Using Clock to Read Memory



*Data outputs always go to the logic "1" state before the data is valid between accessing successive "0's"

**Outputs forced to "0" by Enable.

b) Using the Enable to Read Memory



† In this mode of operation, the negative going edge of Enable should occur on or before the clock negative edge.

‡The data outputs are valid without the logic "1" pulse occurring during the access cycle as shown in a) above.

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM14524, the customer may specify the content of the memory.

Address Inputs:

Words are numbered 0 through 255 and are addressed using sequential addressing of Address leads A0 through A7 with A0 as the least significant digit.

Logic "0" is defined as a "low" Address input (V_{IL}).
Logic "1" is defined as a "high" Address input (V_{IH}).

WORD \ ADDRESS	A7	A6	A5	A4	A3	A2	A1	A0
Word 0	0	0	0	0	0	0	0	0
Word 1	0	0	0	0	0	0	0	1
Word 2	0	0	0	0	0	0	1	0
Word 3	0	0	0	0	0	0	1	1
. .	.	.	.	.	.	.	.	.
. .	.	.	.	.	.	.	.	.
. .	.	.	.	.	.	.	.	.
Word 255	1	1	1	1	1	1	1	1

TRUTH TABLE

CLOCK	ENABLE	B0	B1	B2	B3
V_{DD} ⌐ V_{SS}	1	* ⟨Address⟩	* ⟨Address⟩	* ⟨Address⟩	* ⟨Address⟩
V_{SS} ⌐ V_{DD}	1	OUTPUT DATA LATCHES			
X	0	0	0	0	0

X = Don't Care

*Indicates contents of specified Address will appear at outputs as stated above.

BINARY TO HEXADECIMAL CONVERSION TABLE

BINARY WORD DESIRED	CARD CHARACTER
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	A
1 0 1 1	B
1 1 0 0	C
1 1 0 1	D
1 1 1 0	E
1 1 1 1	F

Two methods may be used to transmit the custom memory pattern to Motorola.

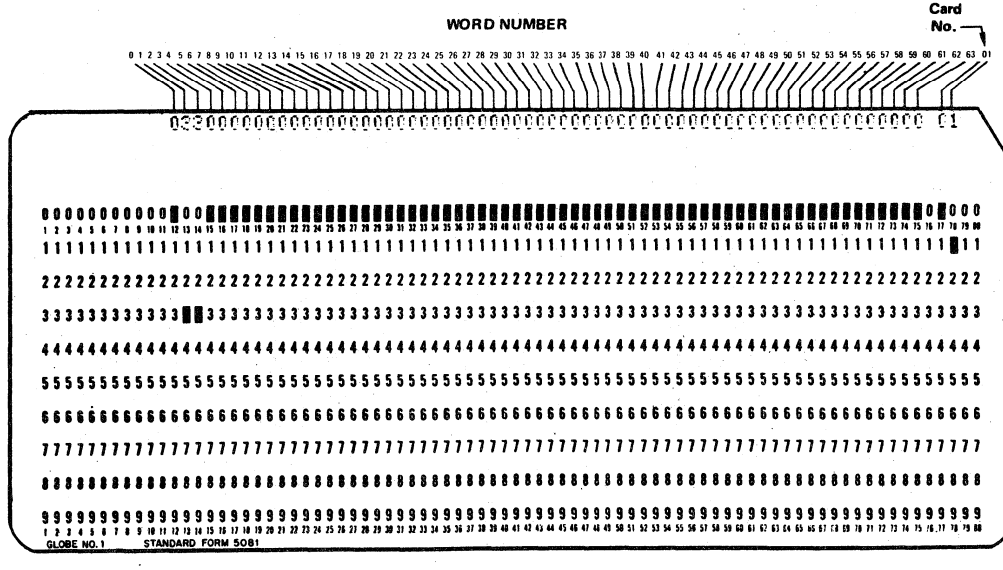
METHOD A: PUNCHED COMPUTER CARDS

A binary coded decimal equivalent of each desired output may be punched in standard computer cards (four cards are required for all 256 words) in numerical (word number) order. 64 words per card are punched in columns 12 thru 75 using the Binary to Hexadecimal conversion table. Columns 77 and 78 are used to number the cards, which must be in numerical order. Please use characters as shown in the table when punching computer cards.

ROM SAMPLE WORD PROGRAMMING FOR PUNCHED CARD

WORD NUMBER	ADDRESS INPUTS								SAMPLE WORD OUTPUTS				CARD CHARACTER
	A7	A6	A5	A4	A3	A2	A1	A0	B3	B2	B1	B0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	1	1	3
2	0	0	0	0	0	0	1	0	0	0	1	1	3
3	0	0	0	0	0	0	1	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1	1	0	1	0	A

Shown in columns 12 – 15 on card below



METHOD B: TRUTH TABLE

For customers who do not have access to punch cards, Motorola will accept Truth Tables. When filling out the table, use the 0 to F hexidecimal character in column "C".

CUSTOM PROGRAM for the MCM14524 Read Only Memory

WORD	C
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
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36	
37	
38	
39	
40	
41	
42	
43	
44	
45	
46	
47	
48	
49	
50	

WORD	C
51	
52	
53	
54	
55	
56	
57	
58	
59	
60	
61	
62	
63	
64	
65	
66	
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87	
88	
89	
90	
91	
92	
93	
94	
95	
96	
97	
98	
99	
100	
101	

WORD	C
102	
103	
104	
105	
106	
107	
108	
109	
110	
111	
112	
113	
114	
115	
116	
117	
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138	
139	
140	
141	
142	
143	
144	
145	
146	
147	
148	
149	
150	
151	
152	

WORD	C
153	
154	
155	
156	
157	
158	
159	
160	
161	
162	
163	
164	
165	
166	
167	
168	
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191	
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193	
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195	
196	
197	
198	
199	
200	
201	
202	
203	

WORD	C
204	
205	
206	
207	
208	
209	
210	
211	
212	
213	
214	
215	
216	
217	
218	
219	
220	
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245	
246	
247	
248	
249	
250	
251	
252	
253	
254	
255	

MOTOROLA

MC14526B

FOR COMPLETE DATA
SEE MC14522B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

BCD – MC14522B
Binary – MC14526B

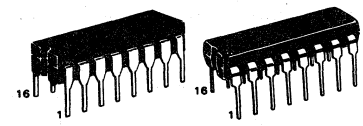
PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

The MC14522B BCD counter and the MC14526B binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure.

These devices are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Clock Inhibit input allows disabling of the pulse counting function.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds.
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition of Clock Inhibit
- 5.0 MHz Counting Rate
- Asynchronous Preset Enable
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

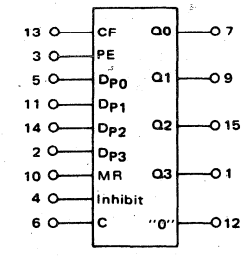
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLES

BOTH TYPES

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
↓	0	0	0	Count-1
X	1	0	0	No Count
1	↓	0	0	Count-1
X	X	1	0	Preset
X	X	X	1	Reset

MC14522B

Count	Output Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC14526B

Count	Output Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14527B

BCD RATE MULTIPLIER

The MC14527B BCD rate multiplier (DRM) provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten input pulses. This part may be used for arithmetic operations including multiplication and division. Typical applications include digital filters, motor speed control and frequency synthesizers.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance – 5.0 pF typical
- Internally Synchronous for High Speed
- Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and Cascade Inputs for Cascade Operation of Two or More DRMs
- "9" Output for the Parallel Enable Configuration and DRMs in Cascade
- Complementary Outputs
- Clear and Set to Nine Inputs

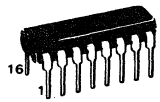
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD RATE MULTIPLIER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

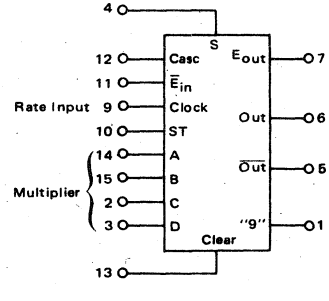
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS									OUTPUT LOGIC LEVEL NUMBER OF PULSES			
D	C	B	A	No. of Clock Pulses	$\overline{E}_{in}$	STROBE	CASCADE	CLEAR	SET	OUT	$\overline{OUT}$	E_{out}	"9"
0	0	0	0	10	0	0	0	0	0	0	1	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	–	–	–	–
X	X	X	X	10	0	1	0	0	0	0	1	1	1
X	X	X	X	10	0	0	1	0	0	1	0	1	1
1	X	X	X	10	0	0	0	1	0	10	10	1	0
0	X	X	X	10	0	0	0	1	0	0	1	1	0
X	X	X	X	10	0	0	0	0	1	0	1	0	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5 ☆	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.85 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.75 μA/kHz) f + I_{DD}							
		15	I_T = (2.6 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1.2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PHL},					ns
Clock to Out	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 115 ns		5.0	–	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	140	
Clock to Out	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 40 ns	t_{PHL}	5.0	–	125	250	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 32 ns		10	–	65	130	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 20 ns		15	–	45	90	
Clock to E_{out}	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 210 ns	t_{PHL}	5.0	–	295	590	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	–	85	170	
Clock to "9"	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns	t_{PHL}	5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	–	155	310	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Set or Clear to Out	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	–	380	760	
t_{PHL} = (0.66 ns/pF) C_L + 132 ns		10	–	165	330	
t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Cascade to Out	t_{PLH}					ns
t_{PHL} = (1.7 ns/pF) C_L + 40 ns		5.0	–	125	250	
t_{PHL} = (0.66 ns/pF) C_L + 32 ns		10	–	65	130	
t_{PHL} = (0.5 ns/pF) C_L + 20 ns		15	–	45	90	
Strobe to Out	t_{PLH}					ns
t_{PHL} = (1.7 ns/pF) C_L + 145 ns		5.0	–	230	260	
t_{PHL} = (0.66 ns/pF) C_L + 72 ns		10	–	105	210	
t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	140	
Clock Pulse Width	t_{WH}	5.0	500	250	–	ns
		10	200	110	–	
		15	150	80	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.0	1.2	MHz
		10	–	4.5	2.5	
		15	–	6.0	3.5	
Clock Pulse Rise and Fall Time	t_{TLH},	5.0	–	–	15	μs
	t_{THL}	10	–	–	15	
		15	–	–	15	
Set or Clear Pulse Width	t_{WH}	5.0	240	80	–	ns
		10	100	35	–	
		15	75	30	–	
Set Removal Time	t_{rem}	5.0	0	-20	–	ns
		10	0	-10	–	
		15	0	-7.5	–	
Enable In Setup Time	t_{su}	5.0	400	175	–	ns
		10	150	60	–	
		15	120	45	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – TEST CIRCUIT AND TIMING DIAGRAM

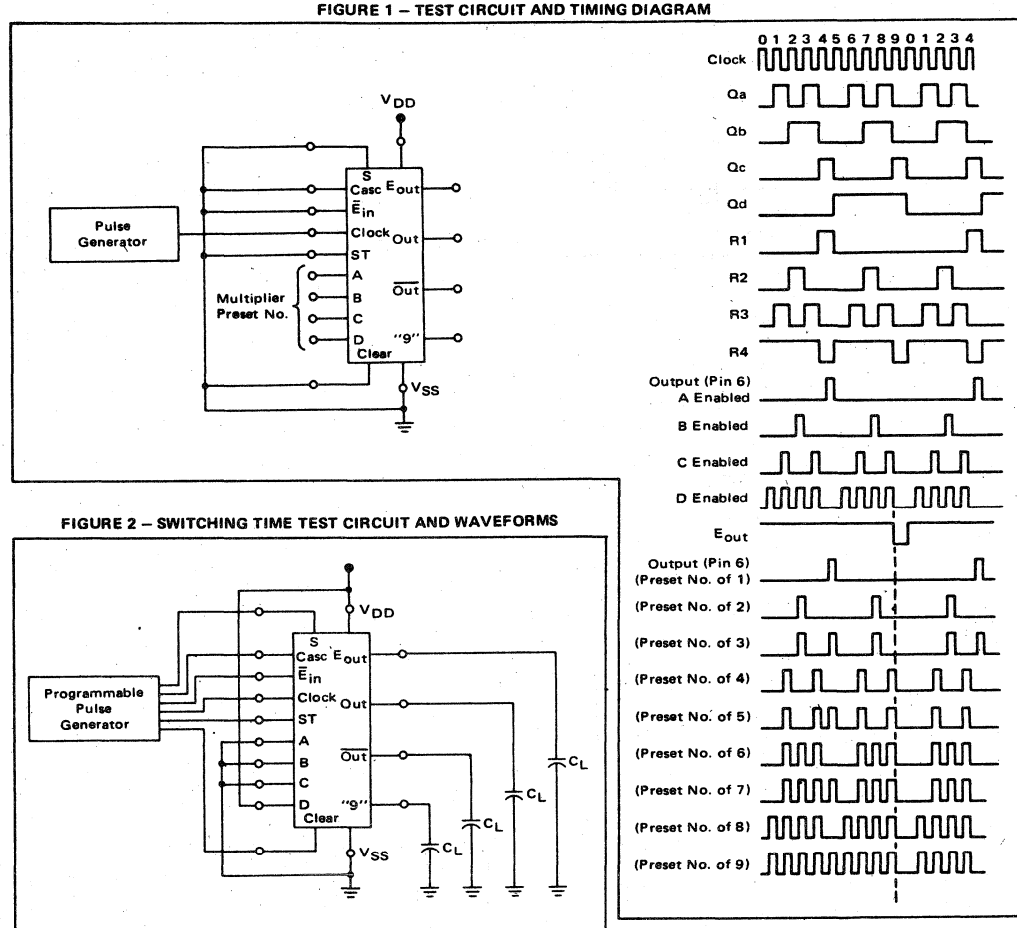


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

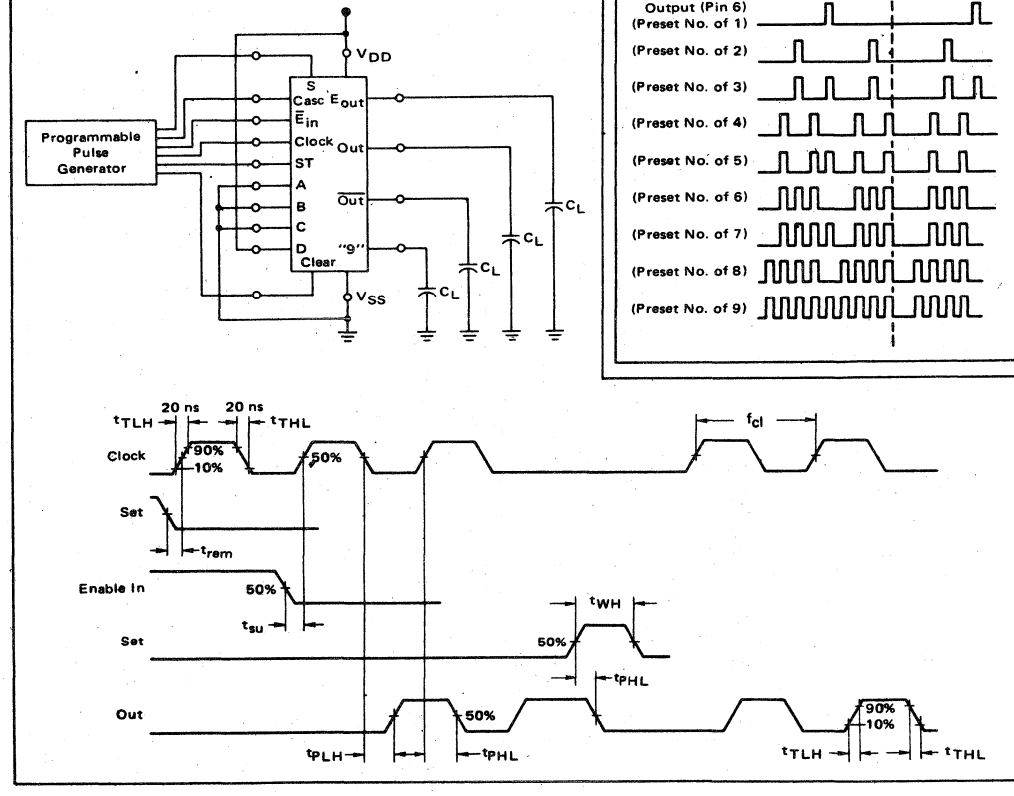
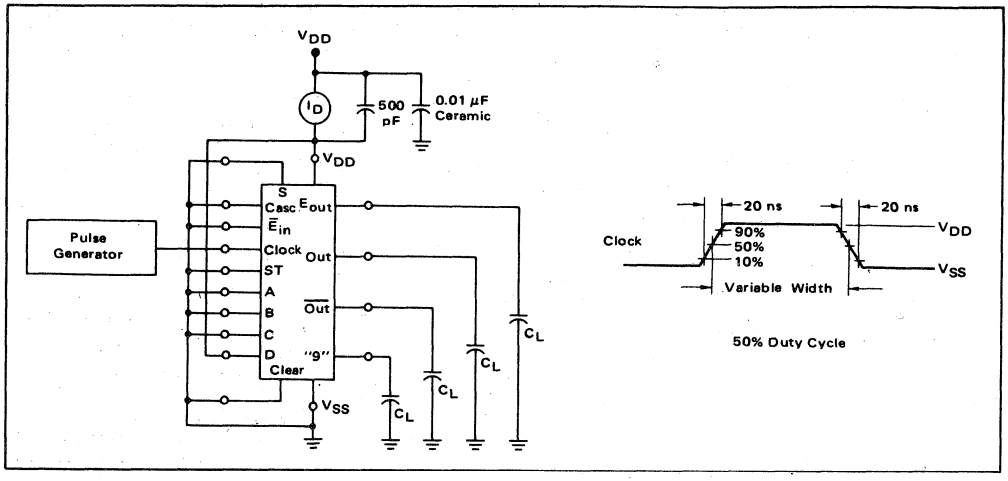


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



LOGIC DIAGRAM

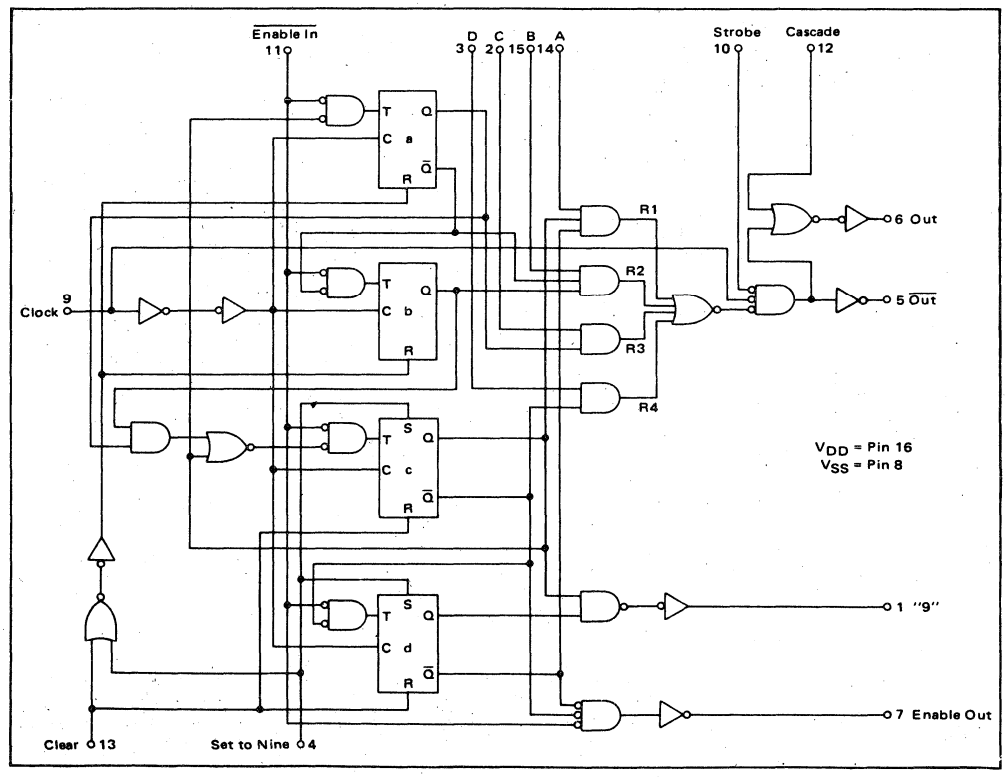
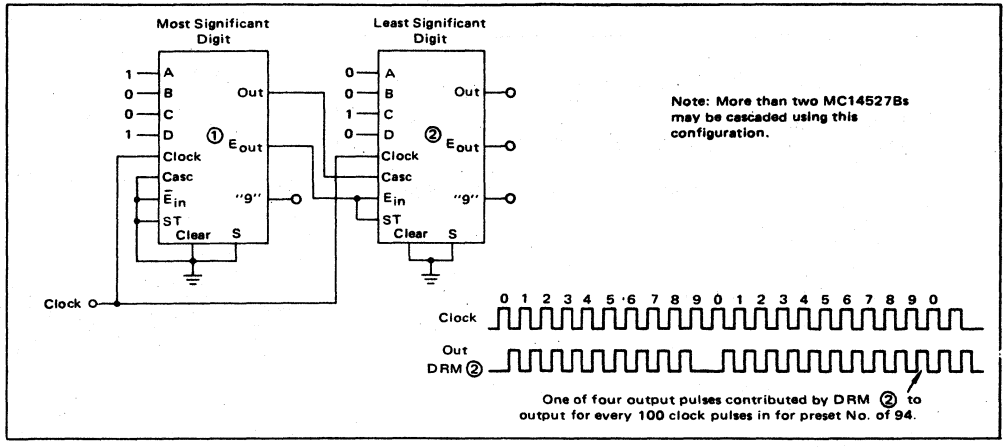


FIGURE 4 – TWO MC14527Bs IN CASCADE WITH PRESET NO. of 94



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14528B

CMOS MSI

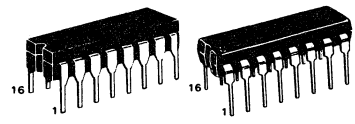
(LOW-POWER COMPLEMENTARY MOS)

DUAL RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

DUAL MONOSTABLE MULTIVIBRATOR

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

- Separate Reset Available
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- See MC14538B Data Sheet for Applications Requiring Precise Control of Output Pulse Width



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

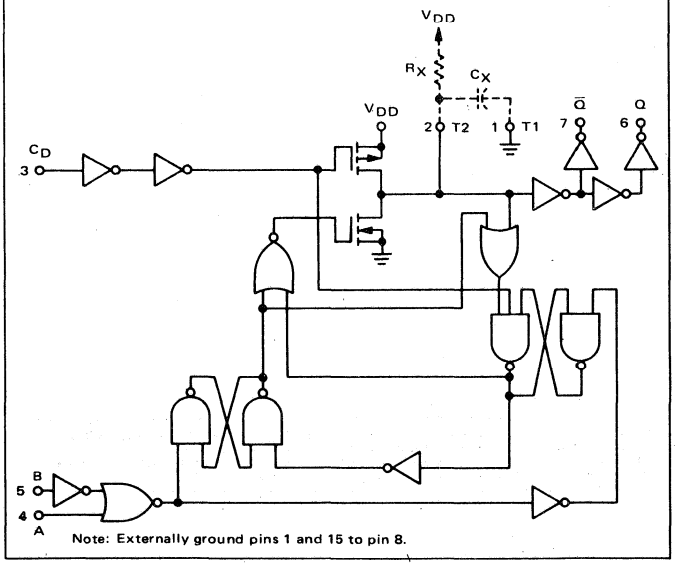
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

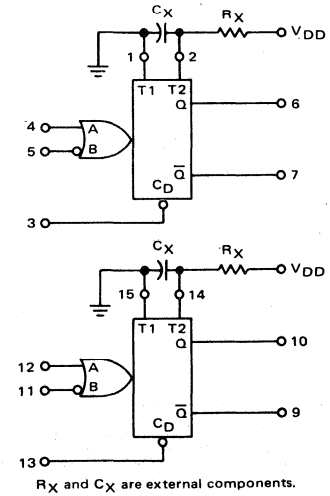
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM
(1/2 of Device Shown)



Note: Externally ground pins 1 and 15 to pin 8.

BLOCK DIAGRAM



R_X and C_X are external components.

V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
**Total Supply Current at an external load Capacitance (C_L) and at external timing capacitance (C_X), use the formula –	I_T	–	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2\times10^{-8} R_X C_X (V_{DD}-2)2f] \times 10^{-3}$ where: I_T in µA (per circuit), C_L and C_X in pF, R_X in megohms, V_{DD} in Vdc, f in kHz is input frequency.							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS** (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	–	–					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns				5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns				10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns				15	–	65	130	
Output Fall Time	t_{THL}	–	–					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns				5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns				10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns				15	–	40	80	
Turn-Off, Turn-On Delay Time – A or B to Q or Q	t_{PLH}, t_{PHL}	15	5.0					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 240 ns				5.0	–	325	650	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns				10	–	120	240	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns				15	–	90	180	
Turn-Off, Turn-On Delay Time – A or B to Q or Q	t_{PLH}, t_{PHL}	1000	10					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 620 ns				5.0	–	705	–	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns				10	–	290	–	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns				15	–	210	–	
Input Pulse Width – A or B	t_{WH}	15	5.0	5.0	150	70	–	ns
				10	75	30	–	
				15	55	30	–	
	t_{WL}	1000	10	5.0	–	70	–	ns
				10	–	30	–	
				15	–	30	–	
Output Pulse Width – Q or $\overline{Q}$ (For C_X < 0.01 μF use graph for appropriate V_{DD} level.)	t_W	15	5.0	5.0	–	550	–	ns
				10	–	350	–	
				15	–	300	–	
Output Pulse Width – Q or Q (For C_X > 0.01 μF use formula: $t_W = 0.2\ R_X\ C_X\ Ln\ [V_{DD} - V_{SS}]$)†	t_W	10,000	10	5.0	–	30	±15	μs
				10	–	50	±40	
				15	–	55	±40	
Pulse Width Match between Circuits in the same package	t1 - t2	10,000	10	5.0	–	6.0	25	%
				10	–	8.0	35	
				15	–	8.0	35	
Reset Propagation Delay – C_D to Q or Q	t_{PLH}, t_{PHL}	15	5.0	5.0	–	325	600	ns
				10	–	90	225	
				15	–	60	170	
		1000	10	5.0	–	1000	–	ns
				10	–	300	–	
				15	–	250	–	
Retrigger Time	t_{rr}	15	5.0	5.0	0	–	–	ns
				10	0	–	–	
				15	0	–	–	
		1000	10	5.0	0	–	–	ns
				10	0	–	–	
				15	0	–	–	
						Min		
External Timing Resistance	R_X	–	–	–	5.0	1000	1000	kΩ
External Timing Capacitance	C_X	–	–	–	No Limits			μF

**The formula given is for the typical characteristics only.

† R_X is in Ohms, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.

FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT

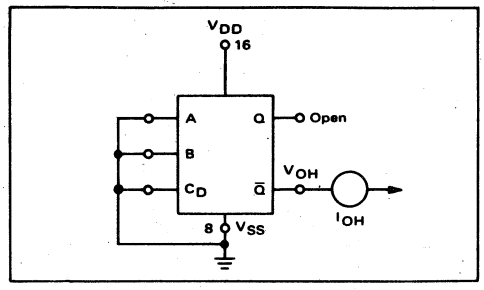


FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT

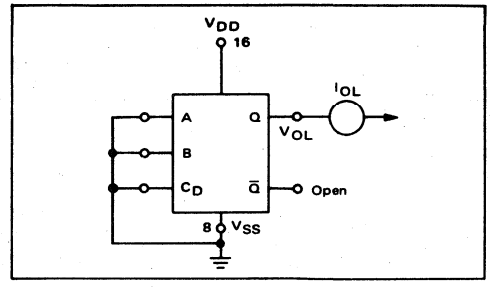


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

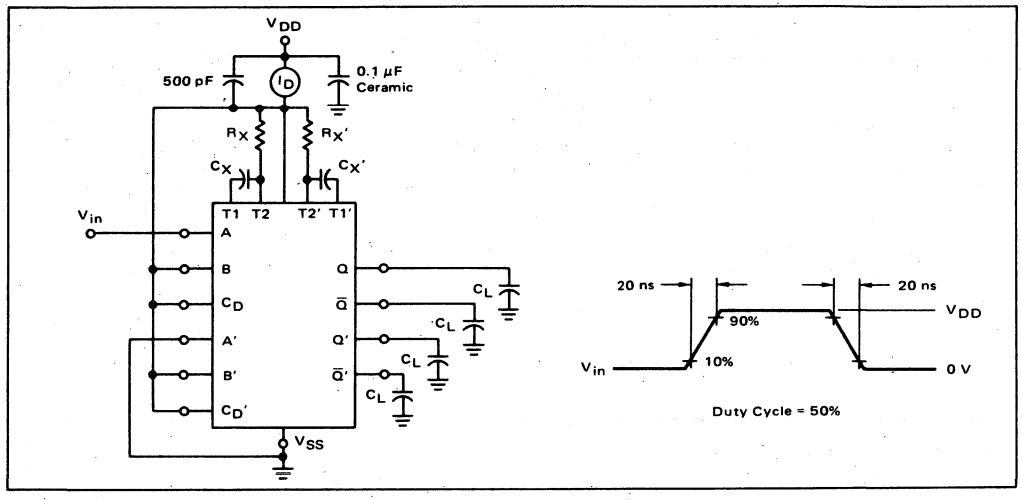
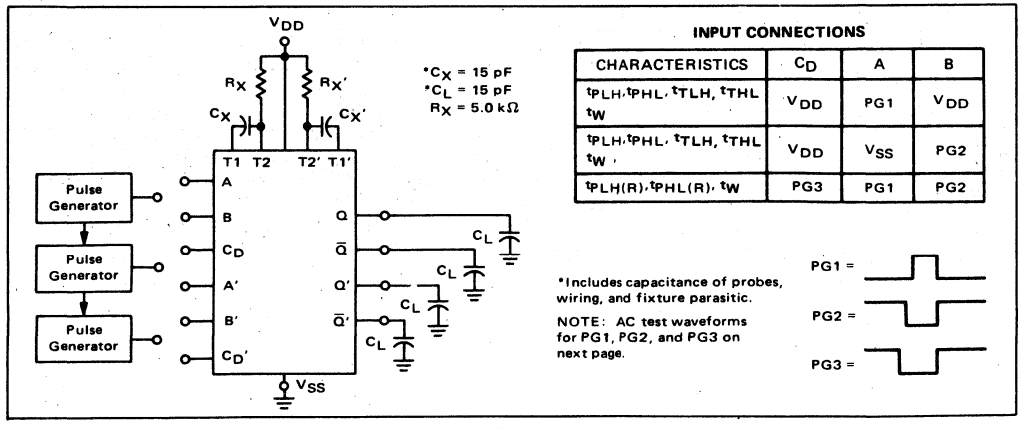


FIGURE 4 – AC TEST CIRCUIT



INPUT CONNECTIONS

CHARACTERISTICS	C_D	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} t_W	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} t_W	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_W	PG3	PG1	PG2

FIGURE 5 – AC TEST WAVEFORMS

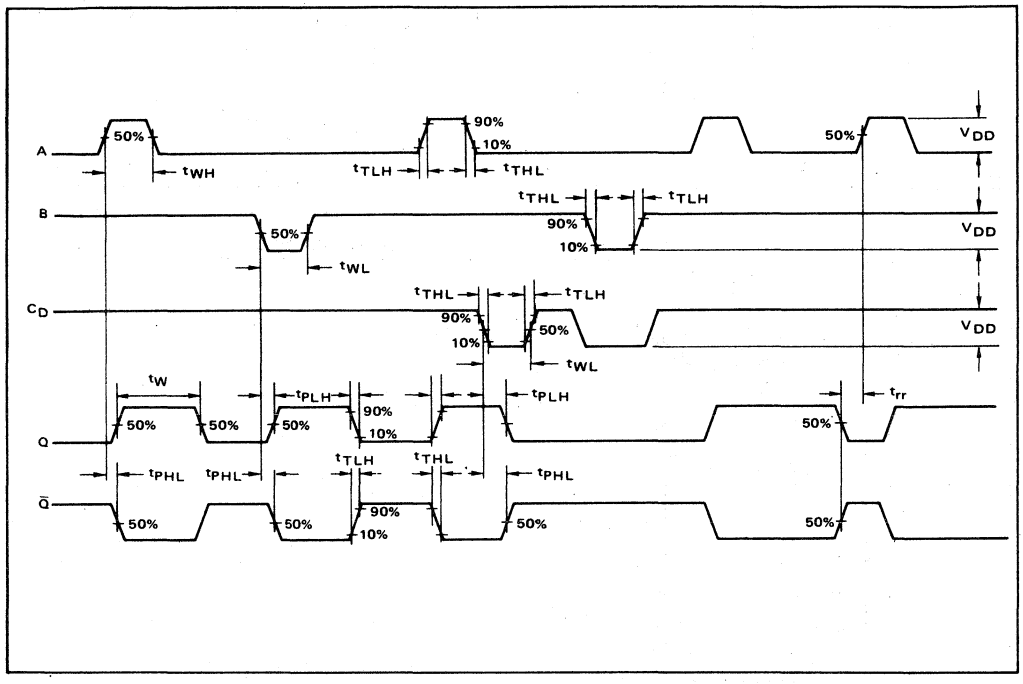


FIGURE 6 – NORMALIZED PULSE WIDTH versus TEMPERATURE

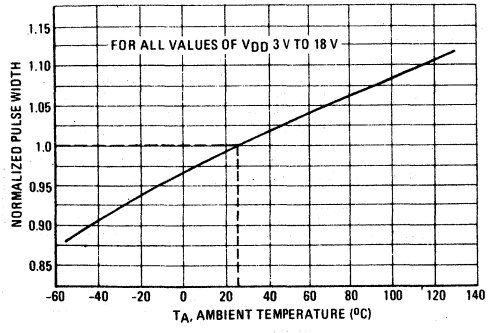
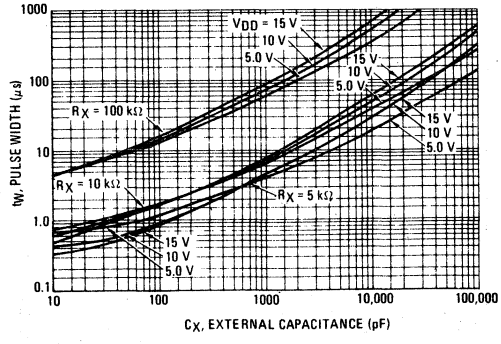


FIGURE 7 – PULSE WIDTH versus C_X



MOTOROLA

MC14529B

DUAL 4-CHANNEL ANALOG DATA SELECTOR

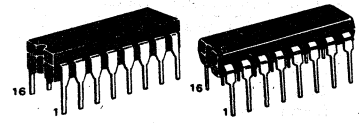
The MC14529B analog data selector is a dual 4-channel or single 8-channel device depending on the input coding. The device is suitable for digital as well as analog application, including various one-of-four and one-of-eight data selector functions. Since the device has bidirectional analog characteristics it can also be used as a dual binary to 1-of-4 or a binary to 1-of-8 decoder.

- Data Paths Are Bidirectional
- Quiescent Current = 1.0 nA/package typical @ 5.0 Vdc
- 10-MHz Operation (typical)
- 3-State Outputs
- Linear "On" Resistance
- "On" Resistance 120 Ohms typical @ 15 V
- Low Noise — 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-CHANNEL ANALOG DATA SELECTOR
OR
8-CHANNEL ANALOG DATA SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

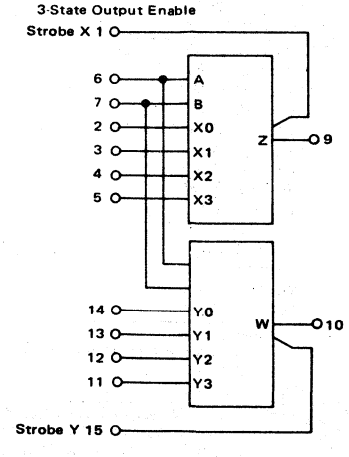
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	ϕ	ϕ	High Impedance		

ϕ = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the control inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} or V_{out} is not constrained to the range $V_{SS} \leq V_{in}$ or $V_{out} \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{SS} Vdc	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	1	V_{OL}	0.0	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0				10	–	0.05	–	0	0.05	–	0.05	
				15	–	0.05	–	0	0.05	–	0.05	
"1" Level		V_{OH}	0.0	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
				10	9.95	–	9.95	10	–	9.95	–	
V_{in} = 0 or V_{DD}				15	14.95	–	14.95	15	–	14.95	–	
Input Voltage # "0" Level	2	V_{IL}	0.0									Vdc
(V_O = 4.5 or 0.5 Vdc)				5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)				10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)				15	–	4.0	–	6.75	4.0	–	4.0	
(V_O = 0.5 or 4.5 Vdc) "1" Level		V_{IH}	0.0	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)				10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)				15	11	–	11	8.25	–	11	–	
Input Current (AL Device) Control		I_{in}	0.0	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device) Control		I_{in}	0.0	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	0.0									pF
Control				–	–	–	–	5.0	7.5	–	–	
Switch Input				–	–	–	–	8.0	–	–	–	
Switch Output				–	–	–	–	20	–	–	–	
Feed Through				–	–	–	–	0.3	–	–	–	
Quiescent Current (AL Device)	3	I_{DD}	–	5.0	–	1.0	–	0.001	1.0	–	60	µAdc
(Per Package)				10	–	1.0	–	0.002	1.0	–	60	
				15	–	2.0	–	0.003	2.0	–	120	
Quiescent Current (CL/CP Device)	3	I_{DD}	–	5.0	–	5.0	–	0.001	5.0	–	70	µAdc
(Per Package)				10	–	5.0	–	0.002	5.0	–	70	
				15	–	10	–	0.003	10	–	140	
"ON" Resistance (AL Device)	4,5,6	R_{ON}										Ohms
(V_C = V_{DD}, R_L = 10 kΩ)												
(V_{in} = +5.0 Vdc)			-5.0	5.0	–	400	–	200	480	–	640	
(V_{in} = –5.0 Vdc)					–	400	–	200	480	–	640	
(V_{in} = ±0.25 Vdc)					–	400	–	190	480	–	640	
(V_{in} = +7.5 Vdc)			-7.5	7.5	–	240	–	160	270	–	400	
(V_{in} = –7.5 Vdc)					–	240	–	160	270	–	400	
(V_{in} = ±0.25 Vdc)					–	240	–	120	270	–	400	
(V_{in} = +10 Vdc)			0	10	–	400	–	180	480	–	640	
(V_{in} = +0.25 Vdc)					–	400	–	180	480	–	640	
(V_{in} = +5.6 Vdc)					–	400	–	220	480	–	640	
(V_{in} = +15 Vdc)			0	15	–	250	–	180	270	–	400	
(V_{in} = +0.25 Vdc)					–	250	–	180	270	–	400	
(V_{in} = +9.3 Vdc)					–	250	–	215	270	–	400	
"ON" Resistance (CL/CP Device)	4,5,6	R_{ON}										Ohms
(V_C = V_{DD}, R_L = 10 kΩ)												
(V_{in} = +5.0 Vdc)			-5.0	5.0	–	410	–	200	480	–	560	
(V_{in} = –5.0 Vdc)					–	410	–	200	480	–	560	
(V_{in} = +0.25 Vdc)					–	410	–	190	480	–	560	
(V_{in} = +7.5 Vdc)			-7.5	7.5	–	250	–	160	270	–	350	
(V_{in} = –7.5 Vdc)					–	250	–	160	270	–	350	
(V_{in} = ±0.25 Vdc)					–	250	–	120	270	–	350	
(V_{in} = +10 Vdc)			0	10	–	410	–	180	480	–	560	
(V_{in} = +0.25 Vdc)					–	410	–	180	480	–	560	
(V_{in} = +5.6 Vdc)					–	410	–	220	480	–	560	
(V_{in} = +15 Vdc)			0	15	–	250	–	180	270	–	350	
(V_{in} = +0.25 Vdc)					–	250	–	180	270	–	350	
(V_{in} = +9.3 Vdc)					–	250	–	215	270	–	350	
Δ"ON" Resistance	–	ΔR_{ON}										Ohms
Between any 2 circuits in a common package												
(V_{in} = ±5.0 Vdc)			-5.0	5.0	–	–	–	15	–	–	–	
(V_{in} = ±7.5 Vdc)			-7.5	7.5	–	–	–	10	–	–	–	

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device
*T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

SWITCHING CHARACTERISTICS (T_A = 25°C)

Characteristic	Figure	Symbol	V_{SS}	V_{DD}	Typical All Types	Maximum AL Device	Maximum CL/CP Device	Unit
V_{in} to V_{out} Propagation Delay Time (C_L = 50 pF, R_L = 1.0 kΩ)	7	t_{PLH},t_{PHL}	0.0	5.0	20	40	60	ns
				10	10	20	30	
				15	8.0	15	25	
Propagation Delay Time, Control to Output, V_{in} = V_{DD} or V_{SS} (V_{in} ≤ 10 Vdc, C_L = 50 pF, R_L = 1.0 kΩ)	8	t_{PHL},t_{PLH}	0.0	5.0	200	400	600	ns
				10	80	160	240	
				15	50	120	180	
Crosstalk, Control to Output (C_L = 50 pF, R_L = 1.0 kΩ) R_{out} = 10 kΩ)	9	–	0.0	5.0	5.0	–	–	mV
				10	5.0	–	–	
				15	5.0	–	–	
Maximum Control Input Pulse Frequency (C_L = 50 pF, R_L = 1.0 kΩ)	10	–	0.0	5.0	5.0	–	–	MHz
				10	10	–	–	
				15	12	–	–	
Noise Voltage (f = 100 Hz)	11,12	–	0.0	5.0	24	–	–	nV/√Cycle
				10	25	–	–	
				15	30	–	–	
(f = 100 kHz)				5.0	12	–	–	
				10	12	–	–	
				15	15	–	–	
Sine Wave (Distortion) (V_{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	–	–	-5.0	5.0	0.36	–	–	%
Input/Output Leakage Current	–	–						nA
(V_{in} = +5.0 Vdc, V_{out} = -5.0 Vdc)			-5.0	5.0	±0.001	±125	±125	
(V_{in} = -5.0 Vdc, V_{out} = +5.0 Vdc)			-5.0	5.0	±0.001	±125	±125	
(V_{in} = +7.5 Vdc, V_{out} = -7.5 Vdc)			-7.5	7.5	±0.0015	±250	±250	
(V_{in} = -7.5 Vdc, V_{out} = +7.5 Vdc)			-7.5	7.5	±0.0015	±250	±250	
Insertion Loss (V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc, f = 1.0 MHz, $I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$	–	–	-5.0	5.0				dB
(R_L = 1.0 kΩ)					2.0	–	–	
(R_L = 10 kΩ)					0.8	–	–	
(R_L = 100 kΩ)					0.25	–	–	
(R_L = 1.0 MΩ)					0.01	–	–	
Bandwidth (-3 dB) (V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc)	–	BW	-5.0	5.0				MHz
(R_L = 1.0 kΩ)					35	–	–	
(R_L = 10 kΩ)					28	–	–	
(R_L = 100 kΩ)					27	–	–	
(R_L = 1.0 MΩ)					26	–	–	
Feedthrough and Crosstalk ($20 \log_{10} \frac{V_{out}}{V_{in}} = -50$ dB)	–	–	-5.0	5.0				kHz
(R_L = 1.0 kΩ)					850	–	–	
(R_L = 10 kΩ)					100	–	–	
(R_L = 100 kΩ)					12	–	–	
(R_L = 1.0 MΩ)					1.5	–	–	

FIGURE 1 - OUTPUT VOLTAGE TEST CIRCUIT

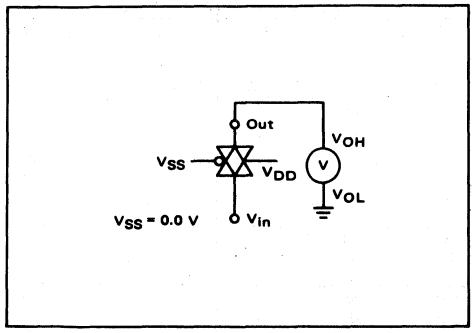


FIGURE 2 – NOISE IMMUNITY TEST CIRCUIT

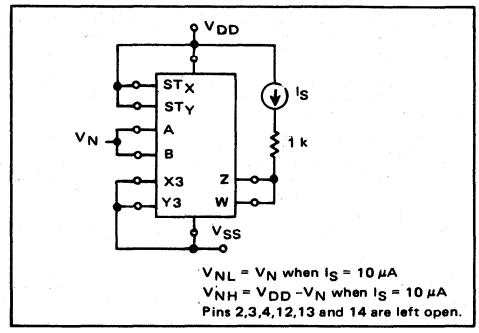


FIGURE 3 – QUIESCENT POWER DISSIPATION TEST CIRCUIT

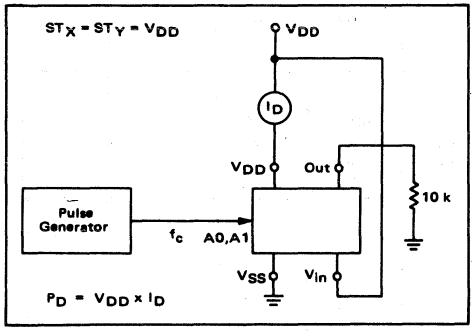
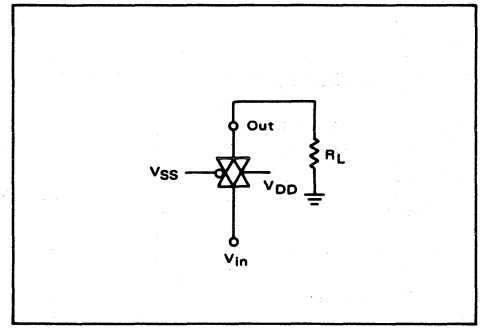


FIGURE 4 – R_{ON} CHARACTERISTICS TEST CIRCUIT



TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 5

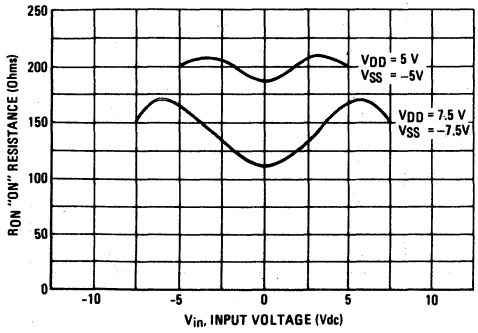


FIGURE 6

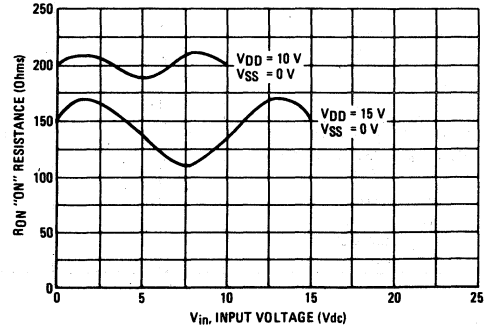


FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

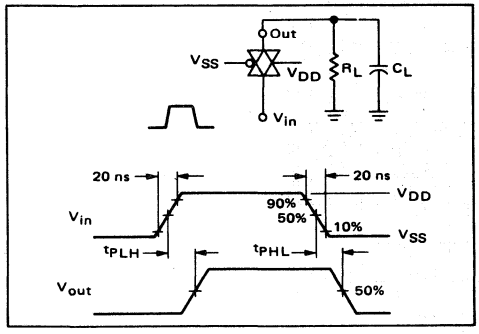


FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

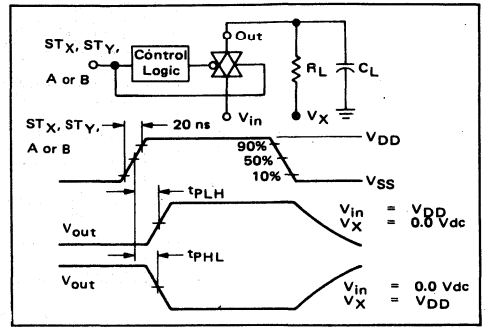


FIGURE 9 – CROSSTALK TEST CIRCUIT

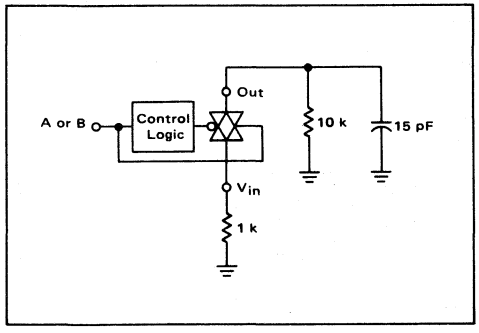


FIGURE 10 – FREQUENCY RESPONSE TEST CIRCUIT

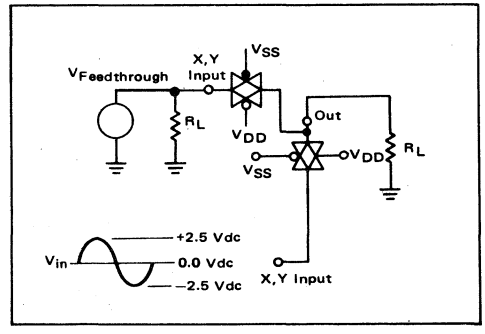


FIGURE 11 – NOISE VOLTAGE TEST CIRCUIT

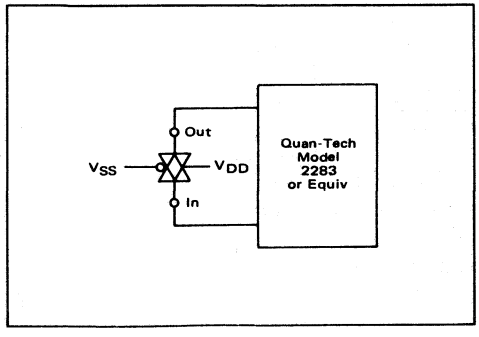


FIGURE 12 – TYPICAL NOISE CHARACTERISTICS

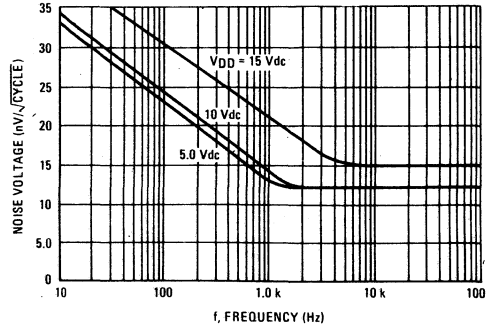
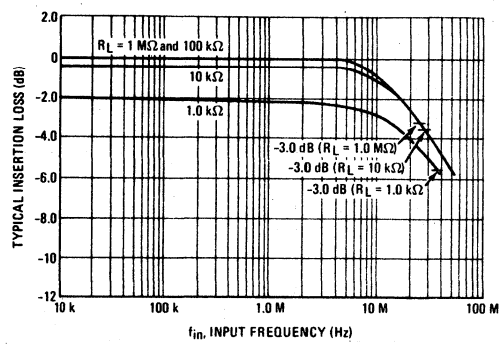
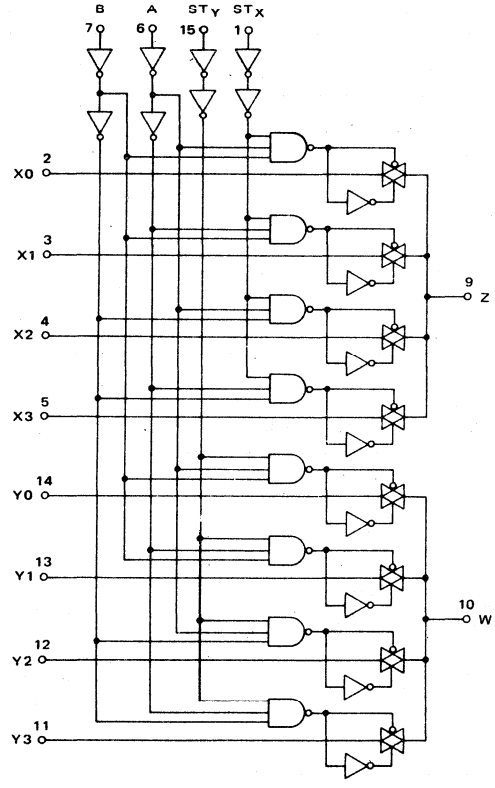


FIGURE 13 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MOTOROLA

MC14530B

CMOS SSI

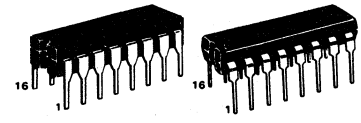
(LOW-POWER COMPLEMENTARY MOS)

DUAL 5-INPUT MAJORITY LOGIC GATE

DUAL 5-INPUT MAJORITY LOGIC GATE

The MC14530B dual five-input majority logic gate is constructed with P-channel and N-channel enhancement mode devices in a single monolithic structure. Combinational and sequential logic expressions are easily implemented with the majority logic gate, often resulting in fewer components than obtainable with the more basic gates. This device can also provide numerous logic functions by using the W and some of the logic (A thru E) inputs as control inputs.

- Single Supply Operation – Positive or Negative
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Input Impedance = 10^{12} ohms typical
- High Fanout > 50
- Diode Protection on Inputs
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

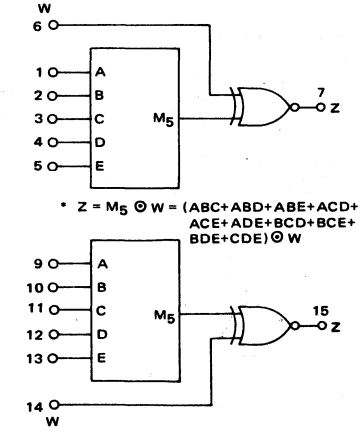
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC TABLE

INPUTS A B C D E	W	Z
For all combinations of inputs where three or more inputs are logical "0".	0	1
	1	0
For all combinations of inputs where three or more inputs are logical "1".	0	0
	1	1

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must be tied to an appropriate logic level (e.g., V_{SS} or V_{DD}).

BLOCK DIAGRAM



* $Z = M_5 \odot W = (ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE) \odot W$

*M_5 is a logical "1" if any three or more inputs are logical "1".

$\odot \equiv$ Exclusive NOR $\equiv \overline{\text{Exclusive OR}}$

TRUTH TABLE

M_5	W	Z
0	0	1
0	1	0
1	0	0
1	1	1

V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.5 or 1.5 Vdc)		5.0	–	1.2	–	2.25	1.25	–	1.15	
(V_O = 7.0 or 3.0 Vdc)		10	–	2.5	–	4.50	2.5	–	2.4	
(V_O = 10.5 or 4.5 Vdc)		15	–	3.0	–	6.75	3.0	–	2.9	
"1" Level	V_{IH}									
(V_O = 1.5 or 3.5 Vdc)		5.0	3.85	–	3.75	2.75	–	3.75	–	Vdc
(V_O = 3.0 or 7.0 Vdc)		10	7.6	–	7.5	5.50	–	7.5	–	
(V_O = 4.5 or 10.5 Vdc)		15	12.1	–	12	8.25	–	12	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.50 μA/kHz) f + I_{DD}							
		15	I_T = (2.25 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination. Standard family noise margin specification is met for any one input tested at a time.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$$

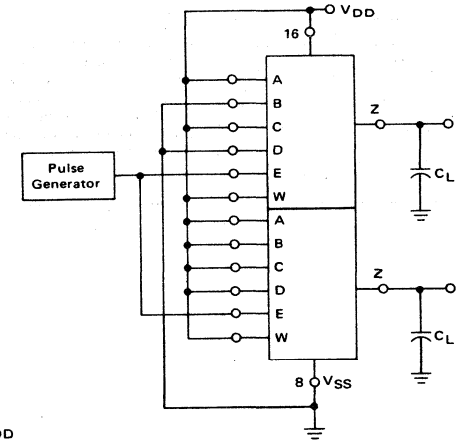
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and fin kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

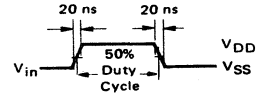
SWITCHING CHARACTERISTICS* (C_L = to pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
A, C, W = V_{DD}; B, E = Gnd; D = Pulse Generator						
t_{PLH} = (1.7 ns/pF) C_L + 290 ns		5.0	–	375	960	
t_{PLH} = (0.66 ns/pF) C_L + 127 ns		10	–	160	400	
t_{PLH} = (0.5 ns/pF) C_L + 85 ns		15	–	110	300	
t_{PHL} = (1.7 ns/pF) C_L + 345 ns	t_{PHL}	5.0	–	430	1200	ns
t_{PHL} = (0.66 ns/pF) C_L + 162 ns		10	–	195	540	
t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	120	410	
A, B, C, D, E = Pulse Generator; W = V_{DD}	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 170 ns		5.0	–	255	640	
t_{PLH} = (0.66 ns/pF) C_L + 87 ns		10	–	120	300	
t_{PLH} = (0.5 ns/pF) C_L + 60 ns		15	–	85	210	
t_{PHL} = (1.7 ns/pF) C_L + 195 ns	t_{PHL}	5.0	–	280	750	ns
t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	330	
t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	250	
A, B, C, D, E = Gnd; W = Pulse Generator	t_{PLH},					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 145 ns	t_{PHL}	5.0	–	230	575	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 72 ns		10	–	105	265	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 50 ns		15	–	75	190	

*The formula given is for the typical characteristics only.

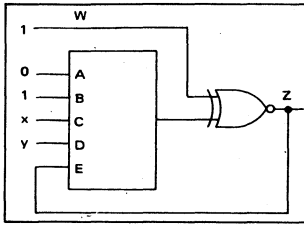
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM





SEQUENTIAL LOGIC APPLICATIONS

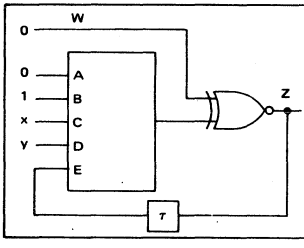
COINCIDENT FLIP-FLOP



x	y	Q_{n+1}
0	0	0
0	1	Q
1	0	Q
1	1	1

A flip-flop that will change only when both inputs agree.

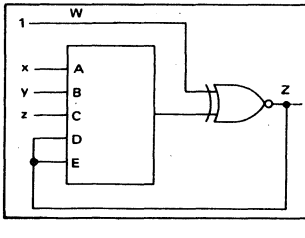
ASTABLE MULTIVIBRATOR



x	y	Q_{n+1}
0	0	1
0	1	2τ
1	0	2τ
1	1	0

A flip-flop with three output conditions, where the third state is in oscillation between "1" and "0". The period of oscillation is twice the delay of the gate and the feedback element.

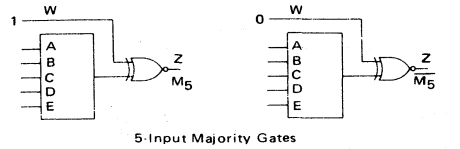
COINCIDENT FLIP-FLOP



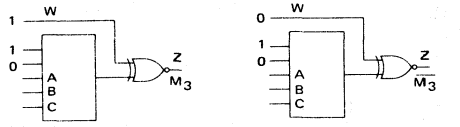
x	y	z	Q_{n+1}
0	0	0	0
0	0	1	Q_n
0	1	0	Q_n
0	1	1	Q_n
1	0	0	Q_n
1	0	1	Q_n
1	1	0	Q_n
1	1	1	1

The flip-flop changes state only when all "1's" or all "0's" are entered. This configuration may be extended by cascading M_5 gates to cover n-inputs where all inputs must be "1's" or "0's" before the output will change. As an example, this configuration is useful for controlling an n-stage up/down counter that is to cycle from a minimum to maximum count and back again without flipping over (from all "1's" to all "0's".)

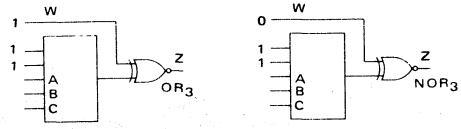
BASIC COMBINATIONAL FUNCTIONS



5-Input Majority Gates

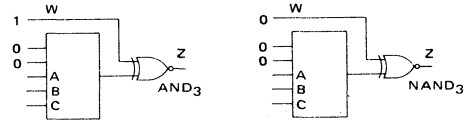


3-Input Majority Gates



3-Input OR Gate

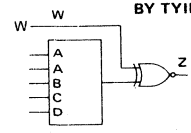
3 Input NOR Gate



3 Input AND Gate

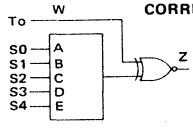
3-Input NAND Gate

DOUBLING THE WEIGHT OF INPUT VARIABLE A BY TYING IT TO ANY TWO INPUTS



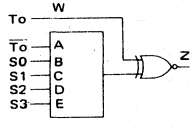
(AB+AC+AD+BCD) ⊙ W

CORRELATION OF MULTIPLE SAMPLES WITH A TEST BIT

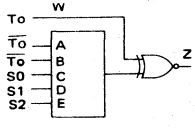


Correlation of 60%, 80%, 100%

The gate will have a "1" output if the test bit To matches or correlates with 3, 4 or 5 of the sample bits S0-S4.



Correlation of 75%, 100%.



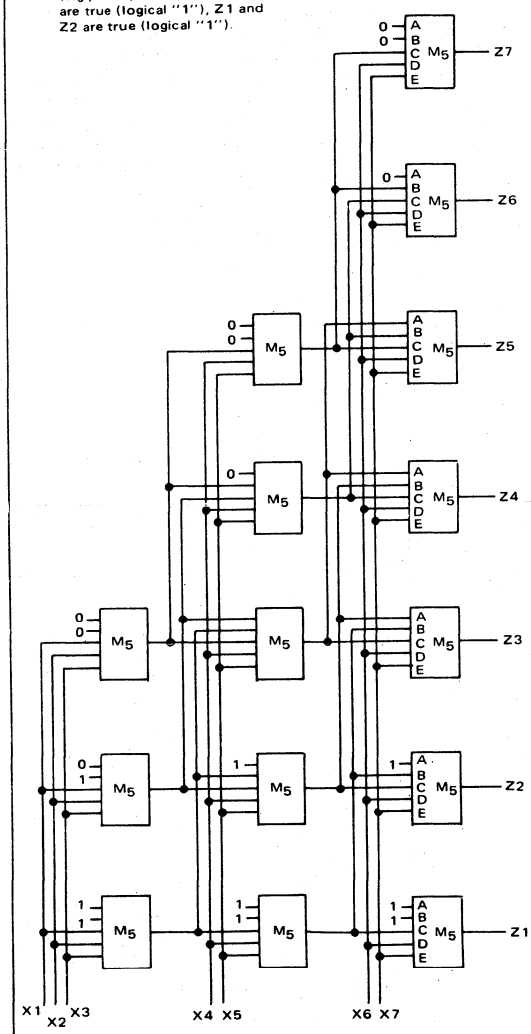
Correlation of 100%

5-INPUT MAJORITY LOGIC GATE APPLICATIONS

Each package labeled M_5 is a single majority logic gate using five inputs, A thru E, and one output Z.

1. Majority Logic Gate Array yielding the symetric function of 1 thru 7 variables true, out of 7 input variables (X1 . . . X7)

(e.g., if any two-input variables are true (logical "1"), Z1 and Z2 are true (logical "1").



MOTOROLA

MC14531B

CMOS MSI

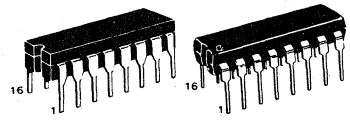
(LOW-POWER COMPLEMENTARY MOS)

12-BIT PARITY TREE

12-BIT PARITY TREE

The MC14531B 12-bit parity tree is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of 12 data-bit inputs (D0 thru D11), and even or odd parity selection input (W) and an output (Q). The parity selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even or odd number of ones, respectively. Words of greater than 12-bits can be accommodated by cascading other MC14531B devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple input summer without carries.

- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Quiescent Current – 5.0 nA/package typical @ 5 Vdc
- Variable Word Length
- Diode Protection on All Inputs



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

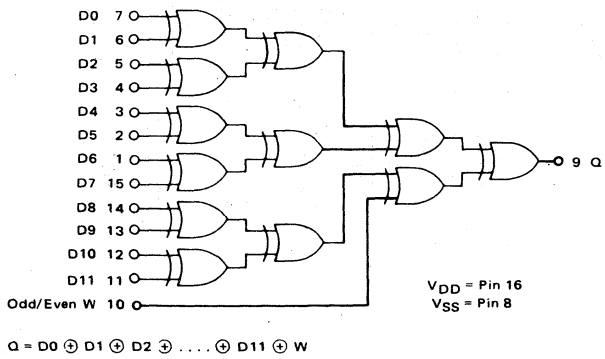
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



$Q = D0 \oplus D1 \oplus D2 \oplus \ldots \oplus D11 \oplus W$

TRUTH TABLE

INPUTS								OUTPUT
W	D11	D10	···	D2	D1	D0	DECIMAL (OCTAL) EQUIVALENT	Q*
0	0	0	···	0	0	0	0 (0)	0
0	0	0	···	0	0	1	1 (1)	1
0	0	0	···	0	1	0	2 (2)	1
0	0	0	···	0	1	1	3 (3)	0
0	0	0	···	1	0	0	4 (4)	1
0	0	0	···	1	0	1	5 (5)	0
0	0	0	···	1	1	0	6 (6)	0
0	0	0	···	1	1	1	7 (7)	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	···	0	0	0	8184 (17770)	0
1	1	1	···	0	0	1	8185 (17771)	1
1	1	1	···	0	1	0	8186 (17772)	1
1	1	1	···	0	1	1	8187 (17773)	0
1	1	1	···	1	0	0	8188 (17774)	1
1	1	1	···	1	0	1	8189 (17775)	0
1	1	1	···	1	1	0	8190 (17776)	0
1	1	1	···	1	1	1	8191 (17777)	1

*0 = Even Parity
1 = Odd Parity

Note: May redefine to suit application by manipulating W and/or other available D's.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.25 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.50 µA/kHz) f + I_{DD}							
		15	I_T = (0.75 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

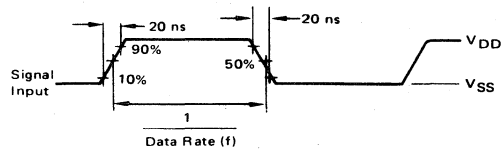
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Data to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 355 ns		5.0	–	440	1320	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 142 ns		10	–	175	525	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	120	360	
Odd/Even to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 165 ns		5.0	–	250	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	210	

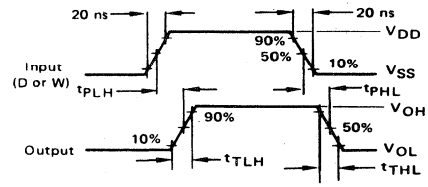
*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORM



f in respect to system clock

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



MOTOROLA

MC14532B

8-BIT PRIORITY ENCODER

The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (E_{in}) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E_{out}).

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Low Input Capacitance – 5.0 pF typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range -- AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUT									OUTPUT				
E_{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

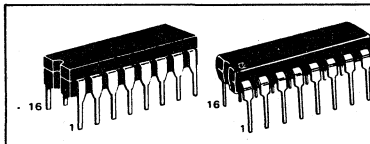
X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT PRIORITY ENCODER



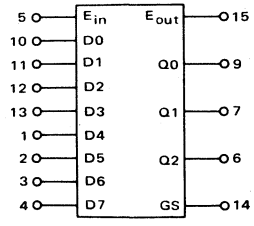
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.74 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.65 μA/kHz) f + I_{DD}							
		15	I_T = (5.73 μA/kHz) f + I_{DD}							

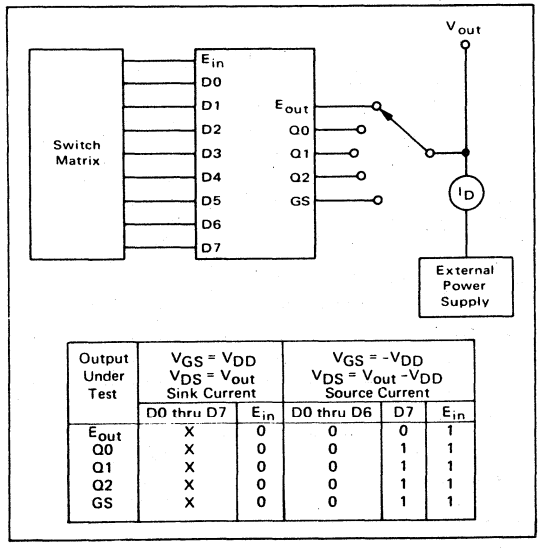
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Ouput Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Progagation Delay Time – E_{in} to E_{out}	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 120 ns		5.0	–	205	410	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 77 ns		10	–	110	220	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 55 ns		15	–	80	160	
Propagation Delay Time (E_{in} to GS	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} - (0.5 ns/pF) C_L + 40 ns		15	–	65	130	
Propagation Delay Time – E_{in} to Q_n	t_{PHL}, t_{PLH}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 195 ns		5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 107 ns		10	–	140	280	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Propagation Delay Time – D_n to Q_n	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 137 ns		10	–	170	340	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Propagation Delay Time – D_n to GS	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 195 ns		5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 107 ns		10	–	140	280	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	

*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL SINK AND SOURCE CURRENT CHARACTERISTICS



Output Under Test	V_{GS} = V_{DD}, V_{DS} = V_{out} Sink Current		V_{GS} = -V_{DD}, V_{DS} = V_{out} -V_{DD} Source Current		
	D0 thru D7	E_{in}	D0 thru D6	D7	E_{in}
E_{out}	X	0	0	0	1
Q0	X	0	0	1	1
Q1	X	0	0	1	1
Q2	X	0	0	1	1
GS	X	0	0	1	1

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT

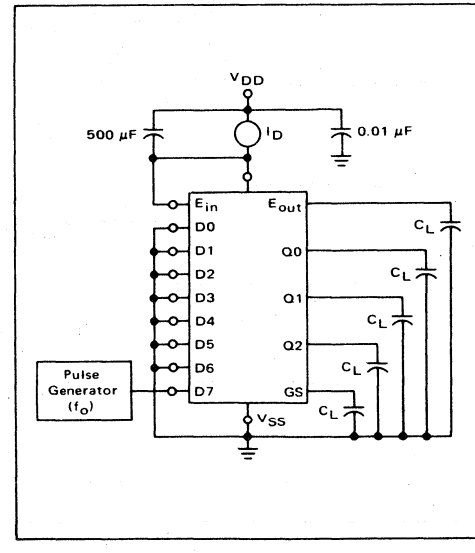
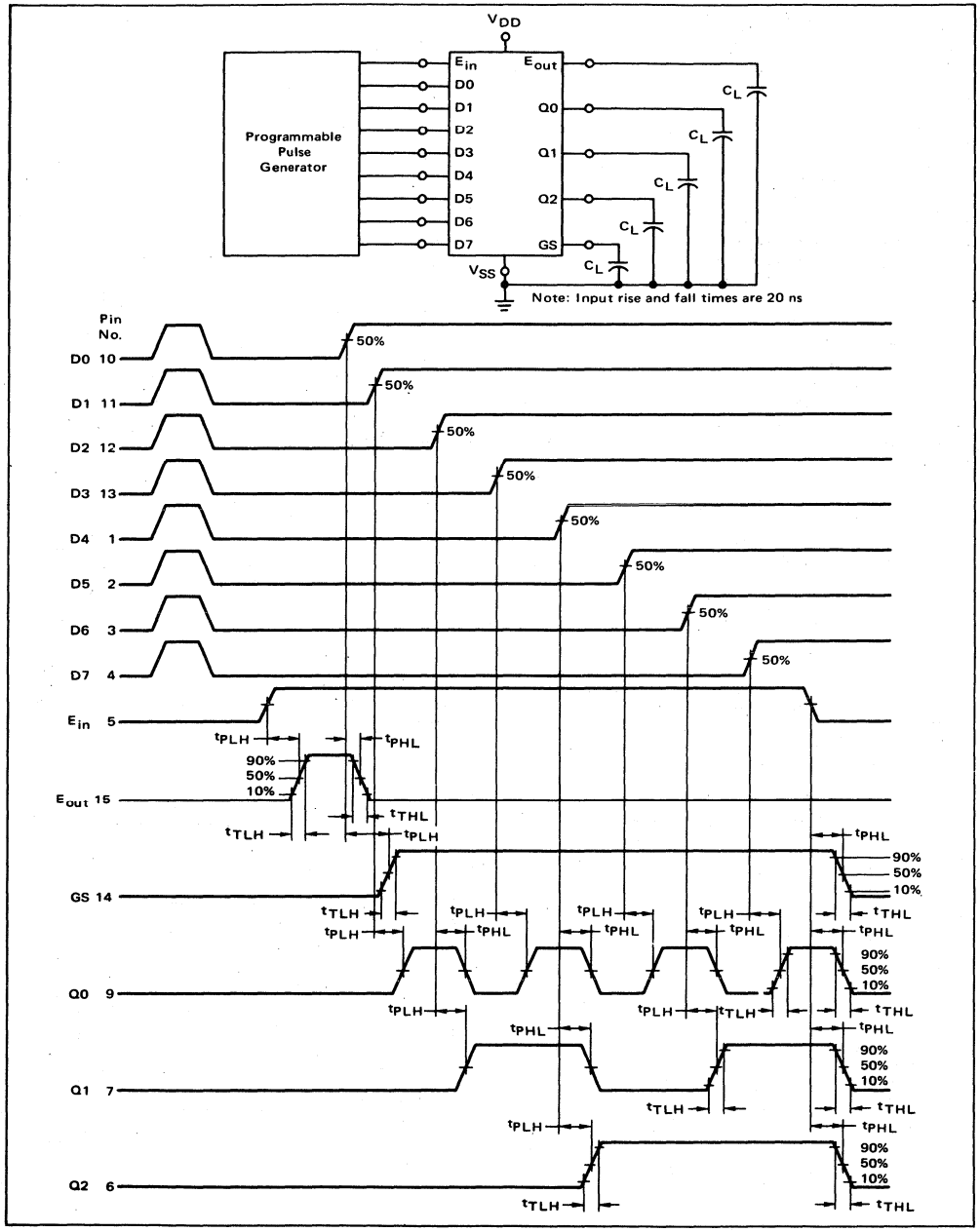


FIGURE 3 – AC TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAM
(Positive Logic)

LOGIC EQUATIONS

$E_{out} = E_{in} \bullet \bar{D}0 \bullet \bar{D}1 \bullet \bar{D}2 \bullet \bar{D}3 \bullet \bar{D}4 \bullet \bar{D}5 \bullet \bar{D}6 \bullet \bar{D}7$
$Q0 = E_{in} \bullet (D1 \bullet \bar{D}2 \bullet \bar{D}4 \bullet \bar{D}6 + D3 \bullet \bar{D}4 \bullet \bar{D}6 + D5 \bullet \bar{D}6 + D7)$
$Q1 = E_{in} \bullet (D2 \bullet \bar{D}4 \bullet \bar{D}5 + D3 \bullet \bar{D}4 \bullet \bar{D}5 + D6 + D7)$
$Q_2 = E_{in} \bullet (D4 + D5 + D6 + D7)$
$GS = E_{in} \bullet (D0 + D1 + D2 + D3 + D4 + D5 + D6 + D7)$

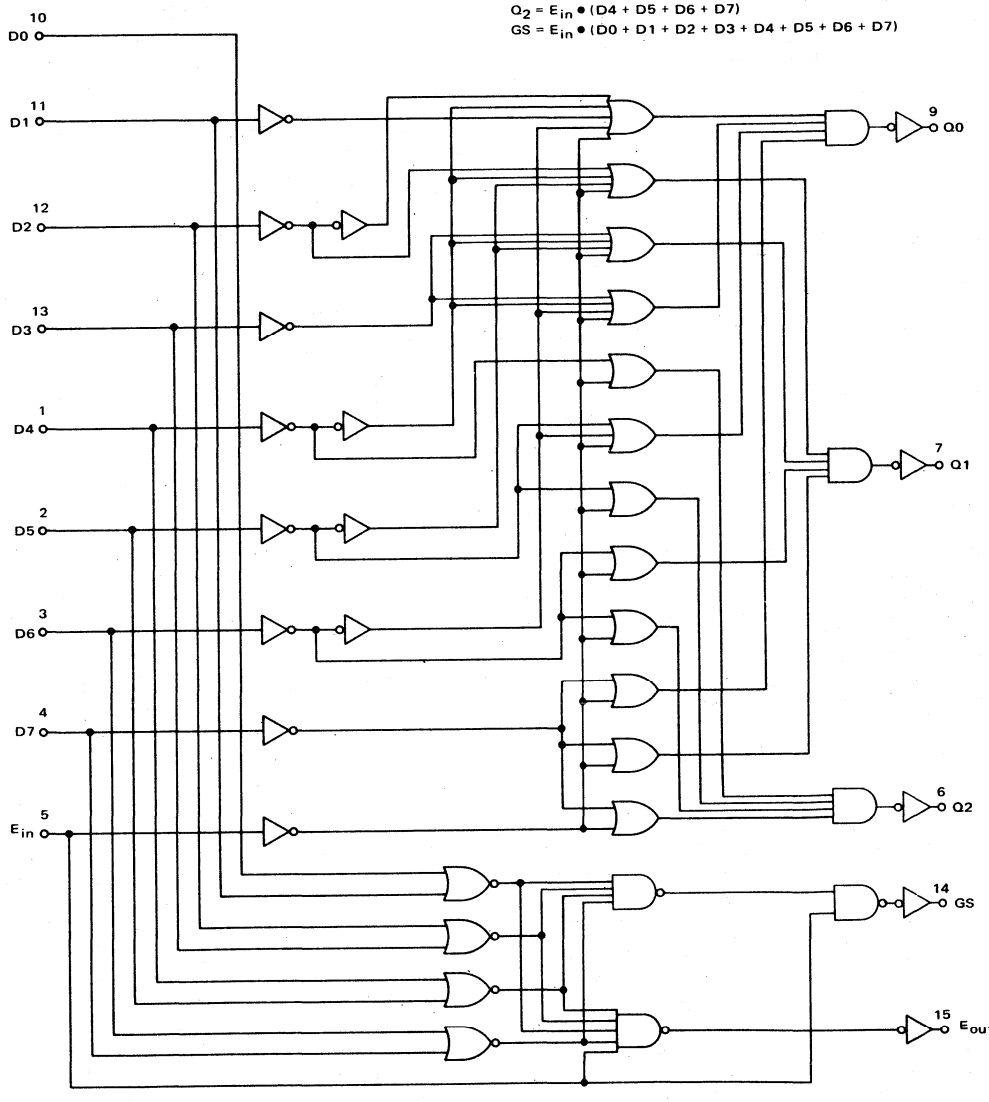


FIGURE 4 – TWO MC14532B's CASCADED FOR 4-BIT OUTPUT

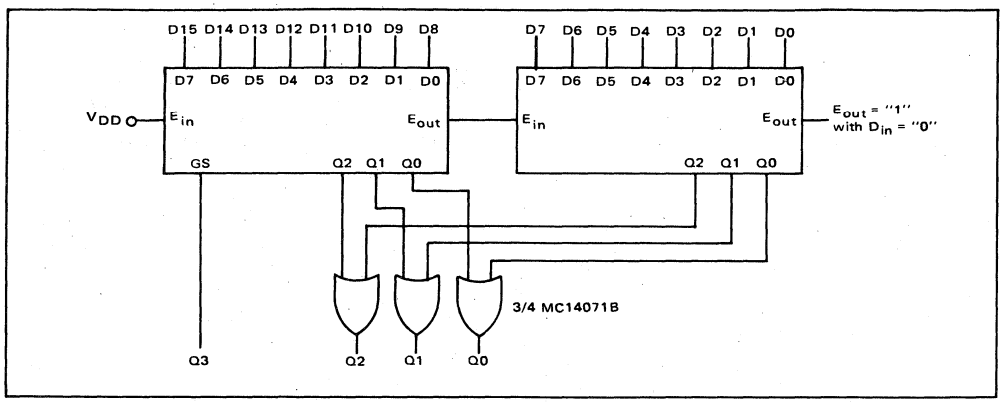


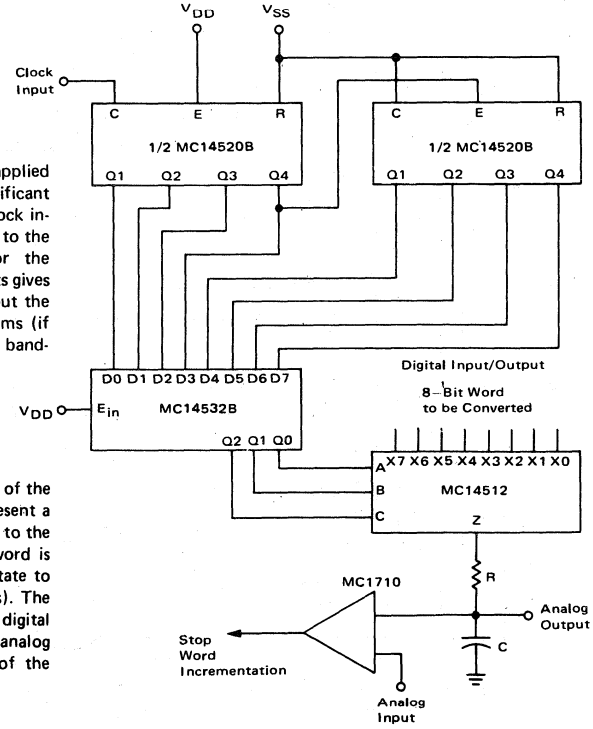
FIGURE 5 – DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTER

DIGITAL TO ANALOG CONVERSION

The digital eight-bit word to be converted is applied to the inputs of the MC14512 with the most significant bit at X7 and the least significant bit at X0. A clock input of up to 2.5 MHz (at V_{DD} = 10 V) is applied to the MC14520B. A compromise between I_{bias} for the MC1710 and ΔR between N and P-channel outputs gives a value of R of 33 k ohms. In order to filter out the switching frequencies, RC should be about 1.0 ms (if R = 33 k ohms, C ≈ 0.03 μF). The analog 3.0 dB bandwidth would then be dc to 1.0 kHz.

ANALOG TO DIGITAL CONVERSION

An analog signal is applied to the analog input of the MC1710. A digital eight-bit word known to represent a digitized level less than the analog input is applied to the MC14512 as in the D to A conversion. The word is incremented at rates sufficient to allow steady state to be reached between incrementations (i.e. 3.0 ms). The output of the MC1710 will change when the digital input represents the first digitized level above the analog input. This word is the digital representation of the analog word.



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14534B

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

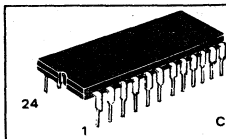
REAL TIME

5-DECADE COUNTER

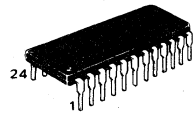
REAL TIME 5-DECADE COUNTER

The MC14534B is a complementary MOS circuit composed of five decade ripple counters that have their respective outputs time multiplexed using an internal scanner. Outputs of each counter are selected by the scanner and appear on four BCD pins. The selected decade is indicated by a logic high on the appropriate digit select pin. Both BCD and digit select outputs have three-state controls providing an "open-circuit" when these controls are high and allowing time multiplexing. Cascading may be accomplished by using the carry-out pin. The counters and scanner can be independently reset by applying a high to the counter master reset (MR) and the scanner reset (SR). The MC14534B was specifically designed for application in real time or event counters where continual updating and multiplexed displays are used.

- Four Operating Modes (See truth table)
- Input Error Detection Circuit
- Clock Conditioning Circuits for Slow Transition Inputs
- Counter Sequences on Positive Transition of Clock A
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 623



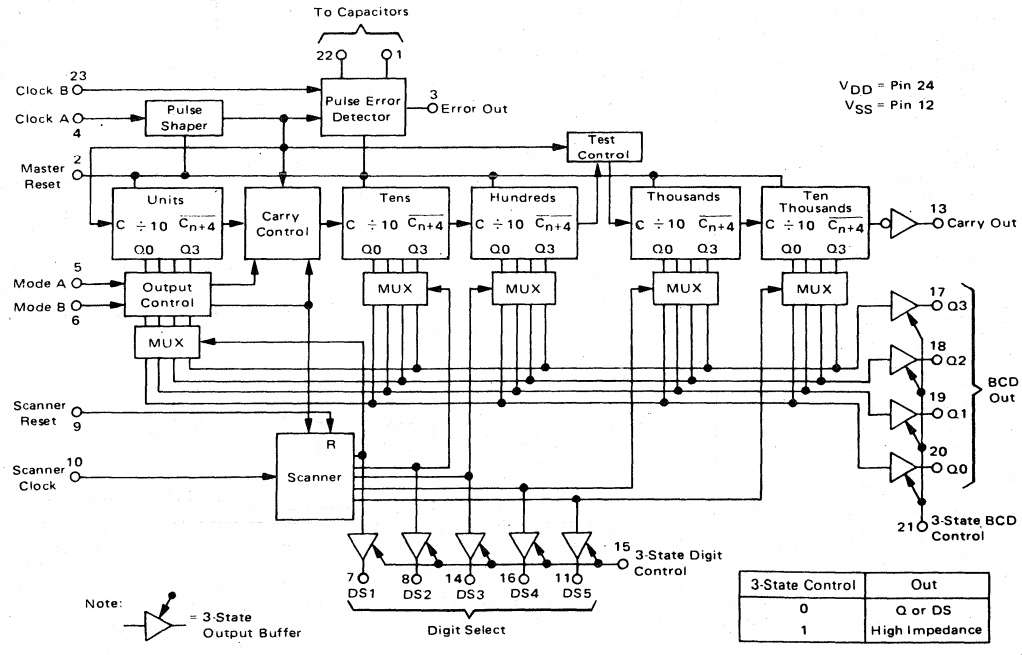
P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes

- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



3-State Control	Out
0	Q or DS
1	High Impedance

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	1.0	–	1.0	1.5	–	–	1.0	
(V_O = 9.0 or 1.0 Vdc)		10	2.0	–	2.0	3.0	–	–	2.0	
(V_O = 13.5 or 1.5 Vdc)		15	3.0	–	3.0	4.5	–	–	3.0	
(V_O = 0.5 or 4.5 Vdc) "1" Level	V_{IH}	5.0	4.0	–	4.0	3.5	–	4.0	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	8.0	–	8.0	7.0	–	8.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	12	–	12	11	–	12	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Output Drive Current – Pins 1 and 22 (AL Device)										mAdc
(V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.31	–	-0.25	-0.8	–	-0.17	–	
(V_{OH} = 9.5 Vdc)		10	-0.31	–	-0.25	-0.4	–	-0.17	–	
(V_{OH} = 13.5 Vdc)		15	-0.9	–	-0.75	-1.6	–	-0.51	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.024	–	0.02	0.03	–	0.014	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.06	–	0.05	0.09	–	0.035	–	
(V_{OL} = 1.5 Vdc)		15	1.3	–	0.25	1.63	–	0.175	–	
Output Drive Current – Pins 1 and 22 (CL/CP Device)										mAdc
(V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.11	–	-0.10	-0.8	–	-0.08	–	
(V_{OH} = 9.5 Vdc)		10	-0.11	–	-0.10	-0.4	–	-0.08	–	
(V_{OH} = 13.5 Vdc)		15	-0.33	–	-0.30	-1.6	–	-0.24	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.012	–	0.01	0.02	–	0.008	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.03	–	0.025	0.05	–	0.02	–	
(V_{OL} = 1.5 Vdc)		15	0.14	–	0.12	1.35	–	0.10	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	μAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.5\ \mu A/kHz)\ f + I_{DD}$ Scan Oscillator Frequency = 1 kHz							μAdc
		10	$I_T = (1.0\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (1.5\ \mu A/kHz)\ f + I_{DD}$							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

†To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$ where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

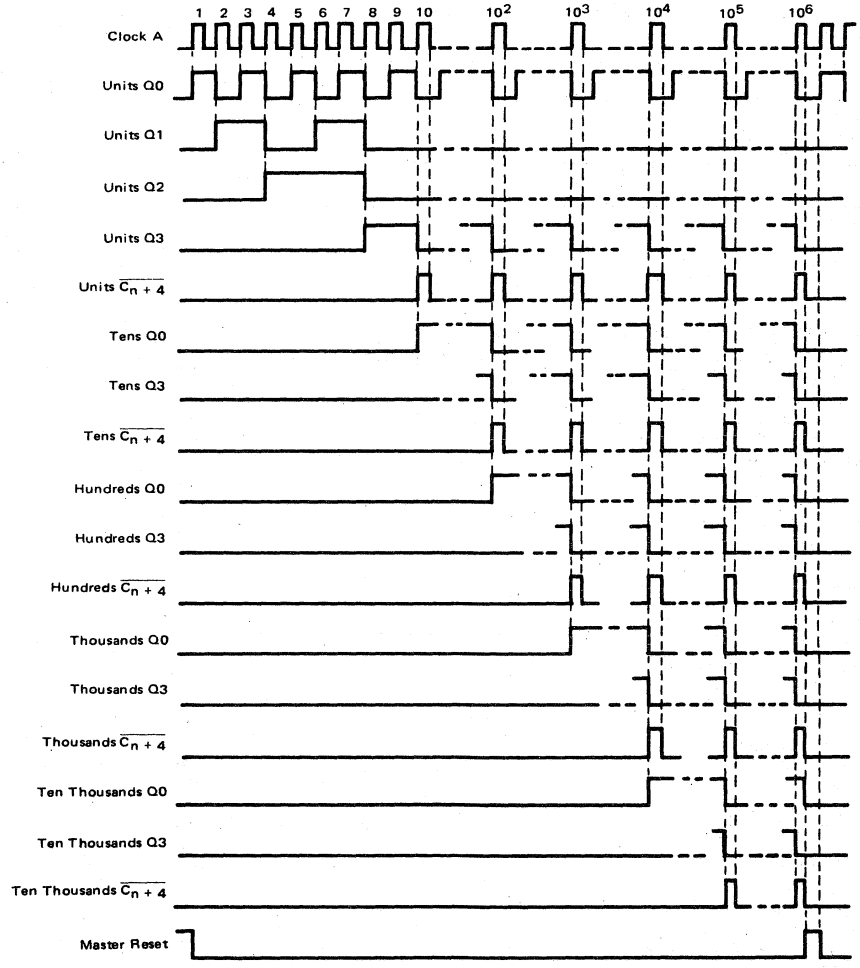
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 95 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 78 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 68 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 117 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 89 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 67 ns		15	–	40	80	
Propagation Delay Time, Clock to Q	t_{PLH}, t_{PHL}					μs
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 4.0 μs		5.0	–	4.0	8.0	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 1.5 μs		10	–	1.5	3.0	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 1.0 μs		15	–	1.0	2.25	
Clock to Carry Out	t_{PLH}					μs
t_{PLH} = (1.8 ns/pF) C_L + 3.3 μs		5.0	–	3.3	6.6	
t_{PLH} = (0.8 ns/pF) C_L + 1.1 μs		10	–	1.1	2.2	
t_{PLH} = (0.6 ns/pF) C_L + 0.8 μs		15	–	0.8	1.7	
Master Reset to Q	t_{PHL}					μs
t_{PHL} = (1.8 ns/pF) C_L + 1.8 μs		5.0	–	1.8	3.6	
t_{PHL} = (0.8 ns/pF) C_L + 0.6 μs		10	–	0.6	1.2	
t_{PHL} = (0.6 ns/pF) C_L + 0.5 μs		15	–	0.5	0.9	
Master Reset to Error Out	t_{PHL}					μs
t_{PHL} = (1.8 ns/pF) C_L + 0.57 μs		5.0	–	0.6	1.5	
t_{PHL} = (0.8 ns/pF) C_L + 0.19 μs		10	–	0.2	.5	
t_{PHL} = (0.6 ns/pF) C_L + 0.11 μs		15	–	0.12	0.38	
Scanner Clock to Q	t_{PLH}, t_{PHL}					μs
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 1.8 μs		5.0	–	1.8	3.6	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 0.6 μs		10	–	0.6	1.2	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 0.5 μs		15	–	0.5	0.9	
Scanner Clock to Digit Select	t_{PLH}, t_{PLH},					μs
t_{PHL}, t_{PLH} = (1.8 ns/pF) C_L + 1.5 μs		5.0	–	1.5	3.0	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 0.5 μs		10	–	0.5	1.0	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 0.4 μs		15	–	0.4	0.75	
Clock Pulse Frequency	f_{cl}	5.0	–	1.0	0.5	MHz
		10	–	3.0	1.0	
		15	–	5.0	1.2	
Clock or Scanner Clock Pulse Width	t_{WH}	5.0	1000	500	–	ns
		10	500	190	–	
		15	375	125	–	
Master Reset Pulse Width	$t_{WH(R)}$	5.0	2000	900	–	ns
		10	600	300	–	
		15	450	250	–	

*The formula given is for the typical characteristics only.

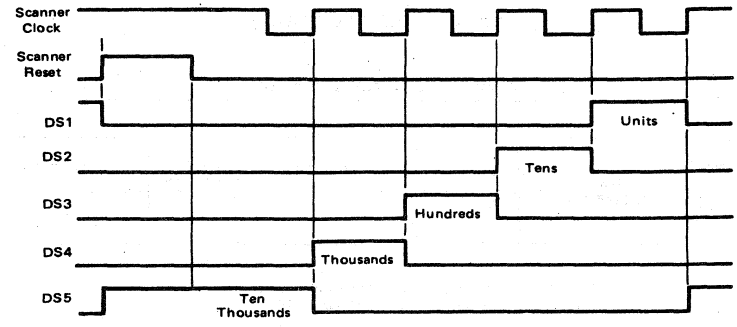
COUNTER TIMING DIAGRAM



MODE CONTROL TRUTH TABLE

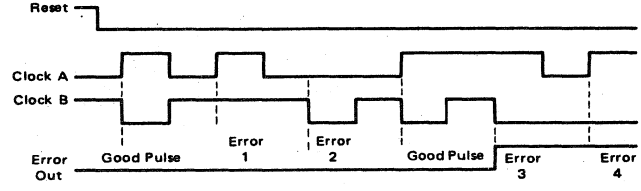
Mode A	Mode B	First Decade Output	Carry to Second Stage	Application
0	0	Normal Count and Display	At 9 to 0 transition of first decade	5-Decade Counter
0	1	Inhibited	Input Clock	Test Mode: Clock directly into stages 1, 2, and 4.
1	1	Inhibited	At 4 to 5 transition of first decade	4-decade counter with ÷ 10 and roundoff at front end.
1	0	Counts 3,4,5,6,7 = 5 Counts 8,9,0,1,2 = 0	At 7 to 8 transition of first decade	4-decade counter with 1/2 pence capability.

SCANNER TIMING DIAGRAM



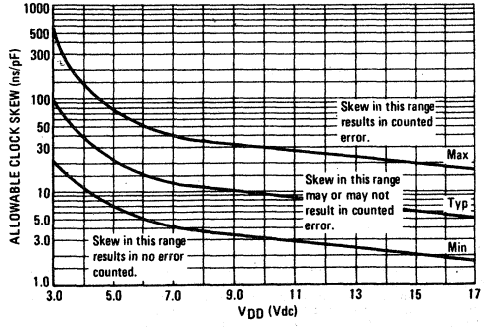
Note: If Mode B = 1, the first decade is inhibited and S1 will not go high, and the cycle will be shortened to four stages.
DS5 is selected automatically when Scanner Reset goes high.

ERROR DETECTION TIMING DIAGRAM



Note: Error detector looks for inverted pulse on Clock B. Whenever a positive edge at Clock A is not accompanied by a negative pulse at Clock B (or vice-versa) within a time period of the one-shots an error is counted. Three errors result in Error Out to go to a "1". If error detection is not needed, tie Clock B high or low and leave Pins 1 and 22 unconnected.

CLOCK SKEW RANGE

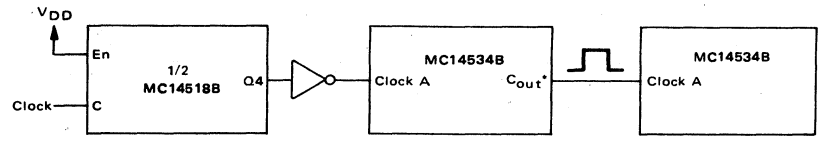


Notes:

1. The skew is the time difference between the low-to-high transition of C_A to the high-to-low transition of C_B or vice-versa. Capacitors C1 = C22 tied from pins 1 and 22 to V_{SS}.
2. This graph is accurate for C1 = C22 $\geqslant$ 100 pF.
3. When the error detection circuitry is not used, pins 1 and 22 are left open.

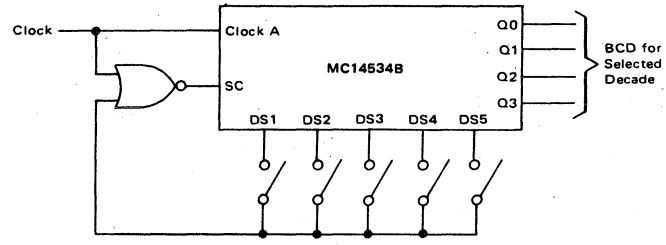
APPLICATIONS INFORMATION

FIGURE 1 – CASCADE OPERATION



*Carry Out is high for a single clock period when all five BCD decades go to zero. (Carry Out also goes high when MR is applied.)

FIGURE 2 – FORCING A DECADE TO THE Q OUTPUTS



When the Q outputs of a given decade are required, this configuration will lock up the selected decade within four clock cycles. The select line feedback may be hardwired or switched.

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14536B

PROGRAMMABLE TIMER

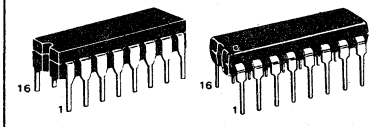
The MC14536B programmable timer is a flexible 24-stage ripple binary counter with 16 stages selectable by a binary code. Provisions for an on-chip RC oscillator, or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has also been included. By selecting the appropriate output in conjunction with the correct input clock frequency, a variety of timing can be achieved.

- 24 Flip-Flop Stages – Will Count From 2^0 to 2^{24}
- Last 16 Stages Selectable By Four-Bit Select Code
- Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit Input
- On-Chip RC Oscillator Provisions
- On-Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation With Very Long Rise and Fall Times
- Clock Input f_{max} = 3.0 MHz typical @ V_{DD} = 10 Vdc
- Counter Advances On Negative Going Edge of Clock
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE TIMER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

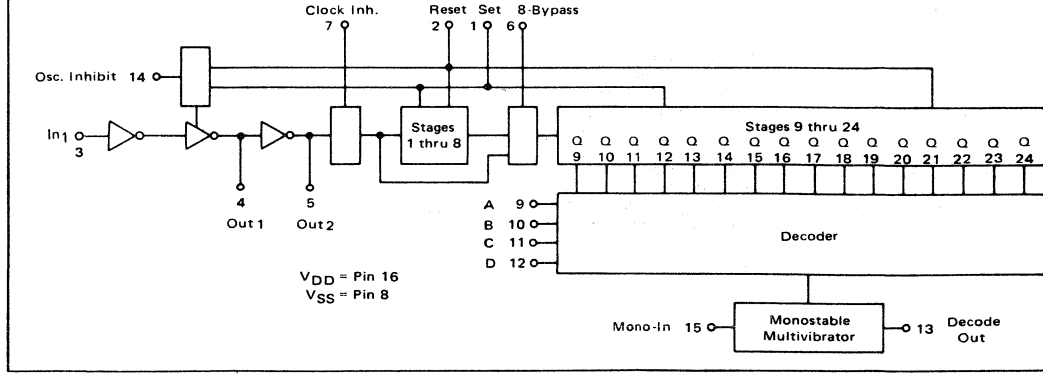
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1		±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	**0.010**	5.0	–	150	µAdc
(Per Package)		10	–	10	–	**0.020**	10	–	300	
		15		20	–	**0.030**	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	**50**	–	**0.010**	**50**	–	**375**	µAdc
(Per Package)		10	–	**100**	–	**0.020**	**100**	–	**750**	
		15	–	**200**	–	**0.030**	**200**	–	**1500**	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.15\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (2.3\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.55\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T\ (50\ pF) + 3 \times 10^{-3}\ (C_L - 50)\ V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q1, 8-Bypass (P in 6) High						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1715 ns		5.0	–	1800	3600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 617 ns		10	–	650	1300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	–	450	1000	
Clock to Q1, 8-Bypass (Pin 6) Low	t_{PLH}, t_{PHL}					µs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3715 ns		5.0	–	3.8	7.6	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1467 ns		10	–	1.5	3.0	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 1075 ns		15	–	1.1	2.3	
Clock to Q16	t_{PLH}, t_{PHL}					µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 6915 ns		5.0	–	7.0	14	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2967 ns		10	–	3.0	6.0	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2175 ns		15	–	2.2	4.5	
Reset to Q_n	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 1415 ns		5.0	–	1500	3000	
t_{PHL} = (0.66 ns/pF) C_L + 567 ns		10	–	600	1200	
t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	–	450	900	
Clock Pulse Width	t_{WH}	5.0	600	300	–	ns
		10	200	100	–	
		15	170	85	–	
Clock Pulse Frequency (50% Duty Cycle)	f_{cl}	5.0	–	1.2	0.4	MHz
		10	–	3.0	1.5	
		15	–	5.0	2.0	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Reset Pulse Width	t_{WH}	5.0	1000	500	–	ns
		10	400	200	–	
		15	300	150	–	

*The formula given is for the typical characteristics only.

IN_1	Set	Reset	Clock Inh	Osc Inh	Out 2	Out 2	Decode Out
⎍	0	0	0	0	⎍	⎎	No Change
⎎	0	0	0	0	⎎	⎍	Advance to next state
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0			No Change
0	0	0	0	X	0	1	No Change
1	0	0	0	⎍	⎎	⎍	Advance to next state

X = Don't Care

TRUTH TABLE

D	C	B	A	Decode Out	8-Bypass
0	0	0	0	9	1
0	0	0	1	10	2
0	0	1	0	11	3
0	0	1	1	12	4
0	1	0	0	13	5
0	1	0	1	14	6
0	1	1	0	15	7
0	1	1	1	16	8
1	0	0	0	17	9
1	0	0	1	18	10
1	0	1	0	19	11
1	0	1	1	20	12
1	1	0	0	21	13
1	1	0	1	22	14
1	1	1	0	23	15
1	1	1	1	24	16

OPERATING CHARACTERISTICS

Set input initializes output to a "1". This is accomplished by setting an output conditioning latch to a 1 while at the same time resetting the 24 flip-flop stages. With the occurence of the first negative transition of the clock, the output will change to a "0". When the circuit is in the Set condition, the counter flip-flop stages will start counting on the second negative transition. The resulting behavior is the same as if each of the 24 flip-flop stages were set.

Reset inputs resets all stages to a logical "0". Reset or Set also disables the on-chip RC oscillator to allow very low power standby operation. In_1 input is used as the external Clock input or as the input to the on-chip RC oscillator.

Out 1, Out 2 outputs are used in the on-chip RC oscillator configuration.

8-Bypass input bypasses the first eight stages resulting in a 16-stage counter with all 16 stages selectable, one at a time. Clock Inhibit input disconnects the first counter stage from the input circuit, therefore inhibiting counting. This Clock Inhibit input is independent of the state of the Clock input. When the Clock Inhibit input is disabled, the counter will start counting only with the occurrence of the first negative edge of the Clock.

Binary Select inputs A, B, C, and D select the flip-flop stage to be connected to the output. Decode Out output can either be connected directly to a flip-flop output or to the monostable output. Osc Inhibit input can be used to disable the on-chip RC oscillator to allow very low power standby operation. Mono In input is used as the timing pin for the on-chip monostable oscillator. If the Mono In input is grounded through a resistor, the monostable circuit is disabled and the output is connected directly to the selected flip-flop. The monostable circuit is enabled if a resistor is connected between this pin and V_{DD} and a capacitor connected between this pin and ground. Any desired pulse width can be achieved depending upon the value of the R and C selected.

The test mode configuration divides the 24 flip-flop stages into three 8-stage sections to facilitate a fast test sequence. This test mode is enabled when 8-Bypass, Set and Reset are at a "1"

APPLICATIONS

FIGURE 1 – TIME INTERVAL CONFIGURATION USING EXTERNAL CLOCK; SET AND CLOCK INHIBIT FUNCTIONS

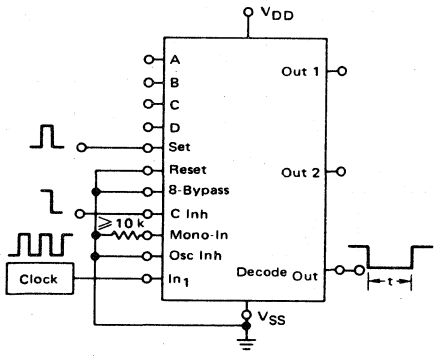


FIGURE 2 – TIME INTERVAL CONFIGURATION USING EXTERNAL CLOCK; RESET AND OUTPUT MONOSTABLE TO ACHIEVE A PULSE OUTPUT

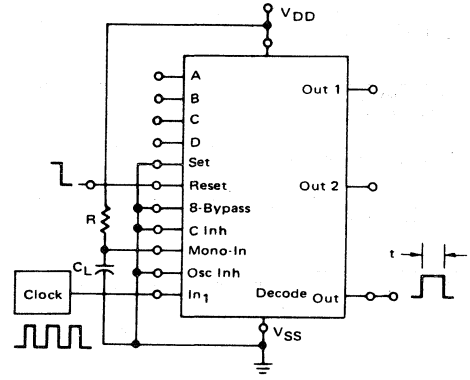
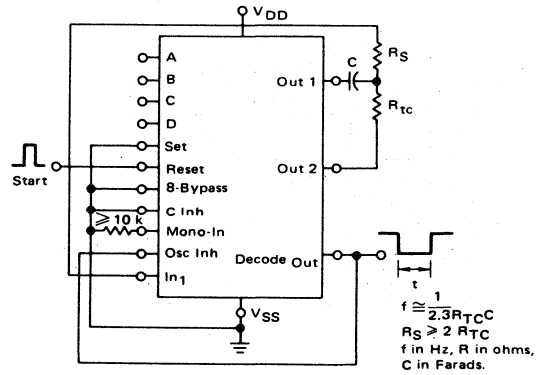
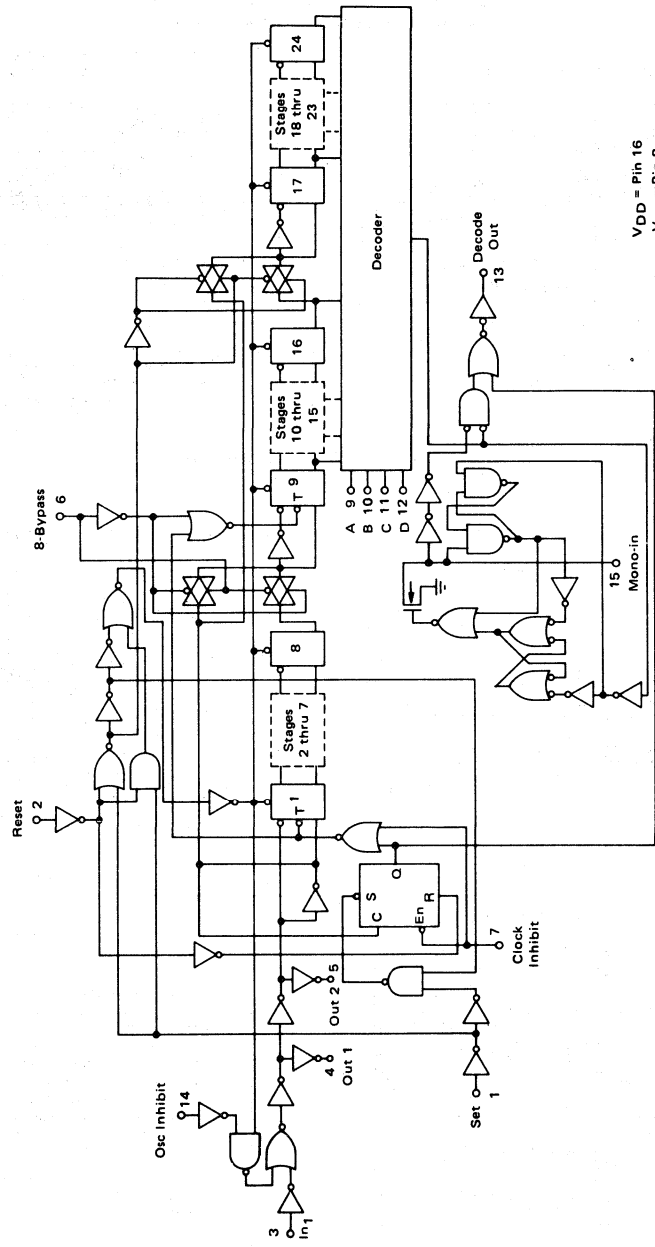


FIGURE 3 – TIME INTERVAL CONFIGURATION USING ON-CHIP RC OSCILLATOR AND RESET INPUT TO INITIATE TIME INTERVAL



LOGIC DIAGRAM



TYPICAL RC OSCILLATOR CHARACTERISTICS

(For Circuit Diagram See Figure 3 in Application)

FIGURE 4 – RC OSCILLATOR STABILITY

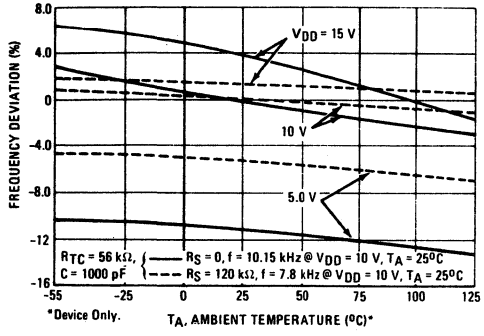
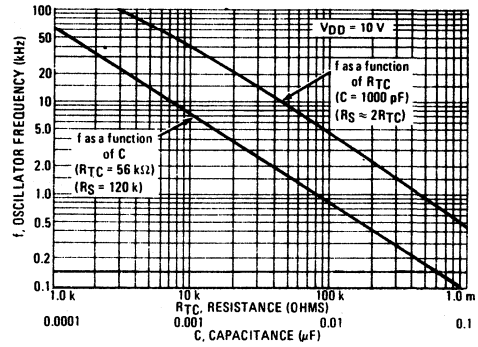


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C



MONOSTABLE CHARACTERISTICS

(For Circuit Diagram See Figure 2 in Application)

FIGURE 6 – TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 5.0 V

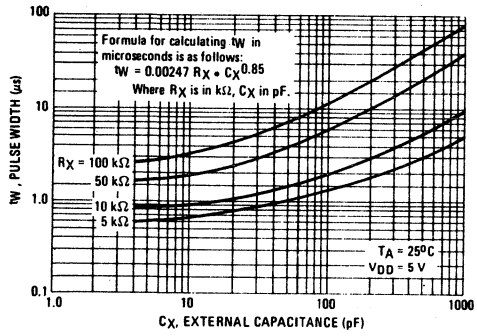


FIGURE 7 – TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 10 V

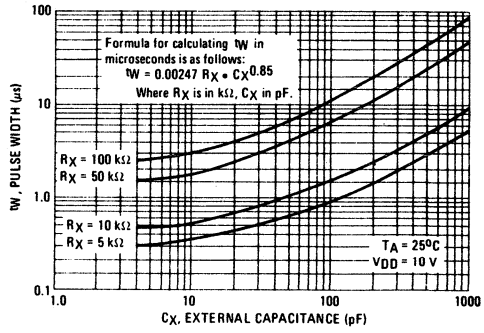
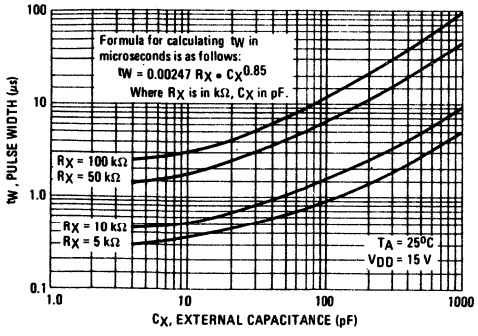


FIGURE 8 – TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 15 V



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 9 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

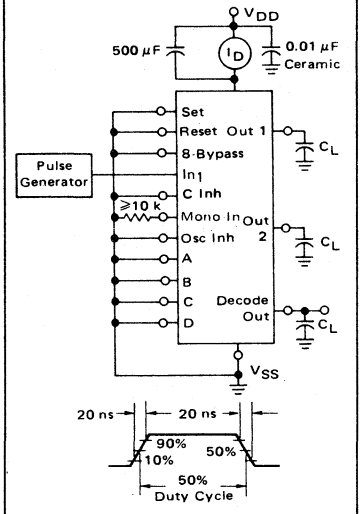
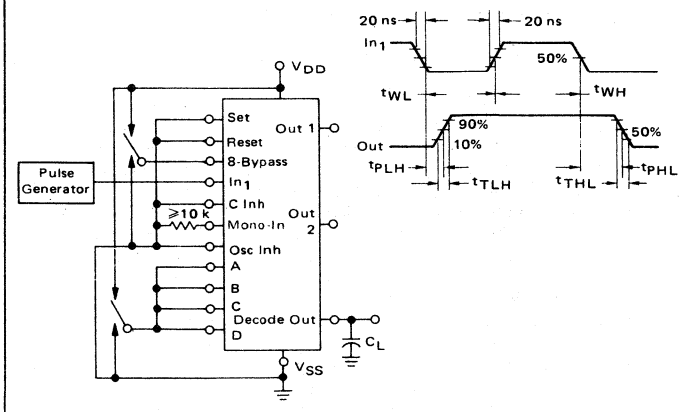


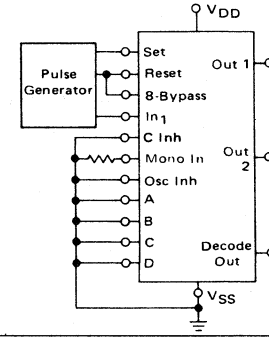
FIGURE 10 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



FUNCTIONAL TEST SEQUENCE

Test function (Figure 11) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into In_1 which will cause the counter to ripple from an all "1" state to an all "0" state.

FIGURE 11 – FUNCTIONAL TEST CIRCUIT



FUNCTIONAL TEST SEQUENCE

INPUTS				OUTPUTS	COMMENTS
In_1	Set	Reset	8-Bypass	Decade Out Q1 thru Q24	
1	0	1	1	0	All 24 stages are in Reset mode.
1	1	1	1	0	Counter is in three 8-stage sections in parallel mode.
0	1	1	1	0	First "1" to "0" transition of clock.
1 0 – – –	1	1	1		255 "1" to "0" transitions are clocked in the counter.
0	1	1	1	1	The 255 "1" to "0" transition.
0	0	0	0	1	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from "1" to "0".
1	0	0	0	1	In_1 Switches to a "1".
0	0	0	0	0	Counter Ripples from an all "1" state to an all "0" state.

MOTOROLA

MCM14537

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14537 is a static random access memory (RAM) organized in a 256 x 1-bit pattern and constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of eight address inputs (A_n), one data input (D_{in}), one write enable input (WE), one strobe input (ST), two chip enable inputs (CE_n), and one data output (D_{out}).

Using both chip enable inputs as extensions of the address inputs, a 10-bit address scheme may be employed. Four MCM14537 devices may be used to comprise a 1024-bit memory without additional address decoding. The CE and ST inputs are dissimilary designed to enable usage of the memory in a variety of applications. An output latch is provided on the chip for storing the data read or written into memory, making a data-out storage register unnecessary. The CE inputs control the data output for third-state (high output impedance) or active operation which makes the memory very useful in a bus oriented system. When CE2 is high the chip is fully disabled. When CE1 is high the output is in the third state but data can be written into the output latch during a read cycle. This enables the use of the memory for fast reading by using the CE1 input to enable the latch. The memory is also designed so that dc signals can operate the memory with no maximum pulse width required on the CE and ST lines.

Medium speed operation and micropower operation make the device useful in scratch pad and buffer applications where micropower or battery operation and high noise immunity are required.

- Quiescent Current = 0.5 μA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- 3-state Output Capability for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

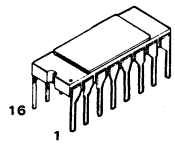
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (256 x 1) STATIC RANDOM ACCESS MEMORY

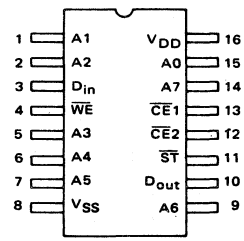


CERAMIC PACKAGE
CASE 690

ORDERING INFORMATION

MCM14XXX — Suffix Denotes
- L Ceramic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Noise Immunity #	V_{NL}									Vdc
($\Delta V_{out} \leq$ 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq$ 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq$ 1.5 Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq$ 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq$ 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq$ 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±1.0	–	±0.00001	±1.0	–	±14	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	100	–	0.5	100	–	1800	µAdc
(Per Package)		10	–	200	–	1.0	200	–	3600	
		15	–	400	–	1.5	400	–	7200	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	100	–	0.5	100	–	1800	µAdc
(Per Package)		10	–	200	–	1.0	200	–	3600	
		15	–	400	–	1.5	400	–	7200	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.46 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.91 µA/kHz) f + I_{DD}							
		15	I_T = (4.37 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

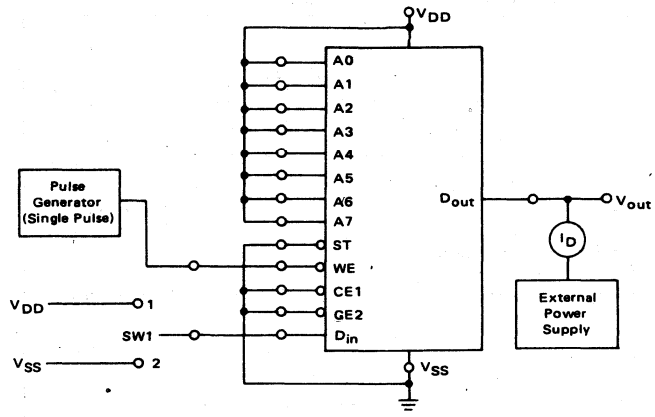
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	3	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns			5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns			10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns			15	–	65	130	
Output Fall Time	3	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns			5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns			10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns			15	–	40	80	
Read Access Time from $\overline{ST}$ or $\overline{CE2}$	4, 5	$t_{acc(R)}$					ns
t_{acc} = (1.4 ns/pF) C_L + 2480 ns			5.0	400	2500	6000	
t_{acc} = (0.7 ns/pF) C_L + 690 ns			10	150	700	2000	
t_{acc} = (0.5 ns/pF) C_L + 393 ns			15	115	400	1500	
Output Enable Delay from $\overline{CE1}$ or $\overline{CE2}$	5, 6	$t_{acc(\overline{CE}_n)}$	5.0	70	300	900	ns
			10	25	100	300	
			15	20	70	225	
Setup Time from A_n to $\overline{ST}$ or $\overline{CE2}$	4, 5, 6, 7	$t_{su(A)}$	5.0	1800	600	–	ns
			10	600	200	–	
			15	450	140	–	
Hold Time from A_n to $\overline{ST}$ or $\overline{CE2}$	4, 5, 6, 7	$t_{h(A)}$	5.0	600	200	–	ns
			10	240	80	–	
			15	180	55	–	
Data Hold Time	7	$t_{h(D)}$	5.0	1400	480	–	ns
			10	500	160	–	
			15	375	110	–	
Data Setup Time	7	$t_{su(D)}$	5.0	3600	1200	–	ns
			10	1800	600	–	
			15	1350	420	–	
$\overline{\text{Write Enable}}$ Hold Time	7	$t_{h(\overline{WE})}$	5.0	150	50	–	ns
			10	60	20	–	
			15	45	15	–	
$\overline{\text{Write Enable}}$ Setup Time	7	$t_{su(\overline{WE})}$	5.0	720	240	–	ns
			10	240	80	–	
			15	180	55	–	
$\overline{\text{Write Enable}}$ to D_{out} Disable**	4	$t_{\overline{WE}}$	5.0	720	240	–	ns
			10	240	80	–	
			15	180	55	–	
$\overline{\text{Strobe}}$ or $\overline{CE2}$ Pulse Width When Reading	4, 5, 6	$t_{WL(R)}$	5.0	1350	450	–	ns
			10	450	150	–	
			15	340	100	–	
$\overline{\text{Strobe}}$, $\overline{CE1}$ or $\overline{CE2}$ Pulse Width When Writing	7	$t_{WL(W)}$	5.0	2400	1200	–	ns
			10	1260	600	–	
			15	945	420	–	
Write Recovery Time	4	$t_{R(W)}$					ns
t_W = (1.4 ns/pF) C_L + 219 ns			5.0	70	240	720	
t_W = (0.7 ns/pF) C_L + 70 ns			10	25	80	240	
t_W = (0.5 ns/pF) C_L + 47.5 ns			15	20	55	180	
$\overline{CE1}$ or $\overline{CE2}$ to D_{out} Disable Delay**	6	$t_{\overline{CE}_n}$	5.0	70	300	900	ns
			10	25	100	300	
			15	20	70	225	
Read Setup Time	4, 5	$t_{su(R)}$	5.0	0	-100	–	ns
			10	0	-40	–	
			15	0	-30	–	
Read Hold Time	4, 5	$t_{h(R)}$	5.0	540	180	–	ns
			10	240	60	–	
			15	180	45	–	
Read Cycle Time	4, 5	$t_{cyc(R)}$	5.0	–	2500	6000	ns
			10	–	700	2100	
			15	–	500	1575	
Write Cycle Time	7	$t_{cyc(W)}$	5.0	–	1400	4800	ns
			10	–	700	2100	
			15	–	500	1575	

* The formula given is for the typical characteristics only.
**10% output change into a 1.0 kΩ load.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CURRENT CHARACTERISTICS TEST CIRCUIT



Input	Output Source Characteristics	Output Sink Characteristics
$\overline{WE}$	Pulse Once	Pulse Once
D_{in}	SW1 in Position 1	SW1 in Position 2
V_{GS}	$-V_{DD}$	V_{DD}
V_{DS}	$V_{out} - V_{DD}$	V_{out}

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

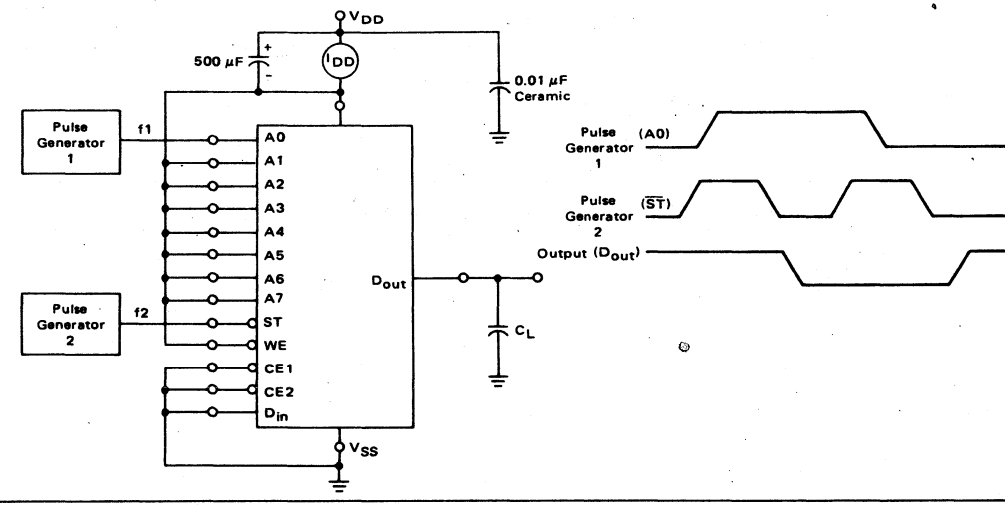


FIGURE 3 – AC TEST CIRCUIT

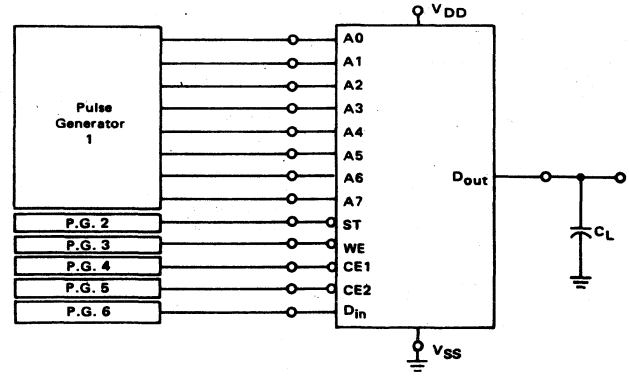
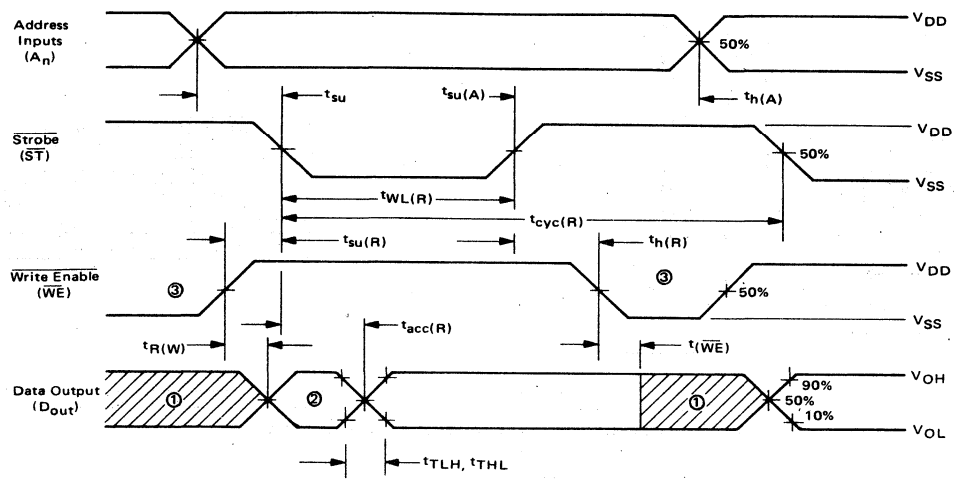
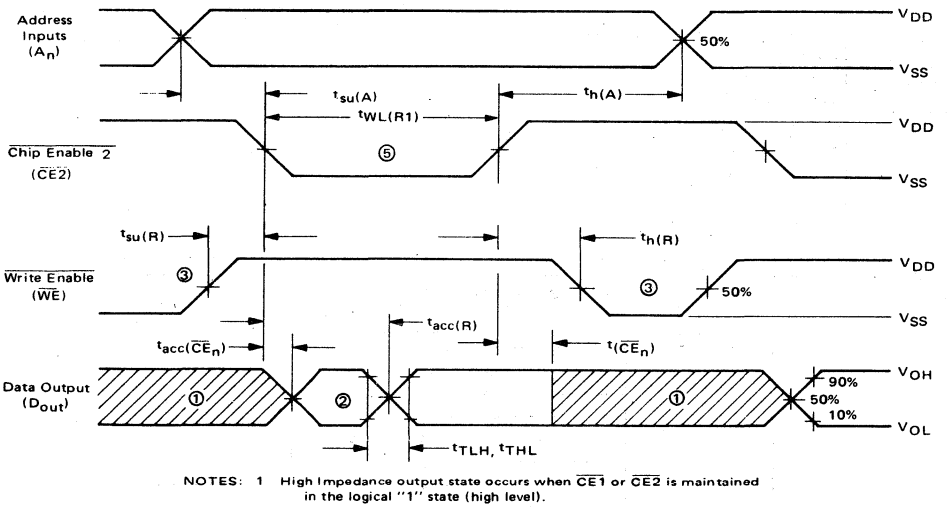


FIGURE 4 – READ CYCLE WAVEFORMS UTILIZING STROBE-TO-ACCESS MEMORY



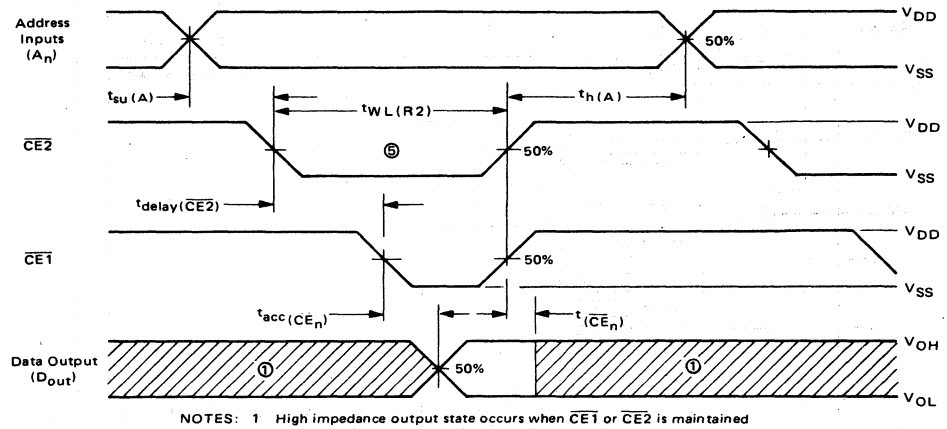
NOTES:
1. High impedance output state occurs when $\overline{WE}$ is maintained as a logical "0" (low level).
2. The output momentarily displays data from the previous state.
3. For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle.
4. $\overline{CE1}$ and $\overline{CE2}$ are maintained at a logical "0" state (low level).
5. All input rise and fall times are 20 ns.

FIGURE 5 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE2}$ FOR ACCESS MEMORY



NOTES:
1. High impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).
2. The output momentarily displays data from the previous state.
3. For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle.
4. All input rise and fall times are 20 ns.
5. $t_{WL(R1)} \geq t_{acc}$ (R) max

FIGURE 6 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE1}$ AND $\overline{CE2}$ TO ACCESS MEMORY

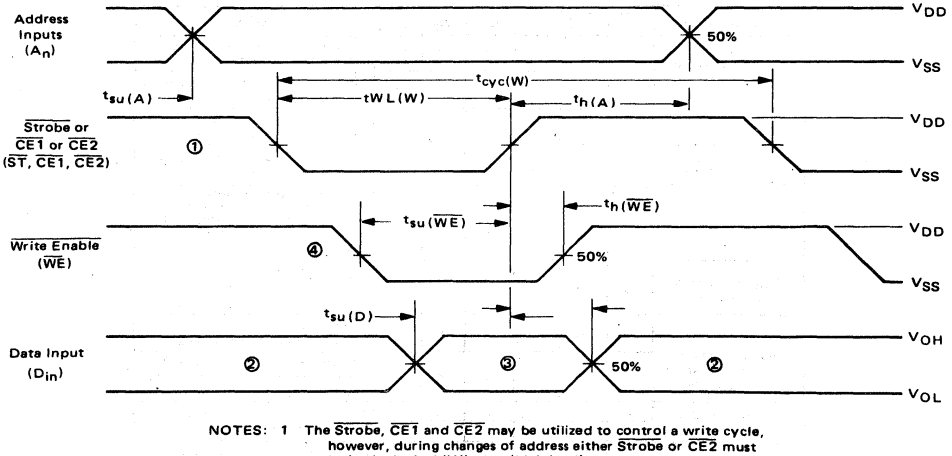


NOTES:
1. High impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).
2. $\overline{WE}$ is maintained at the logical "1" state for this example.
3. All input rise and fall times are 20 ns
4. $t_{delay(\overline{CE2})}$ minimum assuares that only data presently addressed will appear at the output.

$$t_{delay(\overline{CE2})}\ \text{min.} = t_{acc_R\ \text{max.}} - t_{acc(\overline{CE1})}\ \text{min.}$$

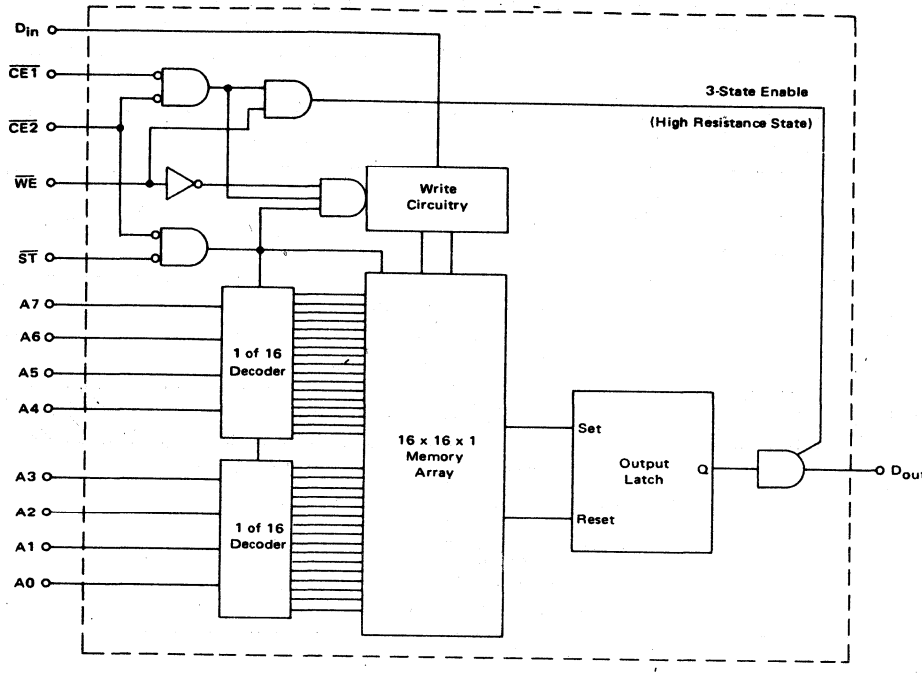
5. $t_{WL(R2)} \geqslant t_{delay}\ (\overline{CE2})\ \text{min} + t_{acc}\ (CE_n)\ \text{max}$

FIGURE 7 – WRITE CYCLE WAVEFORMS



NOTES:
1. The Strobe, $\overline{CE1}$ and $\overline{CE2}$ may be utilized to control a write cycle, however, during changes of address either Strobe or $\overline{CE2}$ must be in the logical "1" state (high level).
2. Data input logic level is don't care during the indicated intervals.
3. Data input logic level must remain fixed.
4. Write Enable may be maintained as a logical "0" during the write cycle.
5. All input rise and fall times are 20 ns.

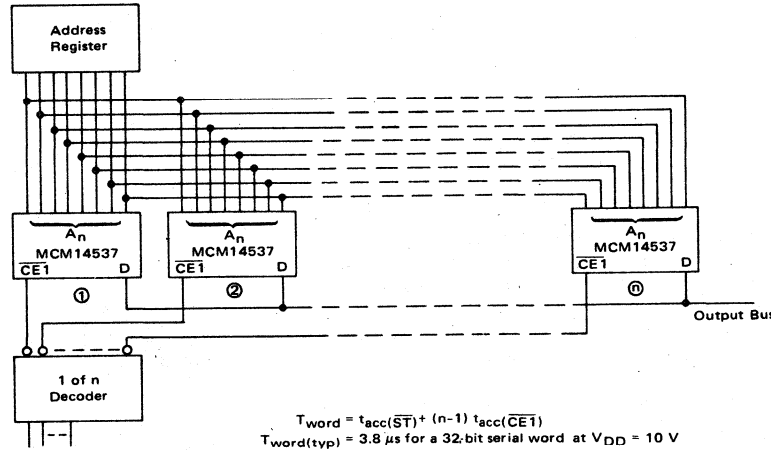
LOGIC/BLOCK DIAGRAM



FUNCTION	$\overline{CE1}$	$\overline{CE2}$	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	COMMENTS
Address changing valid	X	X	1	X	X	R/A	D_{out} will be active if $\overline{CE1}$ and $\overline{CE2}$ = "0" and $\overline{WE}$ = "1".
	X	1	X	X	X	R	$\overline{CE2}$ = "1", fully disables internal logic and output.
Address changing not valid	X	0	0	X	X	R/A	Changing address in this mode may result in altered data.
D_{out} disabled in high resistance state	1	X	X	X	X	R	$\overline{CE1}$ = "1" disables write cycle and D_{out}.
	X	1	X	X	X	R	The chip is fully disabled.
	X	X	X	0	X	R	$\overline{WE}$ = "0" enables writing into memory if $\overline{CE1}$, $\overline{CE2}$, and $\overline{ST}$ = "0".
D_{out} enabled in active state	0	0	X	1	X	A	If $\overline{ST}$ = "1", the output stores and reads the previous data from or written into memory.
Read addressed memory location into output latch.	0	0	0	1	X	A	The output reads the present contents that are addressed.
	1	0	0	1	X	R	The addressed location is read into output latch with output in the "R" state.
Disable reading from memory	X	1	X	X	X	R	Address changing can take place in this condition.
	X	X	1	X	X	R/A	
Write into memory	0	0	0	0	A	R	D_{in} is written into memory and into the output latch
Write disabled	1	X	X	X	X	R	$\overline{WE}$ = "1" is a read enable.
	X	1	X	X	X	R	$\overline{WE}$ = "0" is a write enable.
	X	X	1	X	X	R/A	
	X	X	X	1	X	R/A	

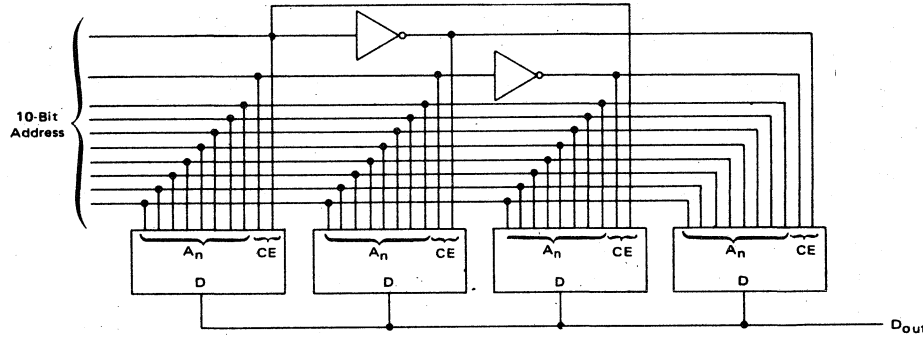
R = High resistance state at D_{out}
A = An active level of either V_{SS} or V_{DD}
R/A = An R or A condition depending on the don't care condition
X = Don't care condition (must be in the "1" or "0" state)
1 = A high level at V_{DD}
0 = A low level at V_{SS}

TYPICAL APPLICATION FOR SERIAL WORDS UTILIZING BUS TECHNIQUES

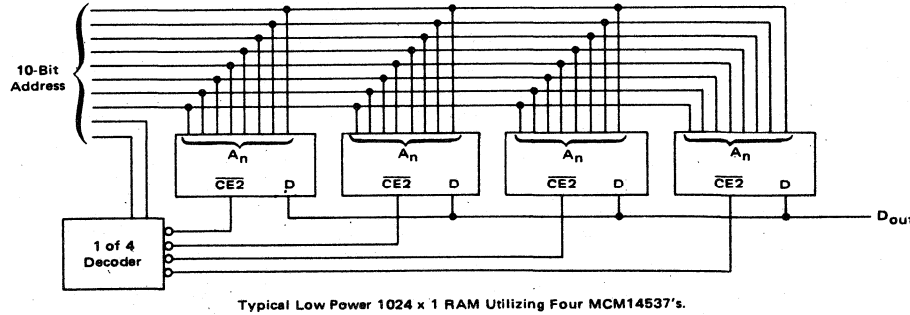


$T_{word} = t_{acc}(\overline{ST}) + (n-1)\, t_{acc}(\overline{CE1})$

$T_{word(typ)} = 3.8\ \mu s$ for a 32-bit serial word at $V_{DD} = 10$ V



Typical 1024 x 1 RAM Utilizing Four MCM14537's.



Typical Low Power 1024 x 1 RAM Utilizing Four MCM14537's.

MOTOROLA

MC14538B

CMOS MSI

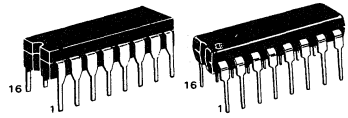
(LOW-POWER COMPLEMENTARY MOS)

DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X. Linear CMOS techniques allow more precise control of output pulse width.

- ±1.0% Typical Pulsewidth Variation from Part to Part
- ±0.5% Typical Pulsewidth Variation over Temperature Range
- New Formula: T = RC (T in seconds, R in ohms, C in farads)
- Pulse Width Range = 10 μs to ∞
- Symmetrical Output Sink and Source Capability
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- Quiescent Current (Standby) = 5.0 nA/package typical @ 5 Vdc
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive or Negative-Going Edge
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-pin Compatible with MC14528B and CD4528B (CD4098)
- For Pulse Widths Less Than 10 μs the MC14528B is Recommended



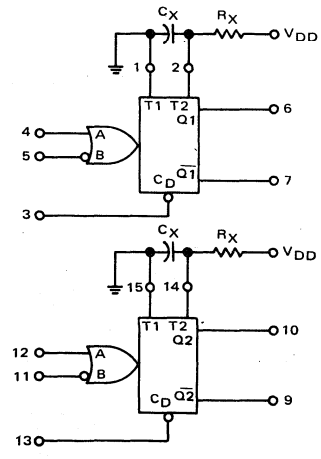
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



R_X and C_X are external components.

V_{DD} = Pin 16
V_{SS} = Pin 8, Pin 1, Pin 15

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage#	"0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)			5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)			10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)			15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)			5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)			10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)			15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	3.6	–	3.0	8.8	–	2.4	–	
Input Current, Pin 2 or 14		I_{in}	15	–	±0.02	–	±0.00001	±.05	–	±0.5	μAdc
Input Current, Other Inputs (AL Device)		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current, Other Inputs (CL/CP Device)		I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance, Pin 2 or 14		C_{in}	–	–	–	–	25	–	–	–	pF
Input Capacitance, Other Inputs (V_{in} = 0)		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)		I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)			10	–	10	–	0.010	10	–	300	
			15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)		I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)			10	–	40	–	0.010	40	–	300	
			15	–	80	–	0.015	80	–	600	
Quiescent Current, Active State		I_{DD}	5.0	–	–	–	35	–	–	–	μAdc
(Q1 = Logic 1)			10	–	–	–	80	–	–	–	
(Q2 = Logic 0)			15	–	–	–	125	–	–	–	
**Total Supply Current at an external load capacitance (C_L) and at external timing network (R_X, C_X)		I_T	5.0	$I_T = (3.5 \times 10^{-2}) R_X C_X f + 4 C_X f + 1 \times 10^{-5} C_L f$							
			10.0	$I_T = (8 \times 10^{-2}) R_X C_X f + 9 C_X f + 2 \times 10^{-5} C_L f$							
			15.0	$I_T = (1.25 \times 10^{-1}) R_X C_X f + 12 C_X f + 3 \times 10^{-5} C_L f$							
				where: I_T in μA (one monostable switching only), C_X in μF, C_L in pF, R_X in k ohms, and f in Hz is the input frequency.							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
A or B to Q or $\overline{Q}$						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 255 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 97 ns		15	–	100	220	
C_D to Q or $\overline{Q}$						ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 205 ns		5.0	–	250	500	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 82 ns		15	–	95	190	
Input Pulse Width	t_{WH},	5.0	70	35	–	ns
A, B or C_D	t_{WL}	10	60	30	–	
		15	50	25	–	
Retrigger Time	t_{rr}	5.0	0	–	–	ns
		10	0	–	–	
		15	0	–	–	
Output Pulse Width — Q or $\overline{Q}$	T					μs
Refer to Figure 9 for other values of R_X and C_X.						
C_X = 0.002 μF, R_X = 100 kΩ		5.0	210	222	234	
		10	212	224	236	
		15	214	226	238	
C_X = 0.1 μF, R_X = 100 kΩ		5.0	9.3	9.86	10.4	ms
		10	9.5	10	10.5	
		15	9.6	10.14	10.7	
C_X = 10 μF, R_X = 100 kΩ		5.0	0.915	0.965	1.015	s
		10	0.93	0.98	1.03	
		15	0.94	0.99	1.04	
Pulse Width Match between circuits in	$\frac{100(T_1 - T_2)}{T_1}$	5.0	–	±1	–	%
the same package.		10	–	±1	–	
C_X = 0.1 μF, R_X = 100 kΩ		15	–	±1	–	

OPERATING CONDITIONS

External Timing Resistance	R_X	–	5.0	–	*	kΩ
External Timing Capacitance	C_X	–	0	–	No Limit	pF

*The maximum usable resistance R_X is a function of the leakage of the capacitor C_X, leakage of the MC14538B, and leakage due to board layout and surface resistance.

FIGURE 1 – LOGIC DIAGRAM
(1/2 of Device Shown)

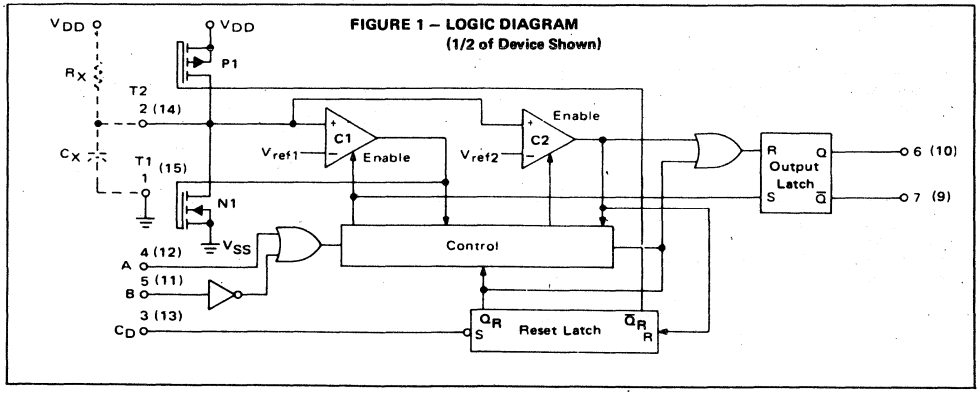


FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

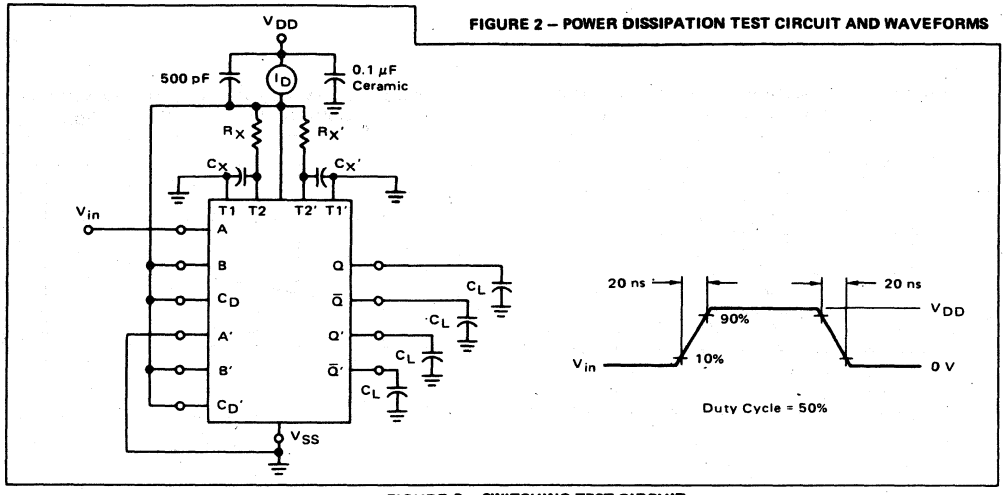
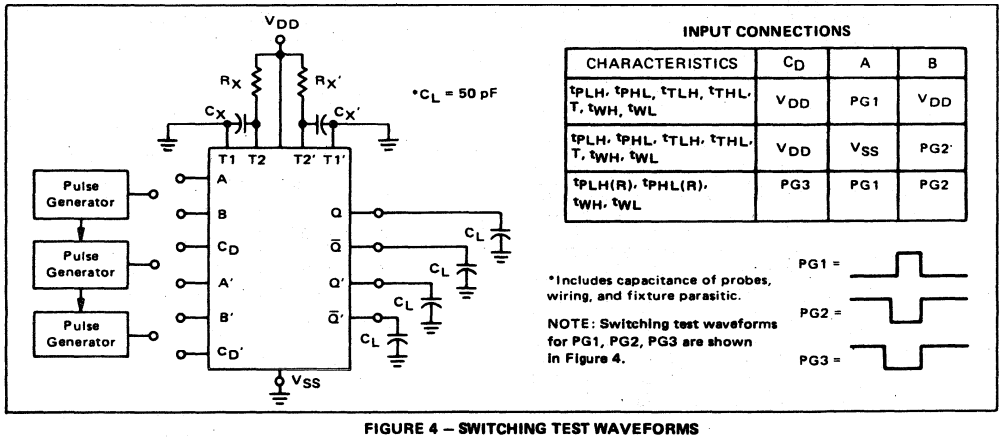


FIGURE 3 – SWITCHING TEST CIRCUIT



INPUT CONNECTIONS

CHARACTERISTICS	C_D	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_{WH}, t_{WL}	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: Switching test waveforms for PG1, PG2, PG3 are shown in Figure 4.

PG1 =

PG2 =

PG3 =

FIGURE 4 – SWITCHING TEST WAVEFORMS

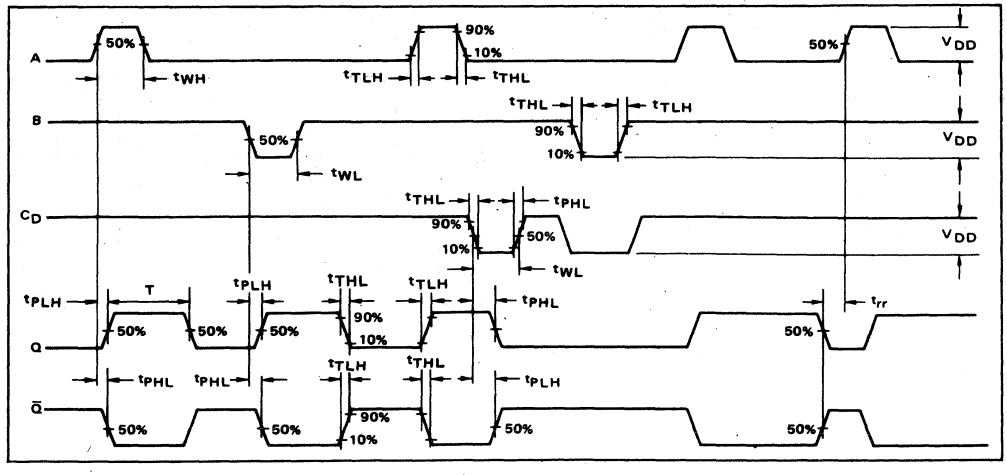


FIGURE 5 – TYPICAL NORMALIZED DISTRIBUTION OF UNITS FOR OUTPUT PULSE WIDTH

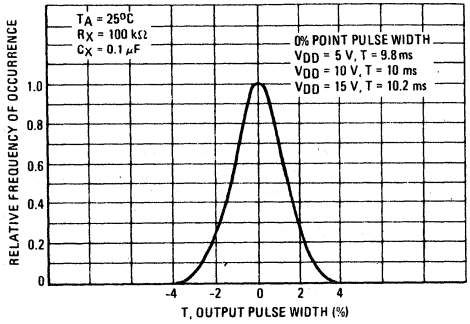


FIGURE 6 – TYPICAL PULSE WIDTH VARIATION AS A FUNCTION OF SUPPLY VOLTAGE V_{DD}

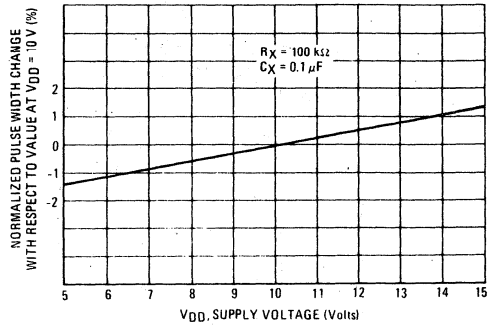


FIGURE 7 – TYPICAL TOTAL SUPPLY CURRENT versus OUTPUT DUTY CYCLE

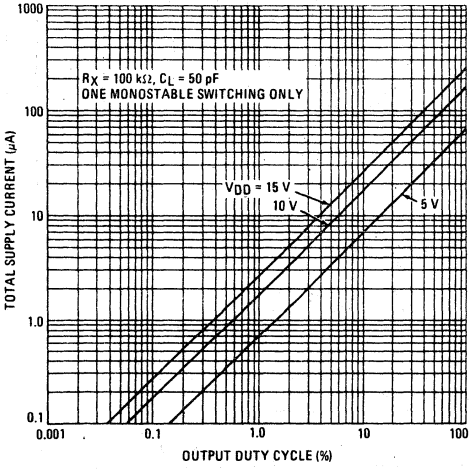


FIGURE 7 – TYPICAL PULSE WIDTH ERROR versus TEMPERATURE

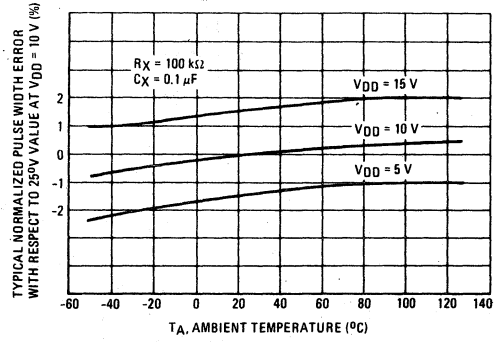
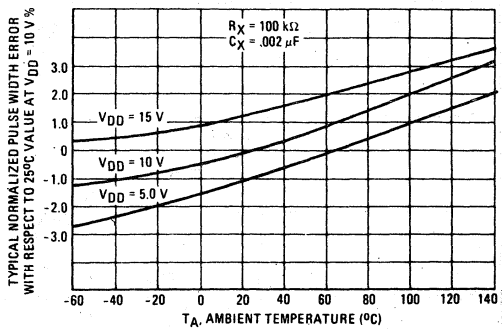
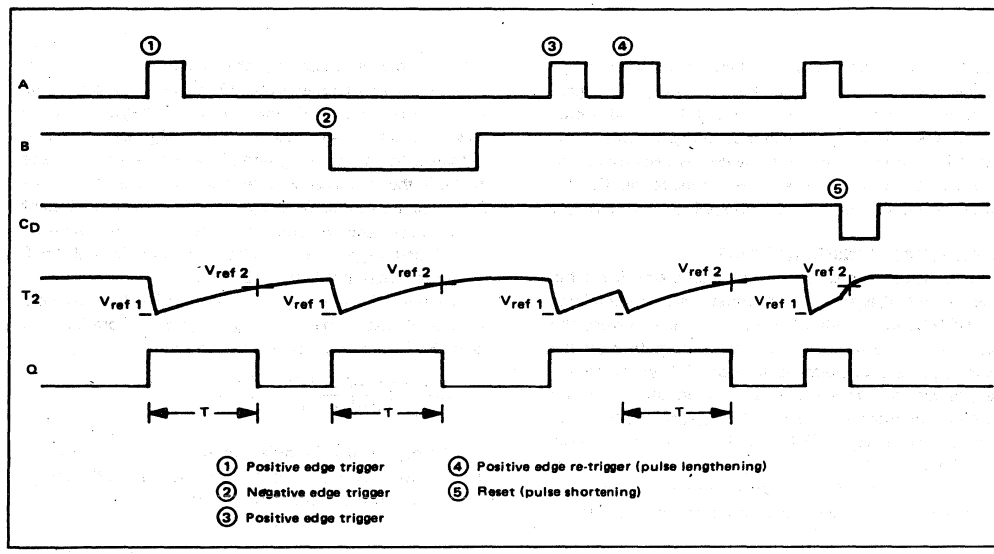


FIGURE 9– TYPICAL PULSE WIDTH ERROR versus TEMPERATURE



THEORY OF OPERATION

FIGURE 10 – Timing Operation



TRIGGER OPERATION

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figures 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and C_D are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1①. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until $V_{ref\ 1}$ is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals $V_{ref\ 2}$, comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2②. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

It should be noted that in the quiescent state C_X is fully charged to V_{DD} causing the current through resistor R_X to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

RETRIGGER OPERATION

The MC14538B is retriggered if a valid trigger occurs ③followed by another valid trigger④before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from $V_{ref\ 1}$, but has not yet reached $V_{ref\ 2}$, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at T2 will again drop to $V_{ref\ 1}$ before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on C_D sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor P1⑤. When the voltage on the capacitor reaches $V_{ref\ 2}$, the

reset latch will clear, and will then be ready to accept another pulse. If the C_D input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

POWER-DOWN CONSIDERATIONS

Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the MC14538B (or MC14528B) is powered down, the capacitor voltage may discharge from V_{DD} through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the V_{DD} supply must not be faster than $(V_{DD}) \cdot (C)/(10\ mA)$. For example, if V_{DD} = 10 V and C_X = 10 μF, the V_{DD} supply should discharge no faster than (10 V) x (10 μF)/(10 mA) = 10 ms. This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

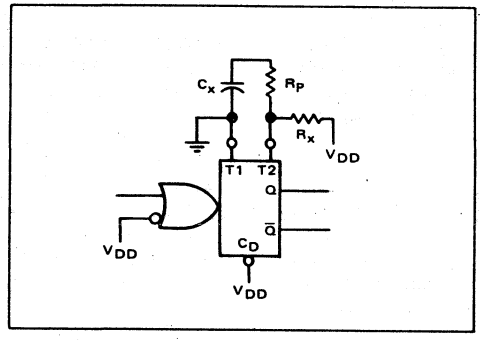
When a more rapid decrease of V_{DD} to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility, a protection resistor, R_p, can be placed between the capacitor C_X and pin 2 (or 14) of the device to limit the discharge current from the capacitor to the V_{DD} supply. Internally, the protection diode is equivalent to a diode and resistor connected in series between pin T2 and V_{DD}. The diode has a forward drop of 0.625 V and the resistance is about 250 Ω.

To limit the discharge current to 10 mA under conditions of instantaneous change of pin 16 from V_{DD} to V_{SS}. Rp is calculated from the equation:

$$Rp = \frac{(V_{DD} - 0.625V)}{(0.010\ Amp)} - 250\ \Omega$$

The pulse width formula now changes from $T = R_X C_X$ to $T = (R_X + Rp)\ C_X$. Figure 11 demonstrates the proper connection of the protection resistor.

FIGURE 11 – Use of a Resistor to Limit Power Down Current Surge



TYPICAL APPLICATIONS

FIGURE 12 – Retriggerable Monostables Circuitry

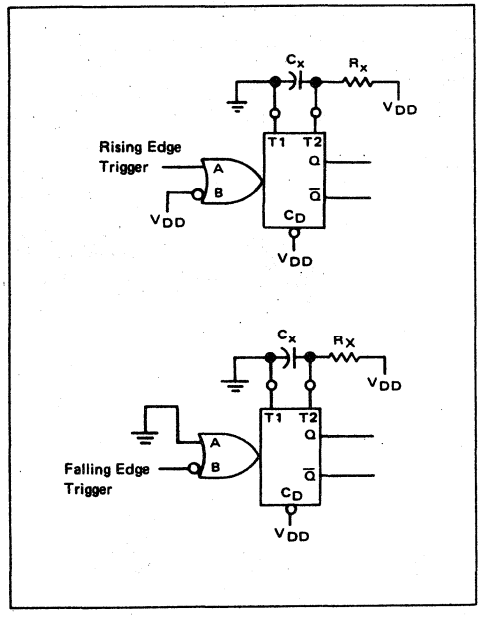


FIGURE 13 – Non-retriggerable Monostables Circuitry

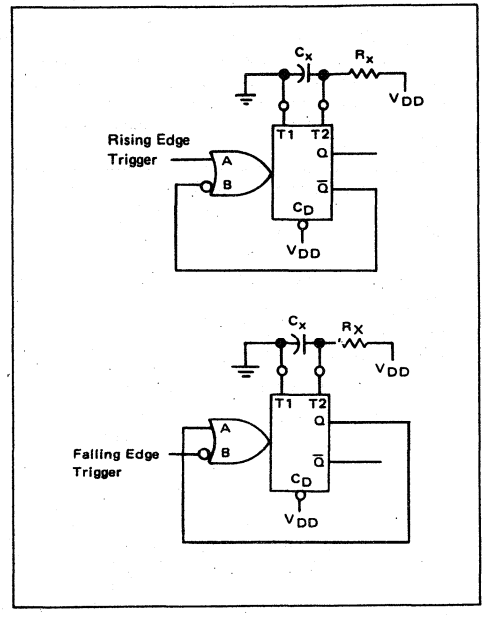


FIGURE 14 – Reduction of Power-Up Output Pulse Width

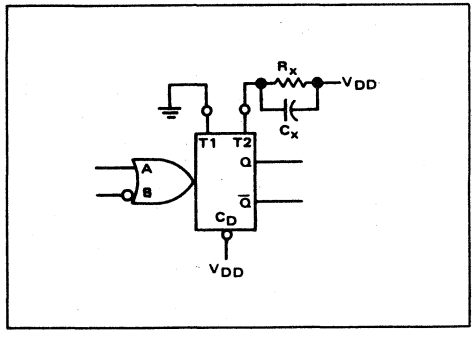
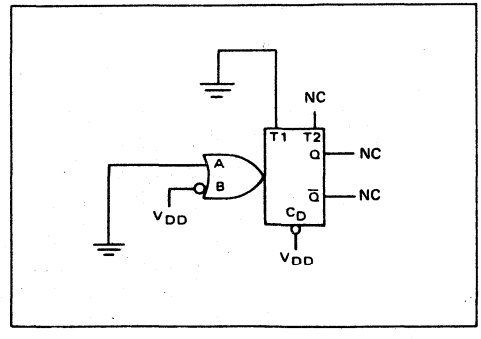


FIGURE 15 – Connection of Unused Sections



MOTOROLA

MC14539B

DUAL 4-CHANNEL DATA SELECTOR/MULTIPLEXER

The MC14539B data selector/multiplexer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of two sections of four inputs each. One input from each section is selected by the address inputs A and B. A "high" on the Strobe input will cause the output to remain "low".

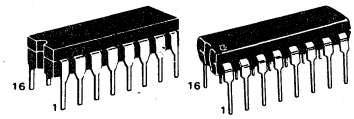
This device finds primary application in signal multiplexing functions. It permits multiplexing from N-lines to l-line, and can also perform parallel-to-serial conversion. The Strobe input allows cascading of n-lines to n-lines.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- High Fanout >50
- Input Impedance = 10^{12} ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-CHANNEL
DATA SELECTOR/MULTIPLEXER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

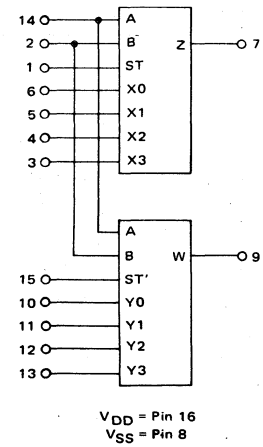
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range -- AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS					
		X3	X2	X1	X0		OUTPUTS
B	A	Y3	Y2	Y1	Y0	ST,ST'	Z, W
X	X	X	X	X	X	1	0
0	0	X	X	X	0	0	0
0	0	X	X	X	1	0	1
0	1	X	X	0	X	0	0
0	1	X	X	1	X	0	1
1	0	X	0	X	X	0	0
1	0	X	1	X	X	0	1
1	1	0	X	X	X	0	0
1	1	1	X	X	X	0	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15		20	–	0.015	20		600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.85\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (1.7\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (2.6\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

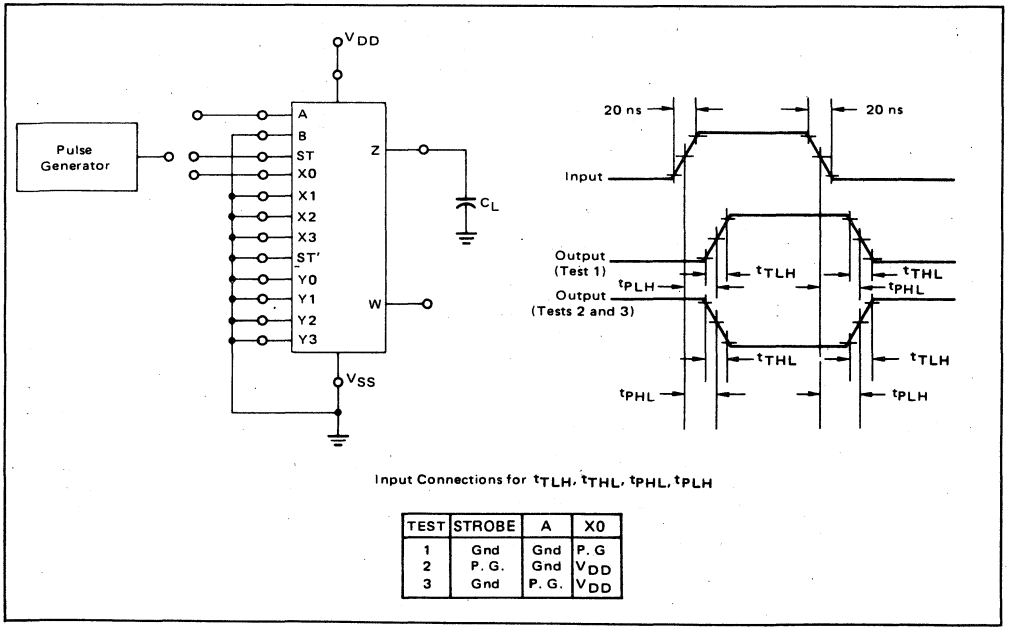
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
X, Y Input to Output						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 125 ns		5.0	–	210	420	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} = (0.55 ns/pF) C_L + 45 ns		15	–	70	140	
A Input to Output	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 140 ns		5.0	–	225	450	
t_{PLH} = (0.66 ns/pF) C_L + 77 ns		10	–	110	220	
t_{PLH} = (0.5 ns/pF) C_L + 60 ns		15	–	85	170	
t_{PHL} = (1.7 ns/pF) C_L + 160 ns	t_{PHL}	5.0	–	245	490	ns
t_{PHL} = (0.66 ns/pF) C_L + 82 ns		10	–	115	230	
t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	
Strobe Input to Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 60 ns		5.0	–	145	290	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	

*The formula given is for the typical characteristics only.

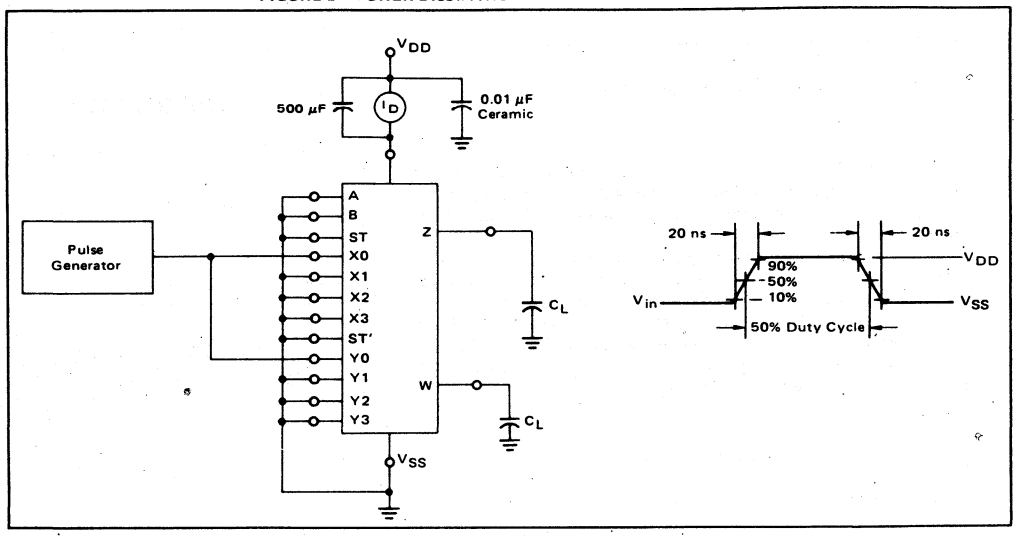
FIGURE 1 – AC TEST CIRCUIT AND WAVEFORMS



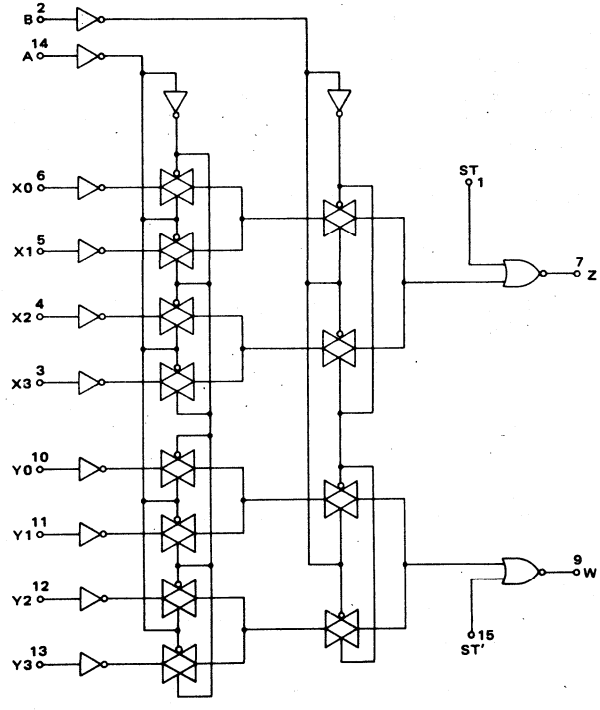
Input Connections for t_{TLH}, t_{THL}, t_{PHL}, t_{PLH}

TEST	STROBE	A	X0
1	Gnd	Gnd	P. G
2	P. G.	Gnd	V_{DD}
3	Gnd	P. G.	V_{DD}

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



LOGIC DIAGRAM



MOTOROLA

MC14541B

PROGRAMMABLE TIMER

The MC14541B programmable timer consists of a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the power-on reset is enabled and initializes the counter, within the specified V_{DD} range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency (f_{osc}) with the n^{th} stage frequency being $f_{osc}/2^n$.

- Available Outputs 2^8, 2^{10}, 2^{13} or 2^{16}
- Increments on Positive Edge Clock Transitions
- Low Symmetrical Output Resistance (typically 100 Ω @ 15 Vdc)
- Built-in Low Power RC Oscillator (±2% accuracy over temperature range and ± 10% supply and ±3% over processing @ <10 kHz)
- Oscillator Frequency Range ≈ DC to 100 kHz
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- Automatic Reset Initializes All Counters When Power Turns On (Limits – V_{DD} from 8.5 Vdc to 18 Vdc when enabled)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as 2^n Frequency Divider or Single Transition Timer
- Q/Q Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow Clock Rise and Fall Times
- Supply Voltage Range = 3.0 Vdc to 18 Vdc

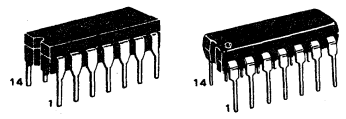
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	45	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

OSCILLATOR/TIMER



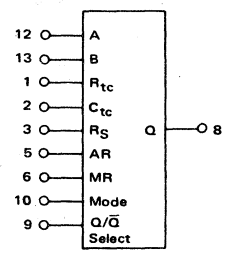
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	7.96	–	6.42	12.83	–	4.49	–	
(V_{OH} = 9.5 Vdc)		10	4.19	–	3.38	6.75	–	2.37	–	
(V_{OH} = 13.5 Vdc)		15	16.3	–	13.2	26.33	–	9.24	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.93	–	1.56	3.12	–	1.09	–	mAdc
(V_{OL} = 0.5 Vdc)		10	4.96	–	4.0	8.0	–	2.8	–	
(V_{OL} = 1.5 Vdc)		15	19.3	–	15.6	31.2	–	10.9	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	5.1	–	4.27	12.83	–	3.5	–	
(V_{OH} = 9.5 Vdc)		10	2.69	–	2.25	6.75	–	1.85	–	
(V_{OH} = 13.5 Vdc)		15	10.5	–	8.8	26.33	–	7.22	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.24	–	1.04	3.12	–	0.85	–	
(V_{OL} = 0.5 Vdc)		10	3.18	–	2.66	8.0	–	2.18	–	
(V_{OL} = 1.5 Vdc)		15	12.4	–	10.4	31.2	–	8.50	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)										μAdc
		5.0	–	5.0	–	0.005	5.0	–	150	
(Pin 5 is High)	I_{DD}	10	–	10	–	0.010	10	–	300	
Auto Reset Disabled		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)										μAdc
		5.0	–	20	–	0.005	20	–	150	
(Pin 5 is High)	I_{DD}	10	–	40	–	0.010	40	–	300	
Auto Reset Disabled		15	–	80	–	0.015	80	–	600	
Auto Reset Quiescent Current										μAdc
		5.0	–	200	–	7	200	–	1200	
	I_{DDR}	10	–	250	–	30	250	–	1500	
(Pin 5 is low)		15	–	500	–	82	500	–	2000	
Supply Current**† (Dynamic plus Quiescent)	I_D	5.0	I_D = (0.4 μA/kHz) f + I_{DD}							μAdc
		10	I_D = (0.8 μA/kHz) f + I_{DD}							
		15	I_D = (1.2 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†When using the on chip oscillator the total supply current (in μAdc) becomes : $I_T = I_D + 2 C_{tc} V_{DD} f \times 10^{-3}$ where I_D is in μA, C_{tc} is in pF, V_{DD} in Volts DC, and f in kHz. (see fig. 3)
Dissipation during power-on with automatic reset enabled is typically 50μA @ V_{DD} = 10Vdc.

**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISITCS* (C_L = 50 pF, T_A = 25°C)

Characteristic	V_{DD} Symbol	Typical Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Turn-Off, Turn-On Clock to Q (2^8 Output)	t_{PLH}					µs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3415 ns	t_{PHL}	5.0	–	3.5	10.5	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1217 ns		10	–	1.25	3.8	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 875 ns		15	–	0.9	2.9	
Turn-On, Turn-Off Clock to Q (2^{16} Output)	t_{PHL}					µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns	t_{PLH}	5.0	–	6.0	18	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 3467 ns		10	–	3.5	10	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2475 ns		15	–	2.5	7.5	
Clock Pulse Width	$t_{WH(cl)}$	5.0	900	300	–	ns
		10	300	100	–	
		15	225	85	–	
Clock Pulse Frequency	f_{cl}	5.0	–	1.5	–	MHz
		10	–	4.0	–	
		15	–	6.0	–	
MR Pulse Width	$t_{WH(R)}$	5.0	900	300	–	ns
		10	300	100	–	
		15	225	85	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

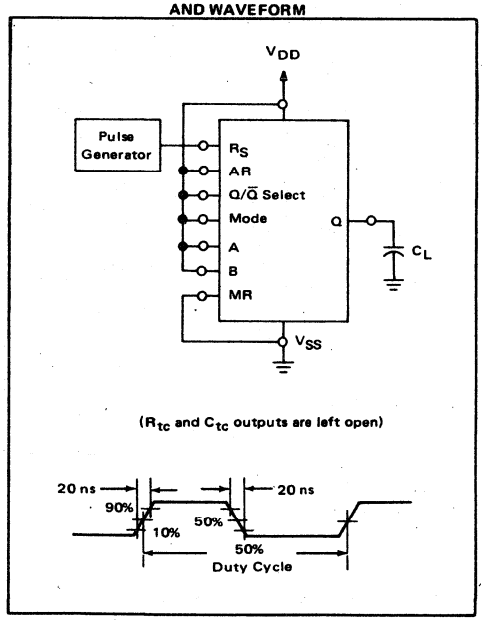
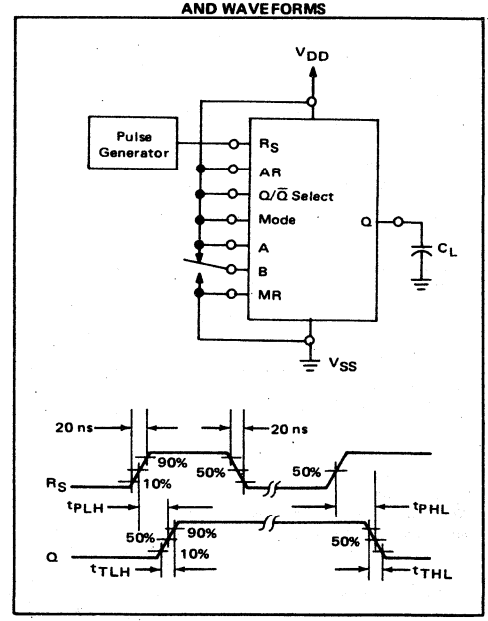
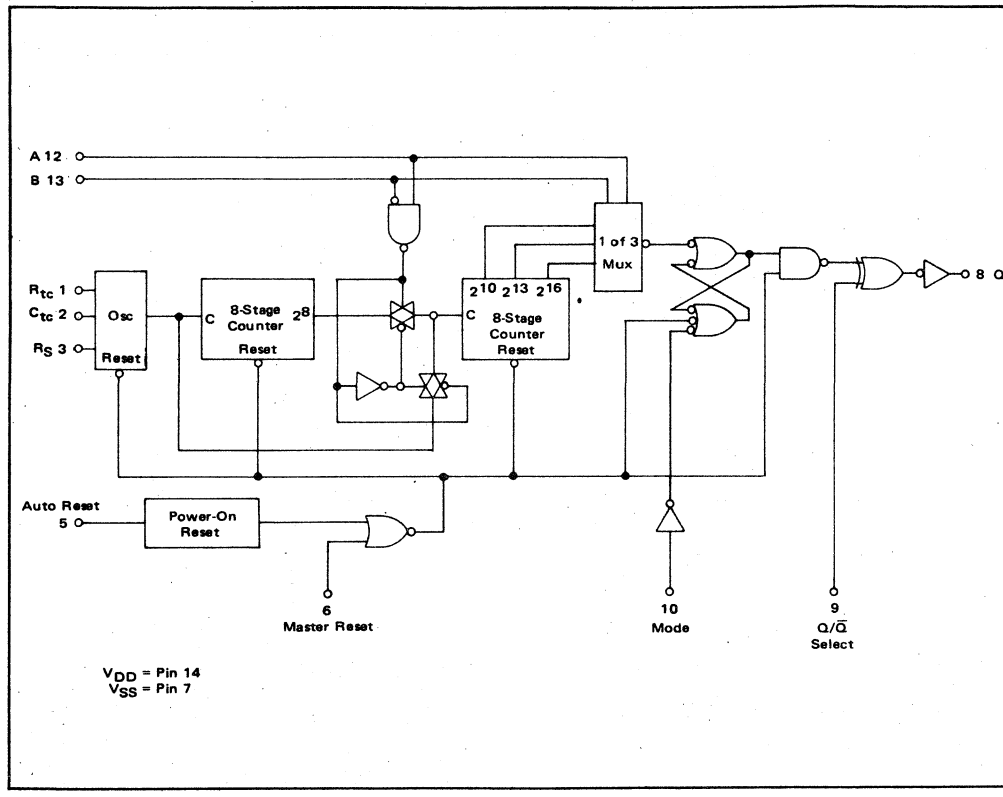


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



EXPANDED BLOCK DIAGRAM



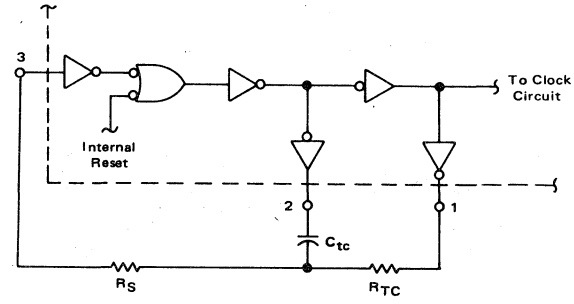
FREQUENCY SELECTION TABLE

A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

	State	
Pin	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset On
9	Output Initially Low After Reset	Output Initially High After Reset
10	Single Cycle Mode	Recycle Mode

FIGURE 3 – OSCILLATOR CIRCUIT USING RC CONFIGURATION



TYPICAL RC OSCILLATOR CHARACTERISTICS

FIGURE 4 – RC OSCILLATOR STABILITY

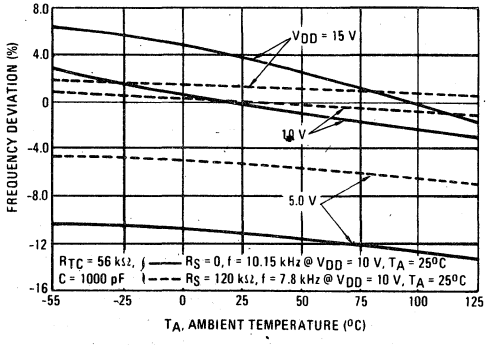
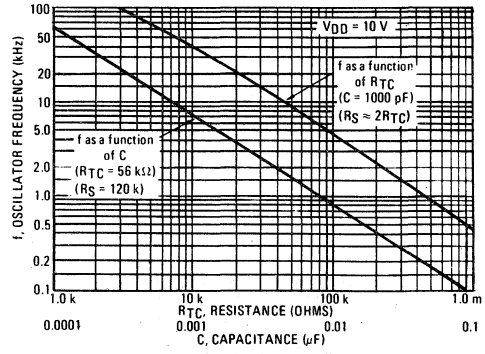


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C



OPERATING CHARACTERISTICS

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a "1" provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

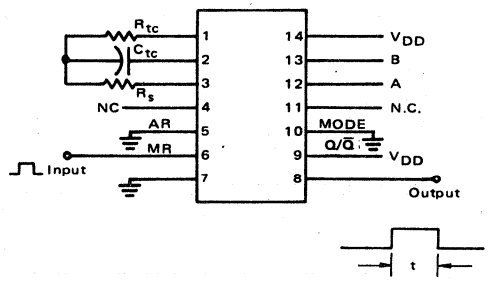
$$f = \frac{1}{2.3\,R_{tc}C_{tc}} \quad \text{if } (1\text{ kHz} \leqslant f \leqslant 100\text{ kHz})$$

and $R_S \approx 2\,R_{tc}$ where $R_S \geqslant 10\,k\Omega$

The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13} and 2^{16}). The 2^n counts as shown in the Frequency Selection Table represents the Q output of the N^{th} stage of the counter. When A is "1", 2^{16} is selected for both states of B. However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputing 2^8).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/$\overline{Q}$ select pin is set to a "0" the Q output is a "0", correspondingly when Q/$\overline{Q}$ select pin is set to a "1" the Q output is a "1".

When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop (see Expanded Block Diagram) resets, counting commenced and after 2^{n-1} counts the RS flip-flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.



DIGITAL TIMER APPLICATION

When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high until the selected (via A and B) number of clock pulses are counted, the Q output then goes low and remains low until another input pulse is received.

This "one shot" is fully retriggerable and as accurate as the input frequency. An external clock can be used (pin 3 is the clock input, pins 1 and 2 are outputs) if additional accuracy is needed.

Notice that a setup time equal to the desired pulse width output is required immediately following initial power up, during which time Q output will be high.

MOTOROLA

MC14543B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

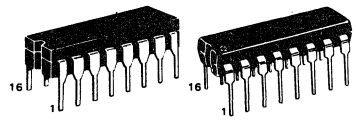
BCD-TO-SEVEN SEGMENT
LATCH/DECODER/DRIVER
for
LIQUID CRYSTALS

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER for LIQUID CRYSTALS

The MC14543B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. the outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Logic Circuit Quiescent Current = 5.0nA/package typical @ 5 Vdc
- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4056A (with Pin 7 Tied to V_{SS}).



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Rance	T_{stg}	−65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I_{OHmax} I_{OLmax}	10	mAdc
Maximum Continuous Output Power* (Source or Sink) per Output	P_{OHmax} P_{OLmax}	70	mW

*$P_{OHmax} = I_{OH}(V_{OH} - V_{DD})$ and $P_{OLmax} = I_{OL}(V_{OL} - V_{SS})$

TRUTH TABLE

INPUTS							OUTPUTS							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							*
†	†	1	†				Inverse of Output Combinations Above							Display as above

X = Don't care
† = Above Combinations
* = For liquid crystal readouts, apply a square wave to Ph.
For common cathode LED readouts, select Ph = 0.
For common anode LED readouts, select Ph = 1.
** = Depends upon the BCD code previously applied when LD = 1.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0,05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 0.5 Vdc)		10	–	–	–	–8.7	–	–	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 9.5 Vdc)		10	–	–	–	10.1	–	–	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 0.5 Vdc)		10	–	–	–	–8.7	–	–	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 9.5 Vdc)		10	–	–	–	10.1	–	–	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1		±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3		±0.00001	±0.3		±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5			pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15		20	–	0.015	20		600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.6 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.1 μA/kHz) f + I_{DD}							
		15	I_T = (4.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	110	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 520 ns		5.0	–	605	1210	
t_{PLH} = (0.66 ns/pF) C_L + 217 ns		10	–	250	500	
t_{PLH} = (0.5 ns/pF) C_L + 160 ns		15	–	185	370	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 420 ns		5.0	–	505	1650	
t_{PHL} = (0.66 ns/pF) C_L + 172 ns		10	–	205	660	
t_{PHL} = (0.5 ns/pF) C_L + 130 ns		15	–	155	495	
Setup Time	t_{su}	5.0	0	-40	–	ns
		10	0	-15	–	
		15	0	-10	–	
Hold Time	t_h	5.0	80	40	–	ns
		10	30	15	–	
		15	20	10	–	
Latch Disable Pulse Width (Strobing Data)	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	

*The formula given is for the typical characteristics only.

LOGIC DIAGRAM

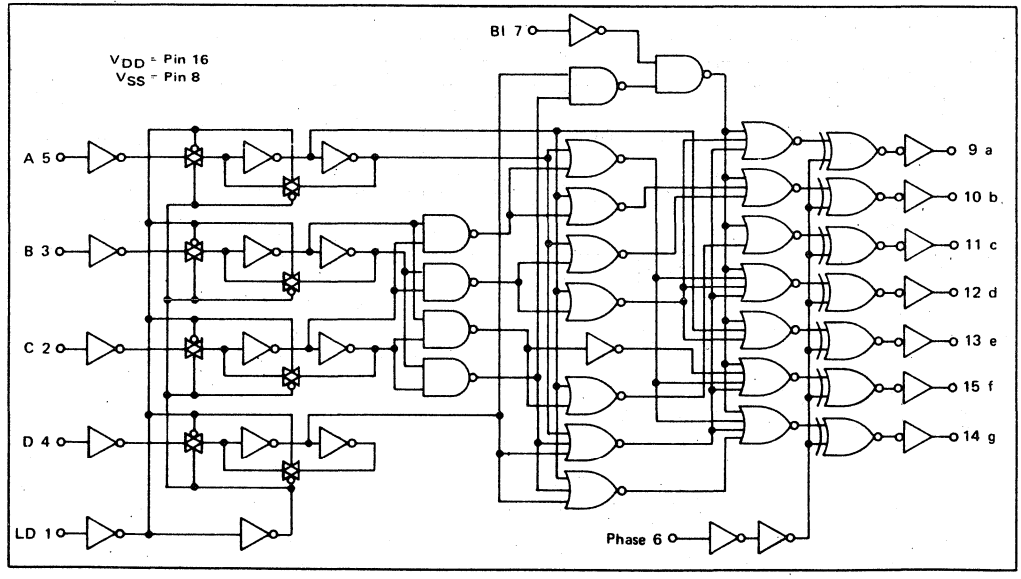


FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

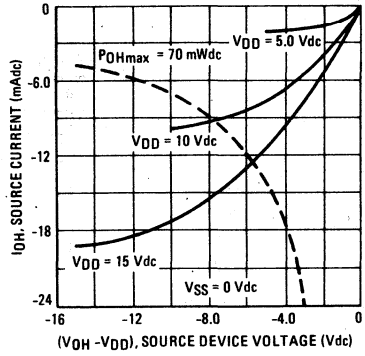


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS

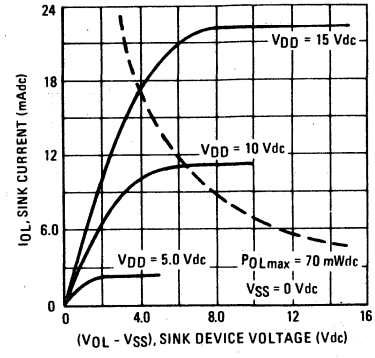


FIGURE 3 – DYNAMIC POWER DISIPATION SIGNAL WAVEFORMS

Inputs BI and Ph low, and Inputs D and LD high. f in respect to a system clock.

All outputs connected to respective C_L loads.

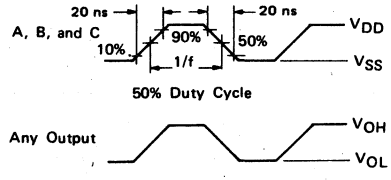
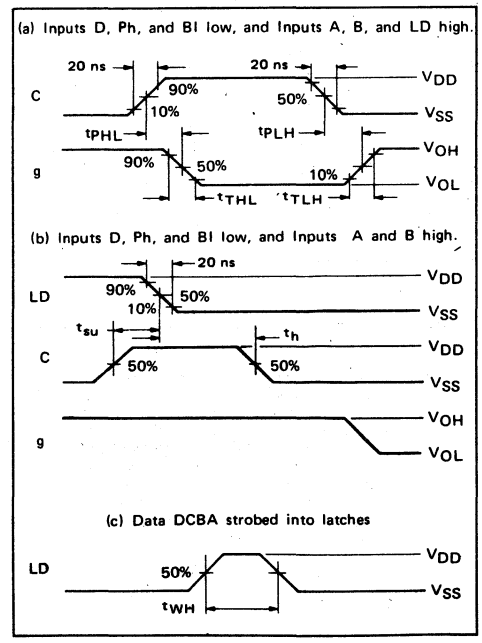
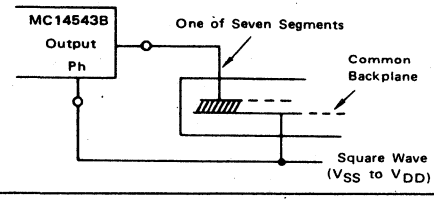


FIGURE 4 – DYNAMIC SIGNAL WAVEFORMS

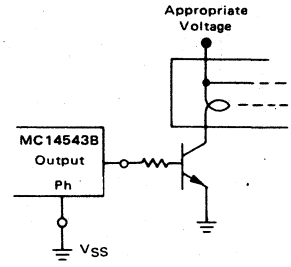


CONNECTIONS TO VARIOUS DISPLAY READOUTS

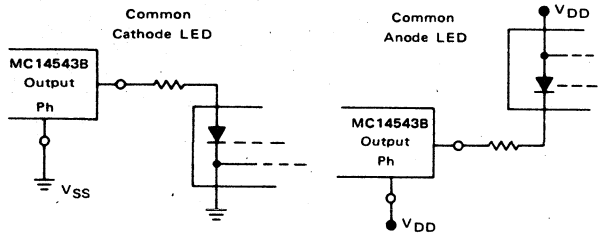
LIQUID CRYSTAL (LC) READOUT



INCANDESCENT READOUT

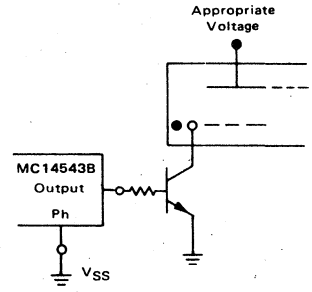


LIGHT EMITTING DIODE (LED) READOUT

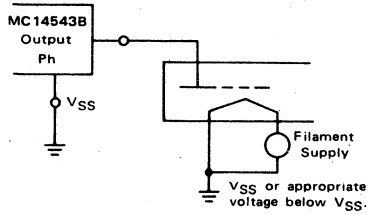


Note: Bipolar transistors may be added for gain (for $V_{DD} \leq 10V$ or $I_{out} \geq 10$ mA).

GAS DISCHARGE READOUT

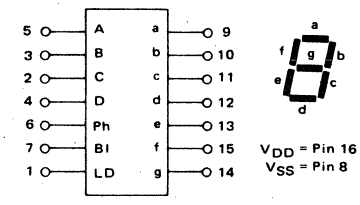


FLUORESCENT READOUT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).



MOTOROLA

MC14544B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER for LIQUID CRYSTALS

The MC14544B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. The Ripple Blanking Input (RBI) and the Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes.

For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

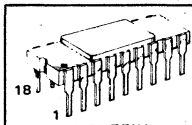
Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Logic Circuit Quiescent Current = 5.0nA/package typical @ 5 Vdc
- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capability for Suppression of Non-significant zero
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4056A (with Pin 7 Tied to V

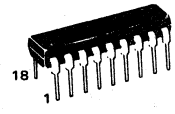
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER WITH RIPPLE BLANKING



L SUFFIX
CERAMIC PACKAGE
CASE 680

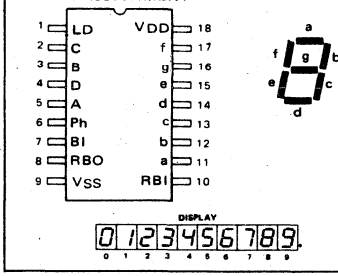


P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Rance	T_{stg}	−65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I_{OHmax} I_{OLmax}	10	mAdc
Maximum Continuous Output Power* (Source or Sink) per Output	P_{OHmax} P_{OLmax}	70	mW

*$P_{OHmax} = I_{OH}(V_{OH} - V_{DD})$ and $P_{OLmax} = I_{OL}(V_{OL} - V_{SS})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 0.5 Vdc)		10	–	–	–	–8.7	–	–	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 9.5 Vdc)		10	–	–	–	10.1	–	–	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 0.5 Vdc)		10	–	–	–	–8.7	–	–	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 9.5 Vdc)		10	–	–	–	10.1	–	–	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.6 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.1 µA/kHz) f + I_{DD}							
		15	I_T = (4.7 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

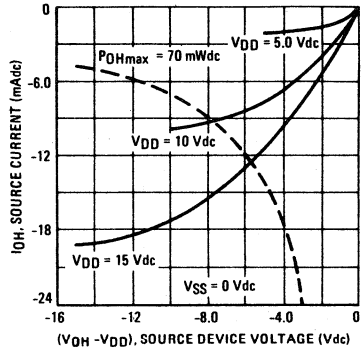


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS

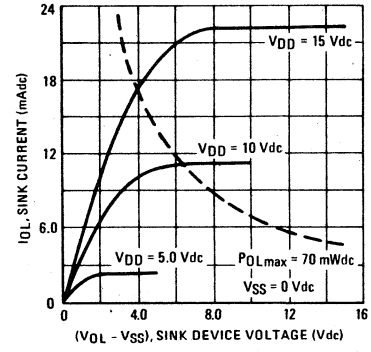


FIGURE 3 – DYNAMIC POWER DISIPATION SIGNAL WAVEFORMS

Inputs BI and Ph low, and Inputs D and LD high.
f in respect to a system clock.

All outputs connected to respective C_L loads.

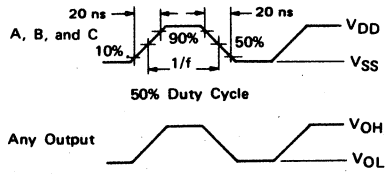
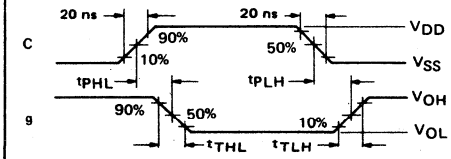
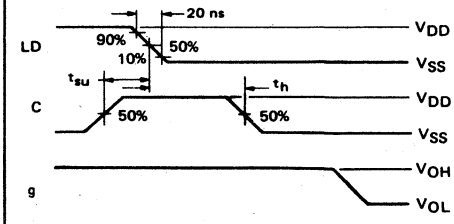


FIGURE 4 – DYNAMIC SIGNAL WAVEFORMS

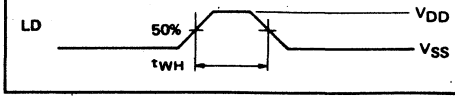
(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.



(b) Inputs D, Ph, and BI low, and Inputs A and B high.

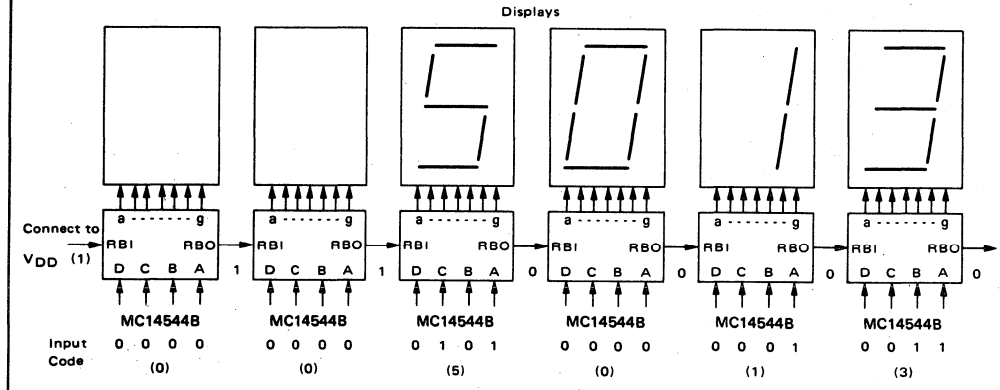


(c) Data DCBA strobed into latches

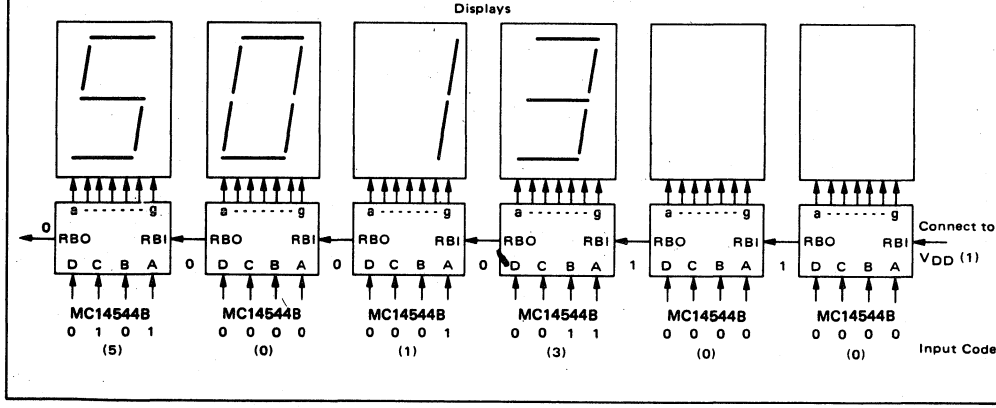


TYPICAL APPLICATIONS FOR RIPPLE BLANKING

LEADING EDGE ZERO SUPPRESSION



TRAILING EDGE ZERO SUPPRESSION

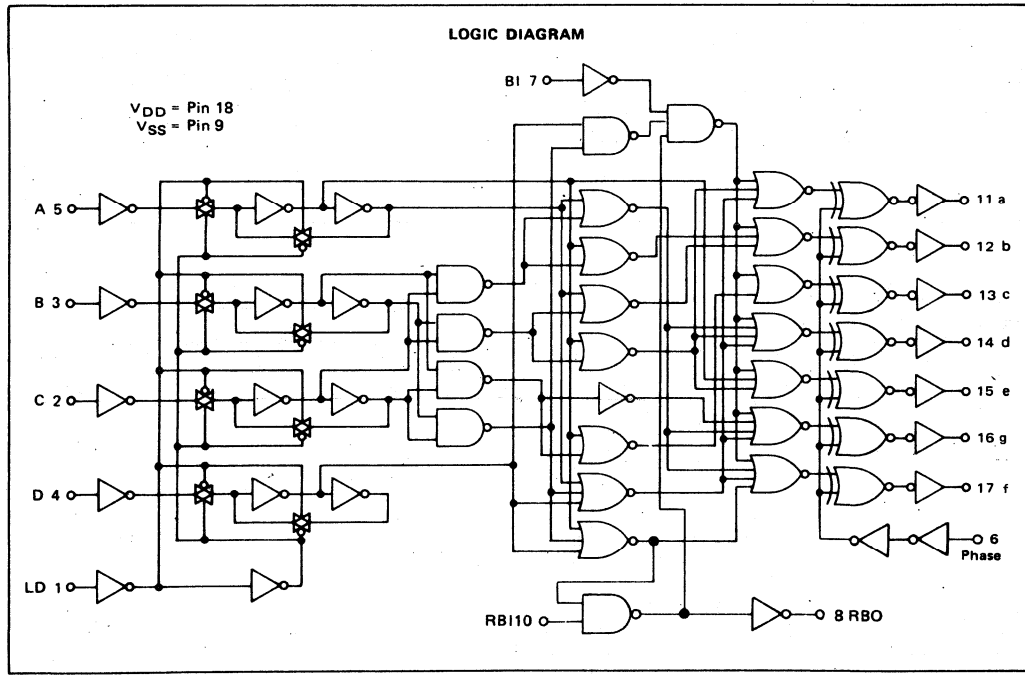


SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

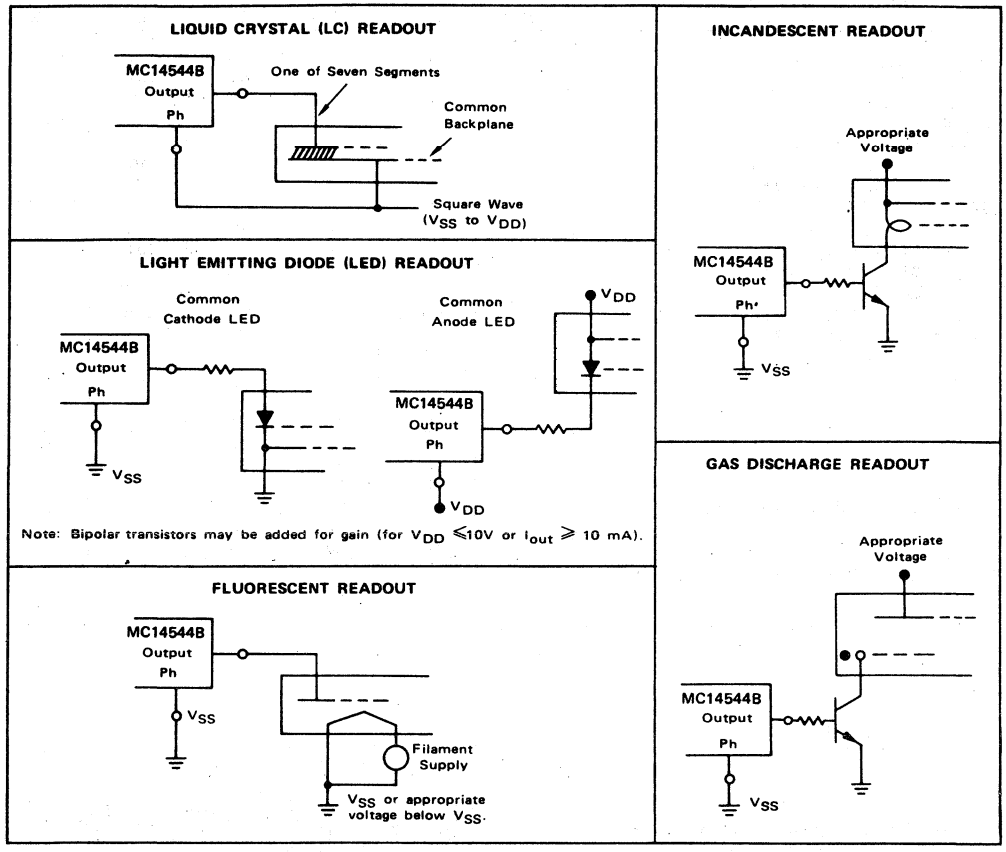
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	110	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 520 ns		5.0	–	605	1210	
t_{PLH} = (0.66 ns/pF) C_L + 217 ns		10	–	250	500	
t_{PLH} = (0.5 ns/pF) C_L + 160 ns		15	–	185	370	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 420 ns		5.0	–	505	1650	
t_{PHL} = (0.66 ns/pF) C_L + 172 ns		10	–	205	660	
t_{PHL} = (0.5 ns/pF) C_L + 130 ns		15	–	155	495	
Setup Time	t_{su}	5.0	0	-40	–	ns
		10	0	-15	–	
		15	0	-10	–	
Hold Time	t_h	5.0	80	40	–	ns
		10	30	15	–	
		15	20	10	–	
Latch Disable Pulse Width (Strobing Data)	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	

*The formula given is for the typical characteristics only.

LOGIC DIAGRAM



CONNECTIONS TO VARIOUS DISPLAY READOUTS



TRUTH TABLE

INPUTS								OUTPUTS								
RBI	LD	BI	Ph	D	C	B	A	RBO	a	b	c	d	e	f	g	DISPLAY
X	X	1	0	X	X	X	X	#	0	0	0	0	0	0	0	Blank
1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0
X	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	1
X	1	0	0	0	0	1	0	0	1	1	0	1	1	0	1	2
X	1	0	0	0	0	1	1	0	1	1	1	1	0	0	1	3
X	1	0	0	0	1	0	0	0	0	1	1	0	0	1	1	4
X	1	0	0	0	1	0	1	0	1	0	1	1	0	1	1	5
X	1	0	0	0	1	1	0	0	1	0	1	1	1	1	1	6
X	1	0	0	0	1	1	1	0	1	1	1	0	0	0	0	7
X	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1	8
X	1	0	0	1	0	0	1	0	1	1	1	1	0	1	1	9
X	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	0	0	0	X	X	X	X	#	*							*
†	†	†	†	†				†	Inverse of Output Combinations Above							Display as above

X = Don't Care † = Above Combinations

* = For liquid crystal readouts, apply a square wave to Ph. For common cathode LED readouts, select Ph = 0. For common anode LED readouts, select Ph = 1. Z

** = Depends upon the BCD Code previously applied when LD = 1.

MOTOROLA

MC14547B

Advance Information

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

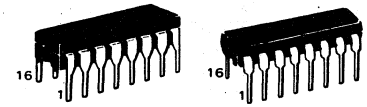
HIGH CURRENT
BCD TO-SEVEN SEGMENT
DECODER/DRIVER

BDC-TO-SEVEN SEGMENT DECODER/DRIVER

The MC14547 BCD-to-seven segment decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of an 8421 BCD-to-seven segment decoder with high output drive capability. Blanking (BI), can be used to turn off or pulse modulate the brightness of the display. The MC14547 can drive seven-segment light-emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- High-Current Sourcing Outputs (Up to 65 mA)
- Low Logic Circuit Power Dissipation
- Supply Voltage Range = +3.0 V to +18 V
- Blanking Input
- Readout Blanking on All Illegal Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Capable of Driving Two Low-Power TTL Loads,
  One Low-Power Schottky TTL Load or
  Two HTL Loads over the Rated Temperature Range.

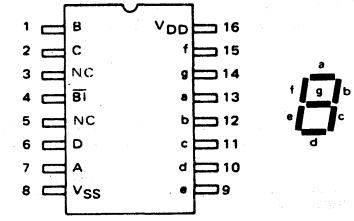


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



MAXIMUM RATINGS (Voltage referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+18 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
Operating Temperature Range MC14547BAL MC14547BCL/CP	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Maximum Continuous Output Drive Current (Source) per Output	I_{OHmax}	65	mA
Maximum Continuous Power Dissipation	P_{OHmax}	1200*	mW

*See power derating curve (Figure 1).

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occure if V_{in} and V_{out} is not constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

INPUTS					OUTPUTS							
$\overline{BI}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	1	1	1	1	1	1	0	0	1	3
1	0	1	0	0	0	1	1	0	0	1	1	4
1	0	1	0	1	1	0	1	1	0	1	1	5
1	0	1	1	0	0	0	1	1	1	1	1	6
1	0	1	1	1	1	1	1	0	0	0	0	7
1	1	0	0	0	1	1	1	1	1	1	1	8
1	1	0	0	1	1	1	1	0	0	1	1	9
1	1	0	1	0	0	0	0	0	0	0	0	Blank
1	1	0	1	1	0	0	0	0	0	0	0	Blank
1	1	1	0	0	0	0	0	0	0	0	0	Blank
1	1	1	0	1	0	0	0	0	0	0	0	Blank
1	1	1	1	0	0	0	0	0	0	0	0	Blank
1	1	1	1	1	0	0	0	0	0	0	0	Blank

X = Don't care

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Drive Voltage (I_{OH} = −65 mA)	V_{OH}	5.0	–	–	–	3.7	–	–	–	Vdc
		10	–	–	–	8.7	–	–	–	
		15	–	–	–	13.7	–	–	–	
Output Drive Current (AL Device)	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	–	–	375	μAdc
(Per Package)		10	–	100	–	0.020	–	–	750	
		15	–	200	–	0.030	–	–	1500	

*T_{low} = −55°C for AL Device, −40° for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device

#Noise immunity specified for worst-case input combination
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	All Types Typ	All Types Max	Unit
Output Rise Time	t_{TLH}					ns
		5.0	–	40	80	
		10	–	30	60	
		15	–	25	50	
Output Fall Time	t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 50 ns		5.0	–	125	250	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 37.5 ns		10	–	75	150	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 37.5 ns		15	–	65	130	
Data Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.40 ns/pF) C_L + 620 ns		5.0	–	640	1280	
t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns		10	–	250	500	
t_{PLH} = (0.20 ns/pF) C_L + 165 ns		15	–	175	350	
t_{PHL} = (1.3 ns/pF) C_L + 655 ns	t_{PHL}	5.0	–	720	1440	ns
t_{PHL} = (0.60 ns/pF) C_L + 260 ns		10	–	290	580	
t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns		15	–	200	400	
Blank Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.30 ns/pF) C_L + 305 ns		5.0	–	320	640	
t_{PLH} = (0.25 ns/pF) C_L + 117.5 ns		10	–	130	260	
t_{PLH} = (0.15 ns/pF) C_L + 92.5 ns		15	–	100	200	
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns	t_{PHL}	5.0	–	485	970	ns
t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns		10	–	200	400	
t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns		15	–	160	320	

LOGIC DIAGRAM

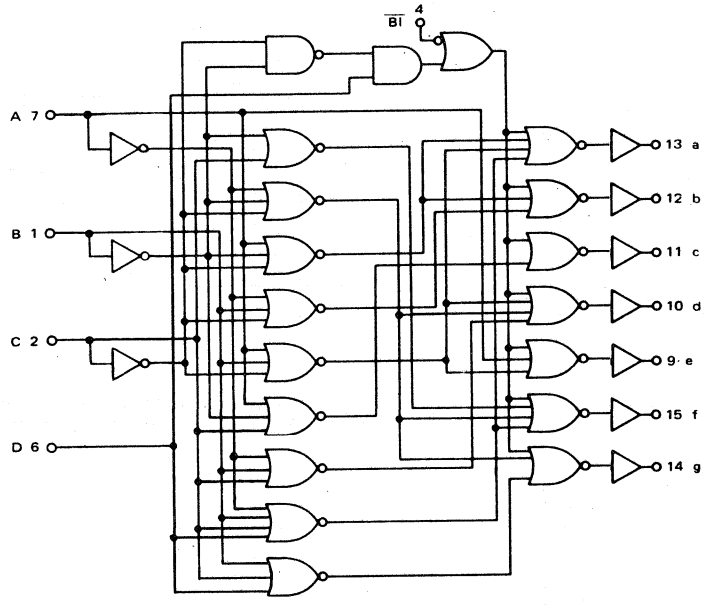
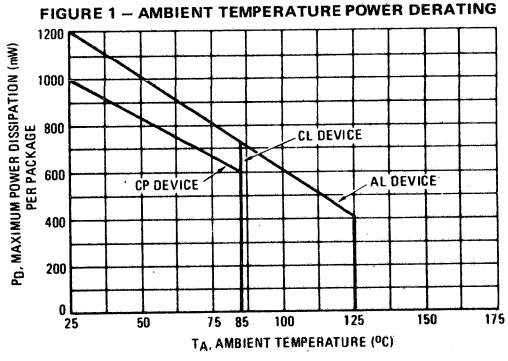
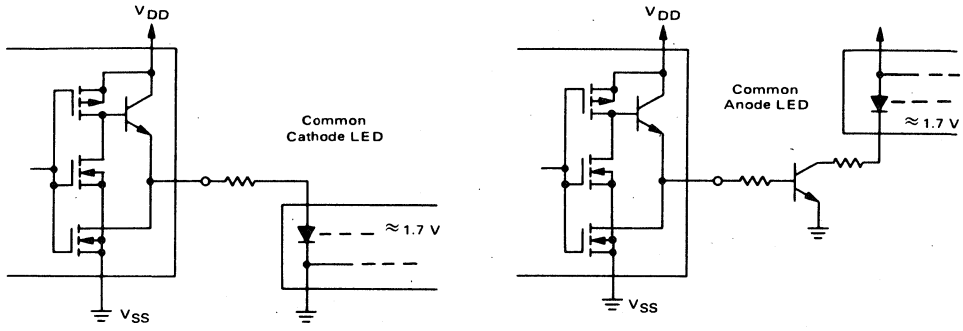


FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING

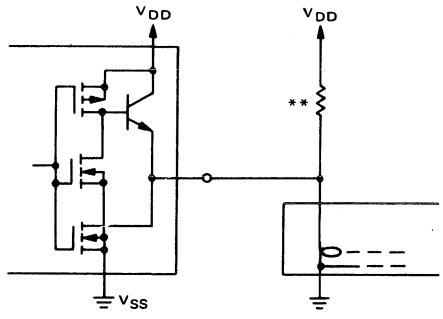


CONNECTIONS TO VARIOUS DISPLAY READOUTS

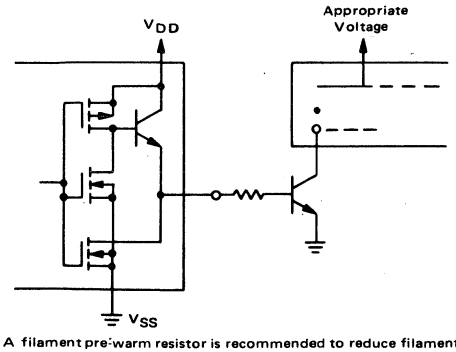
LIGHT EMITTING DIODE (LED) READOUT



INCANDESCENT READOUT

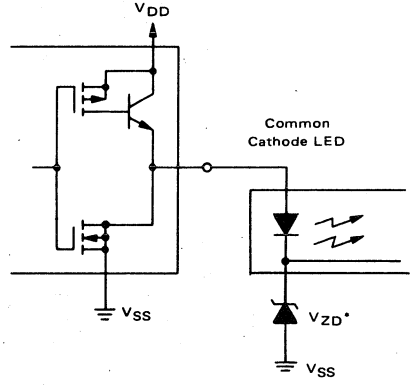


GAS DISCHARGE READOUT



**A filament pre-warm resistor is recommended to reduce filament thermal shcok and increase the effective cold resistance of the filament.

LIGHT-EMITTING DIODE (LED) READOUT USING A ZENER DIODE TO REPLACE DROPPING RESISTORS



*V_{ZD} should be set at $V_{DD} - 1.3\ V - V_{LED}$. Wattage of zener diode must be calculated for number of segments and worst-case conditions.

MOTOROLA

MC14549B
MC14559B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

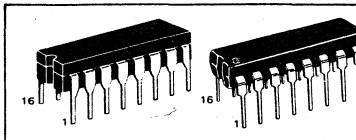
SUCCESSIVE APPROXIMATION REGISTERS

SUCCESSIVE APPROXIMATION REGISTERS

The MC14549B and MC14559B successive approximation registers are 8-bit registers providing all the digital control and storage necessary for successive approximation analog-to-digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the MC14549B is required in the cascaded mode when greater than 8 bits are desired. The Feed Forward (FF) of the MC14559B is used for register shortening where End-of-Conversion (EOC) is required after less than eight cycles.

Applications for the MC14549B and MC14559B include analog-to-digital conversion, with serial and parallel outputs.

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the MC1408 8-Bit D/A Converter
- All Control Inputs Positive-Edge Triggered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



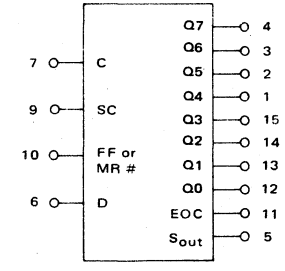
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

#For MC14549B Pin 10 is MR input
For MC14559B Pin 10 is FF input

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLES

MC14549B

SC	$SC_{(t-1)}$	MR	$MR_{(t-1)}$	Clock	Action
X	X	X	X	⌐_	None
X	X	1	X	_⌐	Reset
1	0	0	0	_⌐	Start Conversion
1	X	0	1	_⌐	Start Conversion
1	1	0	0	_⌐	Continue Conversion
0	X	0	X	_⌐	Continue Previous Operation

MC14559B

SC	$SC_{(t-1)}$	EOC	Clock	Action
X	X	X	⌐_	None
1	0	0	_⌐	Start Conversion
X	1	0	_⌐	Continue Conversion
0	0	0	_⌐	Continue Conversion
0	X	1	_⌐	Retain Conversion Result
1	X	1	_⌐	Start Conversion

X = Don't Care
t-1 = State at Previous Clock _⌐

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.28	–	1.02	1.76	–	0.72	–	mAdc
(V_{OL} = 0.5 Vdc) Q Outputs		10	3.2	–	2.6	4.5	–	1.8	–	
(V_{OL} = 1.5 Vdc)		15	8.4	–	6.8	17.6	–	4.8	–	
(V_{OL} = 0.4 Vdc) Sink		5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc) Pin 5, 11 only		5.0	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		10	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.04	–	0.88	1.76	–	0.72	–	mAdc
(V_{OL} = 0.5 Vdc) Q Outputs		10	2.6	–	2.2	4.5	–	1.8	–	
(V_{OL} = 1.5 Vdc)		15	7.2	–	6.0	17.6	–	4.8	–	
(V_{OL} = 0.4 Vdc) Sink		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc) Pin 5, 11 only		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.8 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.6 μA/kHz) f + I_{DD}							
		15	I_T = (2.4 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L)$ $I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

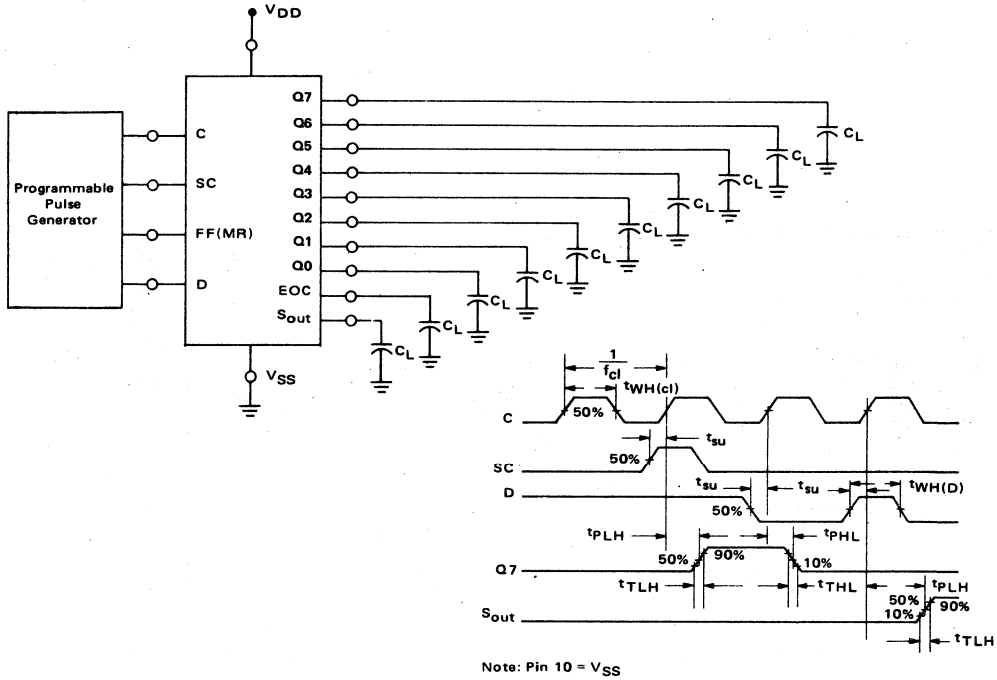
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 177 ns		10	–	210	420	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 130 ns		15	–	155	310	
Clock to S_{out}						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns		5.0	–	750	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 277 ns		10	–	310	620	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 195 ns		15	–	220	440	
Clock to EOC						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/ pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
SC, D, FF or MR Setup Time	t_{su}	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	
Clock Pulse Width	$t_{WH(cl)}$	5.0	700	350	–	ns
		10	270	135	–	
		15	200	100	–	
Pulse Width – D, SC, FF or MR	t_{WH}	5.0	500	250	–	ns
		10	200	100	–	
		15	160	80	–	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5.0	
		15	–	–	4.0	
Clock Pulse Frequency	f_{cl}	5.0	–	1.5	0.8	MHz
		10	–	3.0	1.5	
		15	–	4.0	2.0	

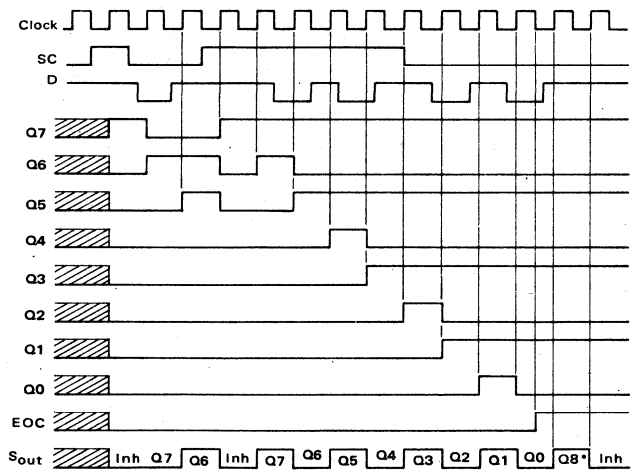
*The formula given is for the typical characteristics only.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



Note: Pin 10 = V_{SS}

TIMING DIAGRAM



— Don't care condition

Inh — Indicates Serial Out is inhibited low.

* — Q8 is ninth-bit of serial information available from 8-bit register.

Note: Pin 10 = V_{SS}

OPERATING CHARACTERISTICS

Both the MC14549B and MC14559B can be operated in either the "free run" or "strobed operation" mode for conversion schemes with any number of bits. Reliable cascading and/or recirculating operation can be achieved if the End of Convert (EOC) output is used as the controlling function, since with EOC = 0 (and with SC = 1 for MC14549B but either 1 or 0 for MC14559B) no stable state exists under continual clocked operation. The MC14559B will automatically recirculate after EOC = 1 during externally strobed operation, provided SC = 1.

All data and control inputs for these devices are triggered into the circuit on the positive edge of the clock pulse.

Operation of the various terminals is as follows:

C = Clock – A positive-going transition of the Clock is required for data on any input to be strobed into the circuit.

SC = Start Convert – A conversion sequence is initiated on the positive-going transition of the SC input on succeeding clock cycles.

D = Data In – Data on this input (usually from a comparator in A/D applications) is also entered into the circuit on a positive-going transition of the clock. This input is Schmitt triggered and synchronized to allow fast response and guaranteed quality of serial and parallel data.

MR = Master Reset (MC14549B only) – Resets all output to 0 on positive-going transitions of the clock. If removed while SC = 0, the circuit will remain reset until SC = 1. This allows easy cascading of circuits.

FF = Feed Forward (MC14559B only) – Provides register shortening by removing unwanted bits from a system.

For operation with less than 8 bits, tie the output *following* the least significant bit of the circuit to EOC. E.g., for a 6-bit conversion, tie Q1 to FF; the part will respond as shown in the timing diagram less two bit times. Not that Q1 and Q0 will still operate and must be disregarded.

For 8-bit operation, FF is tied to V_{SS}.

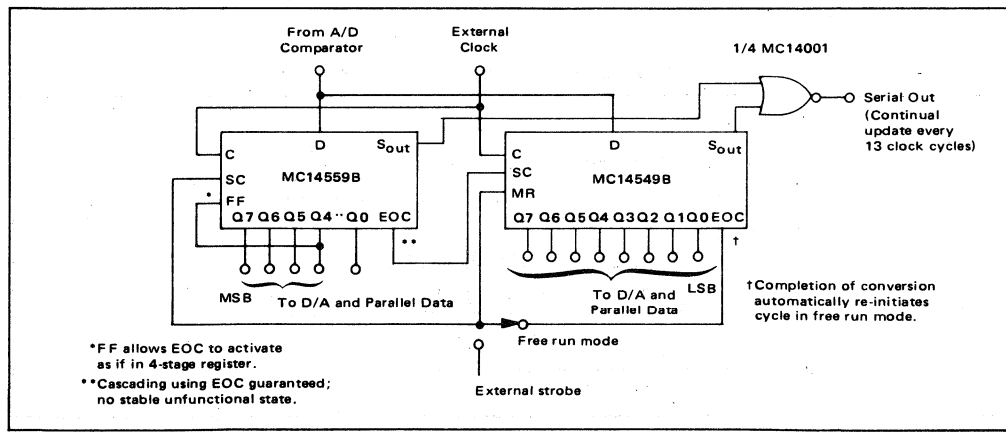
For applications with more than 8 but less than 16 bits, use the basic connections shown in Figure 1. The FF input of the MC14559B is used to shorten the setup. Tying FF directly to the least significant bit used in the MC14559B allows EOC to provide the cascading signal, and results in smooth transition of serial information from the MC14559B to the MC14549B. The Serial Out (S_{out}) inhibit structure of the MC14559B remains inactive one cycle after EOC goes high, while S_{out} of the MC14549B remains inhibited until the second clock cycle of its operation.

Q_n = Data Outputs – After a conversion is initiated the Q's on succeeding cycles go high and are then conditionally reset dependent upon the state of the D input. Once conditionally reset they remain in the proper state until the circuit is either reset or reinitiated.

EOC = End of Convert – This output goes high on the negative-going transition of the clock following FF = 1 (for the MC14559B) or the conditional reset of Q0. This allows settling of the digital circuitry prior to the End of Conversion indication. Therefore either level or edge triggering can indicate complete conversion.

S_{out} = Serial Out – Transmits conversion in serial fashion. Serial data occurs during the clock period when the corresponding parallel data bit is conditionally reset. Serial Out is inhibited on the initial period of a cycle, when the circuit is reset, and on the second cycle after EOC goes high. This provides efficient operation when cascaded.

FIGURE 1 – 12-BIT CONVERSION SCHEME



TYPICAL APPLICATIONS

Externally Controlled 6-Bit ADC (Figure 2)

Several features are shown in this application:

- Shortening of the register to six bits by feeding the seventh output bit into the FF input.
- Continuous conversion, if a continuous signal is applied to SC.
- Externally controlled updating (the start pulse must be shorter than the conversion cycle).
- The EOC output indicating that the parallel data are valid and that the serial output is complete.

Continuously Cycling 8-Bit ADC (Figure 3)

This ADC is running continuously because the EOC signal is fed back to the SC input, immediately initiating a new cycle on the next clock pulse.

Continuously Cycling 12-Bit ADC (Figure 4)

Because each successive approxiamtion register (SAR) has a capability of handling only an eight-bit word, two must be cascaded to make an ADC with more than eight bits.

When it is necessary to cascade two SAR's, the second SAR must have a stable resettable state to remain in while awaiting a subsequent start signal. However, the first stage must not have a stable resettable state while recycling, because during switch-on or due to outside influences, the first stage has entered a reset state, the entire ADC will remain in a stable non-functional condition.

This 12-bit ADC is continuously recycling. The serial as well as the parallel outputs are updated every thirteenth clock pulse. The EOC pulse indicates the completion of

FIGURE 2 – EXTERNALLY CONTROLLED 6-BIT ADC

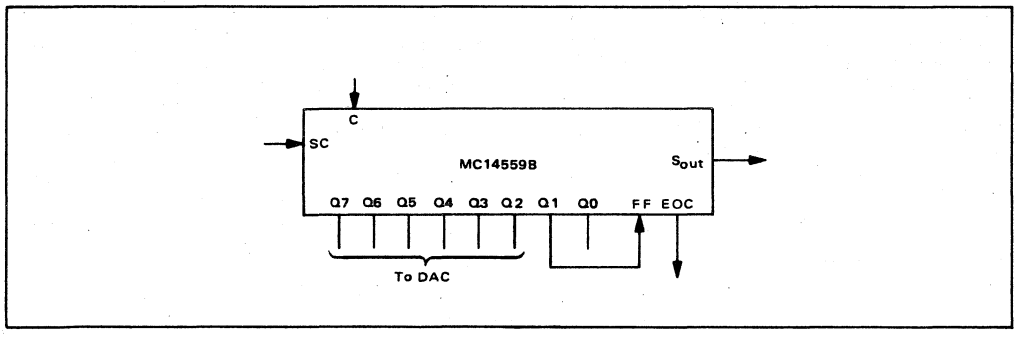


FIGURE 3 – CONTINUOUSLY CYCLING 8-BIT ADC

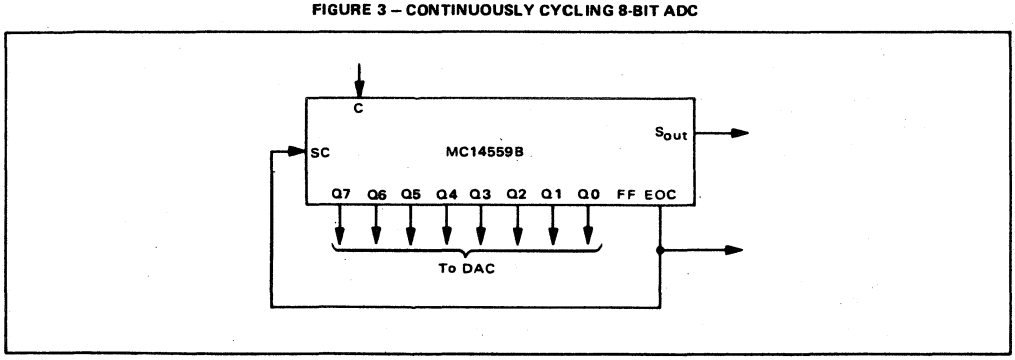
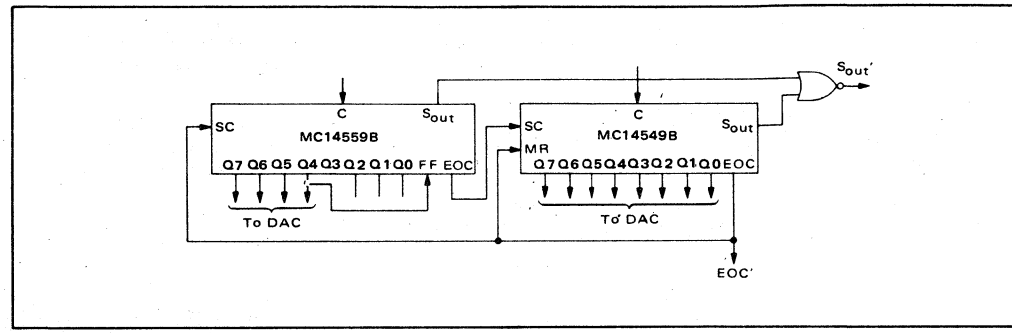


FIGURE 4 – CONTINUOUSLY CYCLING 12-BIT ADC



the 12-bit conversion cycle, the end of the serial output word, and the validity of the parallel data output.

Externally Controlled 12-Bit ADC (Figure 5)

In this circuit the external pulse starts the first SAR and simultaneously resets the cascaded second SAR. When Q4 of the first SAR goes high, the second SAR starts conversion, and the first one stops conversion. EOC indicates that the parallel data are valid and that the serial output is complete. Updating the output data is started with every external control pulse.

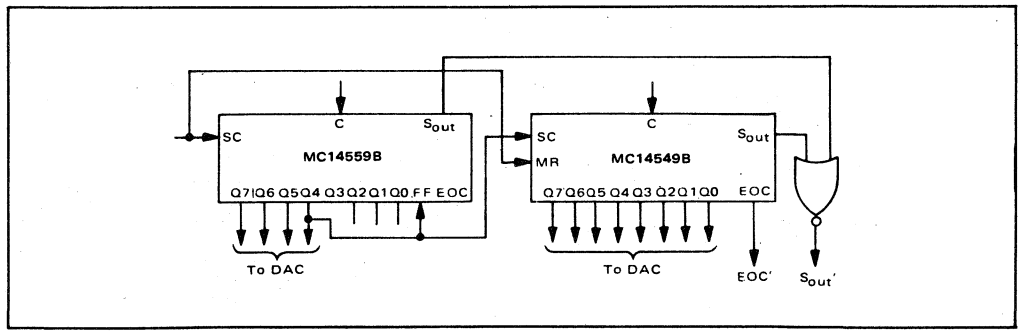
Additional Motorola Parts for Successive Approximation ADC

Monolithic digital-to-analog converters – The MC1408/1508 converter has eight-bit resolution and is available with 6, 7, and 8-bit accuracy. **The amplifier-comparator block** – The MC1407/1507 contains a high speed operational amplifier and a high speed comparator with adjustable window.

With these two linear parts it is possible to construct SA-ADCs with an accuracy of up to eight bits, using as the register one MC14549B or one MC14559B. An additional CMOS block will be necessary to generate the clock frequency.

Additional information on successive approximation ADC is found in Motorola Application Note AN-716.

FIGURE 5 – EXTERNALLY CONTROLLED 12-BIT ADC



MOTOROLA

MC14551B

Advance Information

QUAD 2-INPUT ANALOG MULTIPLEXER/DEMULTIPLEXER

The MC14551B is a digitally controlled analog switch. It is an effective 4 PDT switch with low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- High On/Off Output Voltage Ratio – 65 dB typical
- Quiescent Current = 5.0 nA/Package typical @ 5 Vdc
- Low Crosstalk Between Switches – 80 dB typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up To 65 MHz
- Linearized Transfer Characteristics, $\Delta R_{ON} < 60\ \Omega$ for V_{in} @ V_{DD} to V_{EE} @ 15 Vdc
- Low Noise – 12 $nV/\sqrt{Cycle}$, $f \geq 1$ kHz typical

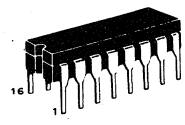
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage $V_{DD} - V_{EE}$	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
Through Current	I	25	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

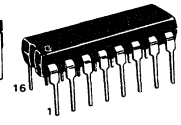
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT ANALOG MULTIPLEXER/ DEMULTIPLEXER



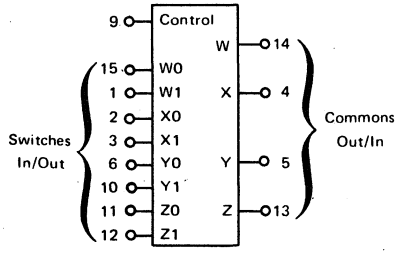
CASE 620
L SUFFIX
CERAMIC PACKAGE



CASE 648
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



Control	ON
0	W0 X0 Y0 Z0
1	W1 X1 Y1 Z1

V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

Note: Control Input referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be $\leq V_{SS}$.

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS ($V_{DD} = V_{SS}$)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Input Current (Control)	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance	C_{in}									pF
(V_{in} = 0)										
Control, Inhibit		–	–	–	–	5.0	–	–	–	
Switch Inputs		–	–	–	–	10	–	–	–	
Output Capacitance	C_{out}	10	–	–	–	17	–	–	–	pF
Feedthrough Capacitance	C_{in-out}	10	–	–	–	0.10	–	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**†	I_T	5.0	$I_T = (0.07\ \mu A/kHz)\ f + I_Q$							μAdc
(Dynamic plus Quiescent,		10	$I_T = (0.20\ \mu A/kHz)\ f + I_Q$							
Per Package)		15	$I_T = (0.36\ \mu A/kHz)\ f + I_Q$							
ON Resistance (AL Device)	R_{ON}	5.0	–	880	–	250	1050	–	1200	Ω
		10	–	400	–	120	500	–	550	
		15	–	220	–	80	280	–	320	
ON Resistance (CL/CP Device)	R_{ON}	5.0	–	880	–	250	1050	–	1200	Ω
		10	–	450	–	120	500	–	520	
		15	–	250	–	80	280	–	300	
Δ ON Resistance Between Any	ΔR_{ON}	5.0	–	–	–	25	–	–	–	Ω
Two Channels		10	–	–	–	10	–	–	–	
		15	–	–	–	5.0	–	–	–	
OFF Channel Leakage Current	–									nAdc
Any Channel		25	–	100	–	±0.01	100	–	–	
(AL Device) All Channels OFF:		15	–	100	–	±0.02	100	–	–	
OFF Channel Leakage Current	–									nAdc
Any Channel		15	–	1000	–	±0.01	1000	–	–	
(CL/CP Device)										
All Channels OFF:		15	–	1000	–	±0.02	1000	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity is defined as the control input voltage coincident with the specified change, ΔV_{out}, at an output in the OFF state.
**The formulas given are for the typical characteristics only at 25°C.
†Total Supply Current, I_T, is the current drawn at device terminals V_{DD} and V_{SS} for total current through the device. The channel component, $(V_{in}-V_{out})/R_{ON}$, should not be included.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}–V_{SS} Vdc	Min	Typ	Max	Unit
Propagation Delay Times Switch Input to Switch Output (R_L = 10kΩ)	t_{PLH},t_{PHL}					ns
t_{PLH},t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns		5.0	–	35	90	
t_{PLH},t_{PHL} = (0.08 ns/pF) C_L + 11 ns		10	–	15	40	
t_{PLH},t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns		15	–	12	30	
Inhibit to Output (R_L = 10 kΩ): Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level	t_{PHZ},t_{PLZ} t_{PZH},t_{PZL}					ns
		5.0	–	360	900	
		10	–	160	375	
		15	–	120	300	
Control Input to Output (R_L = 10 kΩ)	t_{PLH},t_{PHL}					ns
		5.0	–	350	875	
		10	–	140	350	
		15	–	100	250	
Sine Wave Distortion (R_L = 1 kΩ, f = 1 kHz)	–	10	–	0.04	–	%
Bandwidth (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD} – V_{SS}) p-p, $20 \log_{10} \frac{V_{out}}{V_{in}}$ = –3 dB)	BW	10	–	55	–	MHz
Feedthrough Attenuation, Input to Output (R_L = 1 kΩ, $20 \log_{10} \frac{V_{out}}{V_{in}}$ = –50 dB)	–	10	–	3.0	–	MHz
Channel Separation (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD} – V_{SS}) p-p, $20 \log_{10} \frac{V_{out(B)}}{V_{in(A)}}$ = –50 dB)	–	10	–	3.0	–	MHz
Feedthrough Control, Input to Output (R1 = 1 kΩ, R_L = 10 kΩ, Control/Inhibit t_r = t_f = 20 ns	–	10	–	30	–	mV
Maximum Control Frequency (R_L = 1 kΩ, V_{out} = 1/2 V_{in})	–	10	–	10	–	MHz

*The formulas given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC

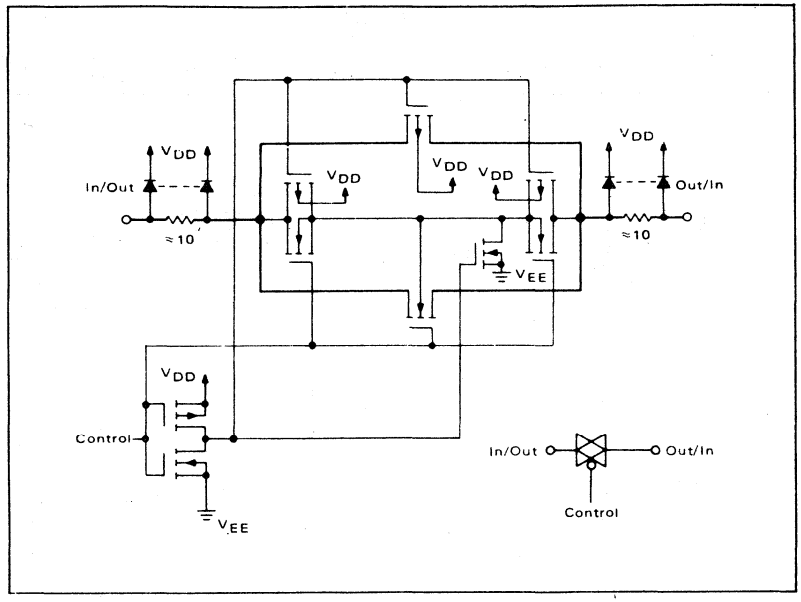
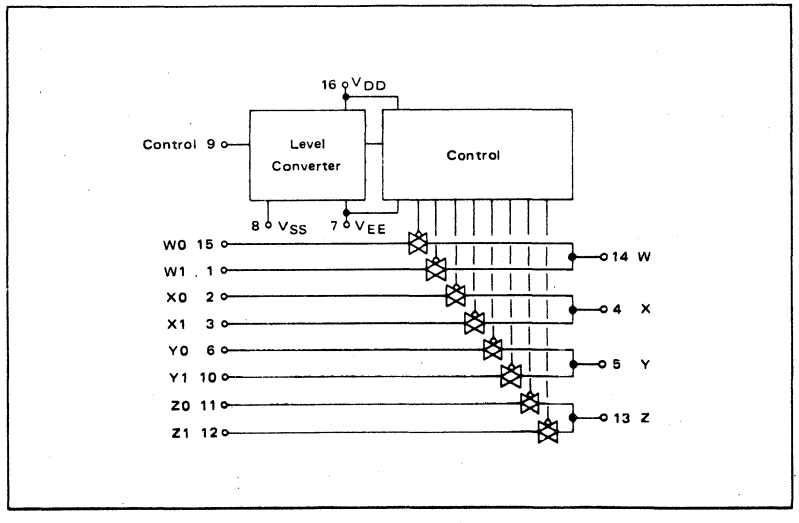


FIGURE 2 – MC14551B FUNCTIONAL DIAGRAM



TEST CIRCUITS

FIGURE 3 – INPUT VOLTAGE

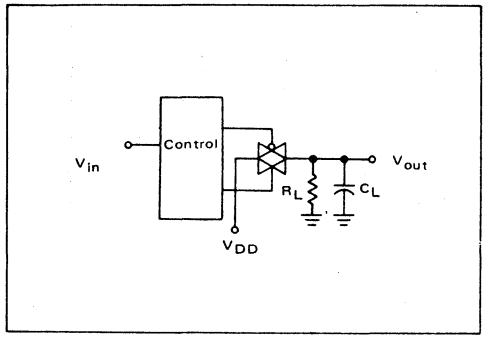


FIGURE 4 – PROPAGATION DELAY TIMES, CONTROL AND INHIBIT TO OUTPUT

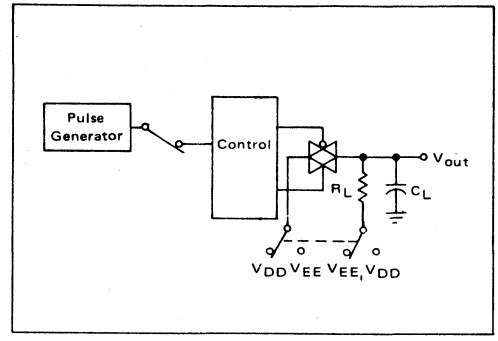


FIGURE 5 – BANDWIDTH AND FEEDTHROUGH ATTENUATION

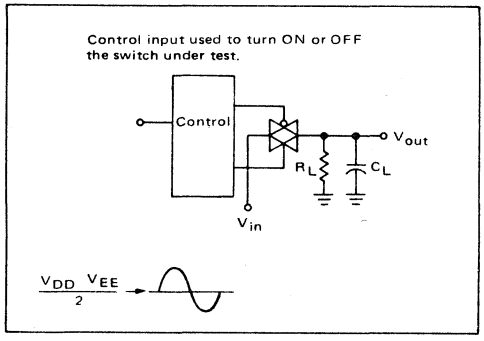


FIGURE 6 – CROSSTALK BETWEEN ANY TWO SWITCHES

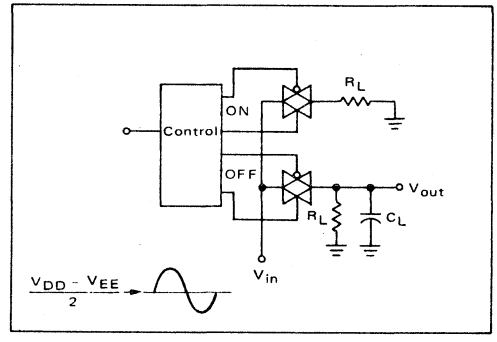


FIGURE 7 – FEEDTHROUGH, CONTROL TO SIGNAL OUTPUT

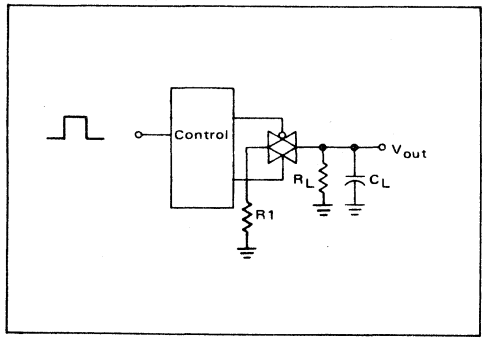


FIGURE 8 – MAXIMUM CONTROL FREQUENCY

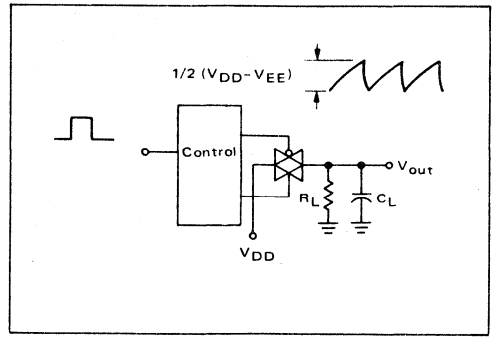
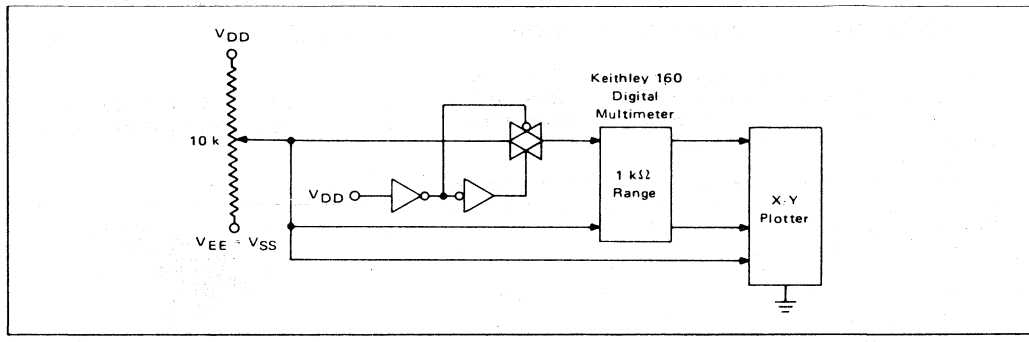


FIGURE 9 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 10 – V_{DD} @ 7.5 V, V_{EE} @ –7.5V

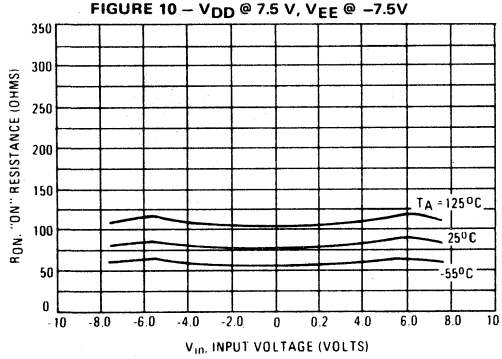


FIGURE 11 – V_{DD} @ 5.0V, V_{EE} @ –5.0 V

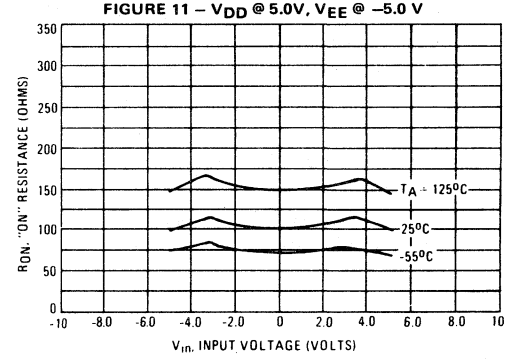


FIGURE 12 – V_{DD} @ 2.5 V, V_{EE} @ –2.5 V

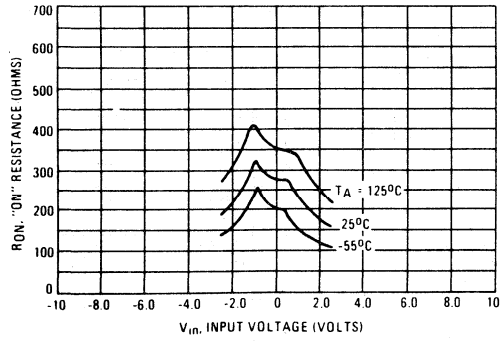
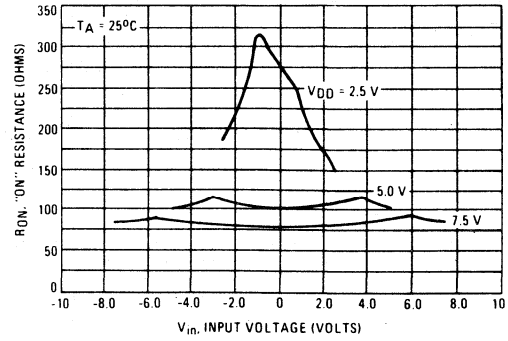


FIGURE 13 – COMPARISON at 25°C, V_{DD} @ $-V_{EE}$



MOTOROLA

MCM14552

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (64 x 4) STATIC RANDOM ACCESS MEMORY

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14552 is a static random access memory (RAM) organized in a 64 x 4 bit pattern. The three chip enable inputs can be used as extensions of the six address inputs, creating 9-bit address scheme. Eight MCM14552 devices may be used to comprise a 2048-bit memory (512 x 4) without additional address decoding.

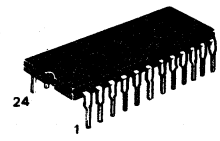
The mode control (M) is used to change the control logic characteristic of the circuit. For example, with M high, the 3-state input (T) fully controls the 3-state characteristic of the output. With M low, the output 3-state characteristic is controlled by chip enable inputs (CE), write enable input (WE) and T.

The memory is designed so that dc signals may operate the memory, with no maximum pulse width restrictions.

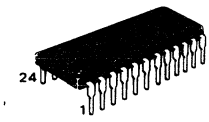
Medium speed, micropower operation, and control flexibility make the device useful in scratch pad or buffer applications where battery operation or high noise immunity are required.

- Quiescent Current = 50 μA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- 3-state Output Capability for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

NOTE: Pin 20(LE)) must be connected to V_{SS}



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MCM14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

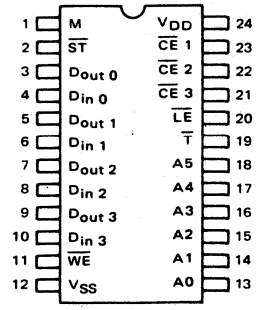
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}.

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±1.0	–	±0.00001	±1.0	–	±14.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.050	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.100	10	–	300	
		15	–	20	–	0.150	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.050	50	–	375	µAdc
(Per Package)		10	–	100	–	0.100	100	–	750	
		15	–	200	–	0.150	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.98 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.96 µA/kHz) f + I_{DD}							
		15	I_T = (5.86 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	1	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns			5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 25 ns			10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns			15	–	65	130	
Output Fall Time	1	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns			5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns			10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns			15	–	40	80	
Read Cycle Time	1, 2	$t_{cyc(R)}$	5.0	–	2000	6000	ns
			10	–	750	2200	
			15	–	500	1650	
Write Cycle Time	3, 4	$t_{cyc(W)}$	5.0	–	1200	3600	ns
			10	–	750	2200	
			15	–	500	1650	
Address to $\overline{\text{Strobe}}$ Setup Time	1, 3	$t_{su(A\text{-}\overline{ST})}$	5.0	1500	500	–	ns
			10	450	150	–	
			15	350	120	–	
$\overline{\text{Strobe}}$ to Address Hold Time	1, 3	$t_{h(\overline{ST}\text{-}A)}$	5.0	150	50	–	ns
			10	100	0	–	
			15	75	0	–	
Address to $\overline{\text{Chip Enable}}$ Serup Time	2, 4	$t_{su(A\text{-}\overline{CE})}$	5.0	1800	600	–	ns
			10	600	200	–	
			15	450	150	–	
$\overline{\text{Chip Enable}}$ to Address Hold Time	2, 4	$t_{h(\overline{CE}\text{-}A)}$	5.0	450	150	–	ns
			10	300	100	–	
			15	225	75	–	
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Reading	1, 2	$t_{WL(R)}$	5.0	1800	450	–	ns
			10	450	150	–	
			15	350	100	–	
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Writing	3, 4	$t_{WL(W)}$	5.0	3600	1200	–	ns
			10	1800	600	–	
			15	1350	400	–	
Read Setup Time	1	$t_{su(R)}$	5.0	0	-100	–	ns
			10	0	-40	–	
			15	0	-30	–	
Read Hold Time	1	$t_{h(R)}$	5.0	540	180	–	ns
			10	240	60	–	
			15	180	45	–	
Data Setup Time	3, 4	$t_{su(D)}$	5.0	1800	600	–	ns
			10	600	200	–	
			15	450	150	–	
Data Hold Time	3, 4	$t_{h(D)}$	5.0	600	200	–	ns
			10	150	50	–	
			15	120	30	–	

*The formula given is for the typical characteristics only.

(continued)

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C) (continued)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Write Enable Setup Time	3, 4	$t_{su}(\overline{WE})$	5.0	720	240	–	ns
			10	240	80	–	
			15	180	55	–	
Write Enable Hold Time	3, 4	$t_h(WE)$	5.0	150	50	–	ns
			10	60	20	–	
			15	45	15	–	
Read Access Time from Strobe	1, 3	$t_{acc}(R\text{-}\overline{ST})$	5.0	–	2000	6000	ns
			10	–	700	2100	
			15	–	350	1600	
Read Access Time from Chip Enable	2	$t_{acc}(R\text{-}\overline{CE})$	5.0	–	2100	6300	ns
			10	–	750	2250	
			15	–	400	1700	
Output Enable/Disable Delay from Chip Enable or Write Enable	2, 4	$t_R(\overline{CE})$, $t_R(\overline{WE})$	5.0	–	400	1200	ns
			10	–	200	600	
			15	–	150	450	
Three-State Enable/Disable Output Delay	2	$t(\overline{T})$	5.0	–	400	1200	ns
			10	–	160	480	
			15	–	120	360	
Latch to Output Propagation Delay	1	$t_{\overline{LE}}$	5.0	–	500	1500	ns
			10	–	200	600	
			15	–	150	450	

*The formula given is for the typical characteristics only.

LOGIC DIAGRAM

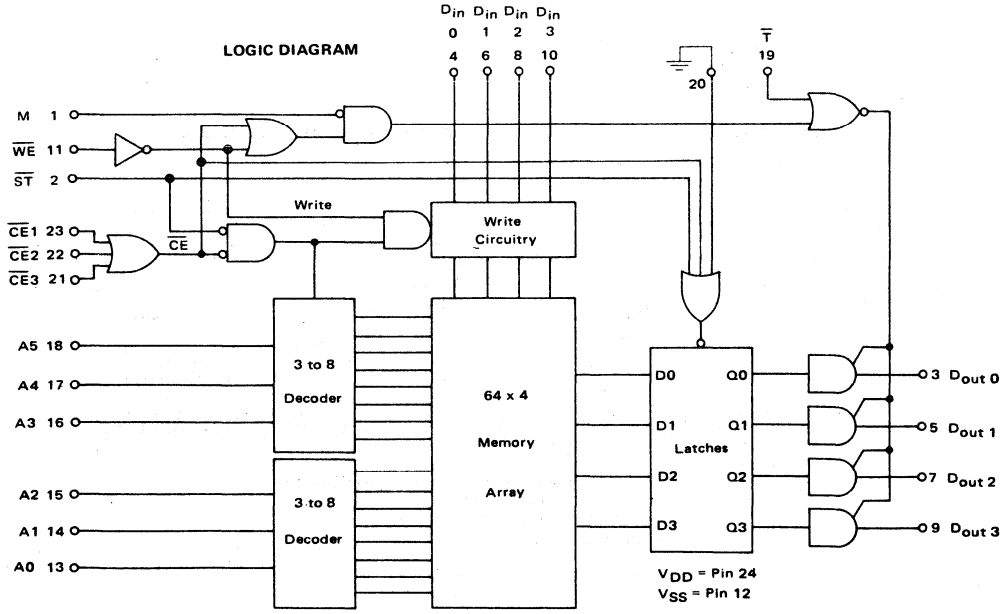
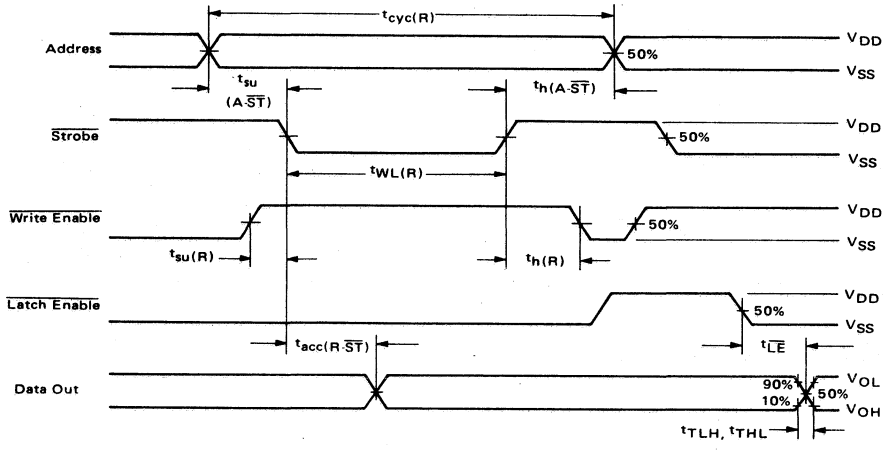
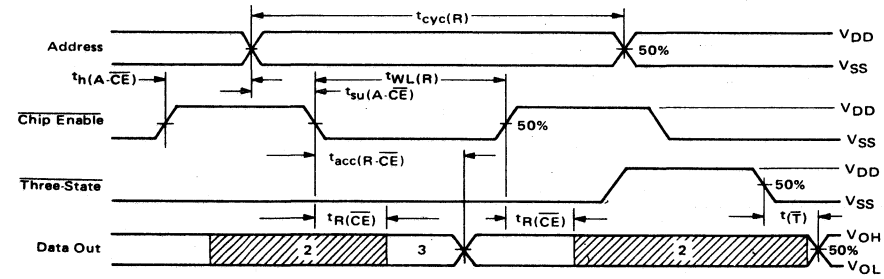


FIGURE 1 – READ CYCLE WAVEFORMS UTILIZING STROBE TO ACCESS MEMORY



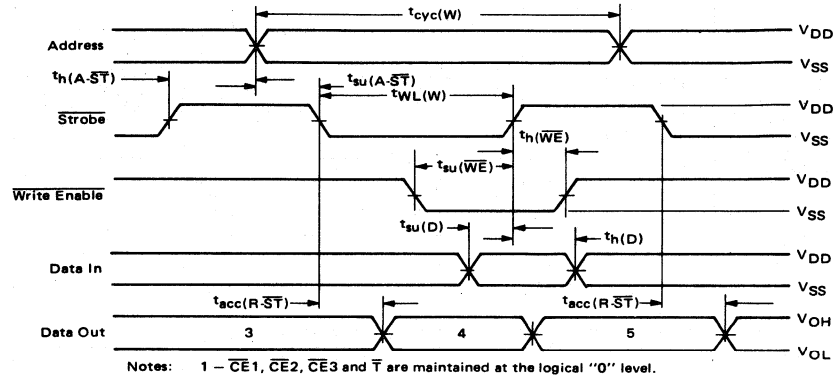
Notes: 1 – $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are low, M is high.
2 – $\overline{WE}$ may be held high during the complete read cycle.

FIGURE 2 – READ CYCLE WAVEFORMS UTILIZING CHIP ENABLE TO ACCESS MEMORY



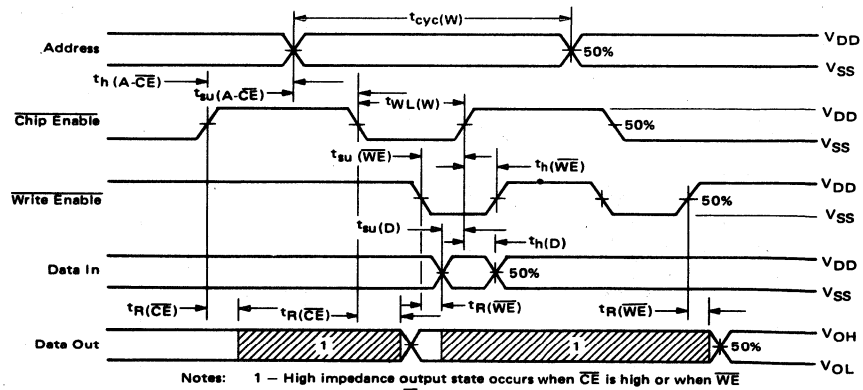
Notes: 1 – Unused $\overline{CE}$, $\overline{ST}$, M and $\overline{T}$ are low and $\overline{WE}$ is high.
2 – High impedance output state occurs when any $\overline{CE}$ is high and M is low, or when $\overline{T}$ is high.
3 – The output displays data from the previous state.
4 – $t_{WL(R)} \geq t_{acc(R\cdot\overline{CE})max}$.

FIGURE 3 – WRITE CYCLE WAVEFORMS UTILIZING STROBE



Notes:
1 – $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are maintained at the logical "0" level.
2 – M is maintained at the logical "1" level.
3 – The output displays the contents of the previous state.
4 – The output displays the contents of the presently addressed location as in a read modify write cycle.
5 – The output displays the data that was written into addressed location.

FIGURE 4 – WRITE CYCLE WAVEFORM UTILIZING CHIP ENABLE



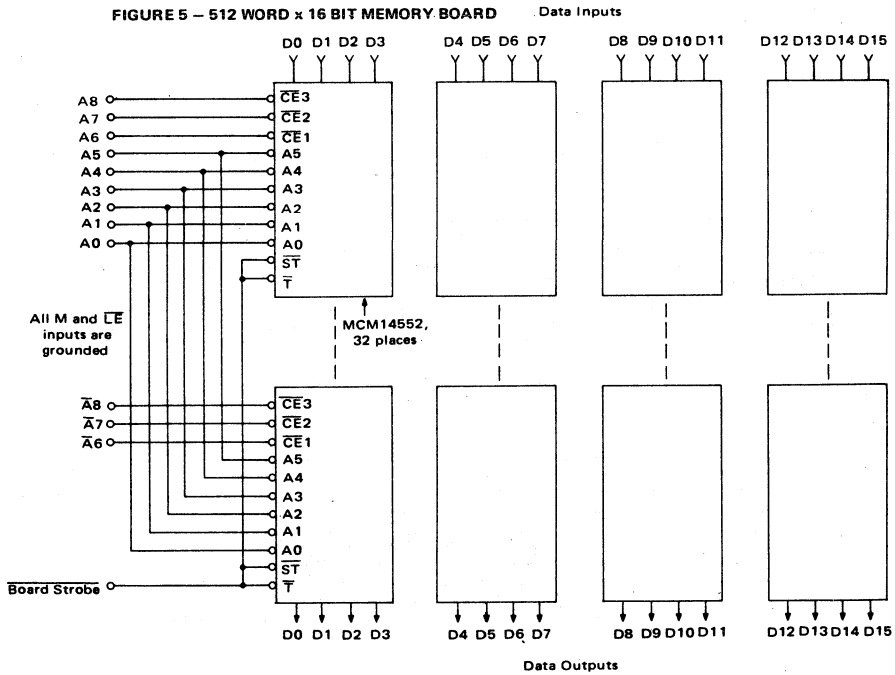
Notes:
1 – High impedance output state occurs when $\overline{CE}$ is high or when $\overline{WE}$ is low, for M and $\overline{T}$ maintained in the low state.
2 – Unused $\overline{CE}$'s, $\overline{ST}$, M and $\overline{T}$ are maintained at the logical "0" level.

TRUTH TABLE

Function	$\overline{CE}$ 1	$\overline{CE}$ 2	$\overline{CE}$ 3	$\overline{T}$	$\overline{LE}$	M	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	Comments
Address Changing Valid	X	X	X	X	X	X	1	X	X	R/A	D_{out} will be active if all $\overline{CE}$ = 0, $\overline{T}$ = 0 and $\overline{WE}$ = 1 or if M = 1 and $\overline{T}$ = 0
	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
Address Changing Not Valid	0	0	0	X	X	X	0	X	X	R/A	D_{out} will be active if $\overline{T}$ = 0 and $\overline{WE}$ = 1 or if M = 1 and $\overline{T}$ = 0
D_{out} Disabled (in high resistance state)	X	X	1	X	X	0	X	X	X	R	Disables write circuitry
	X	1	X	X	X	0	X	X	X	R	
	1	X	X	X	X	0	X	X	X	R	
	X	X	X	1	X	X	X	X	X	R	$\overline{T}$ = 1 always disables D_{out}
	X	X	X	X	X	0	X	0	X	R	M = 0 and write operation disables D_{out}
D_{out} Enabled (in active state)	0	0	0	0	X	X	X	1	X	A	Read operation, D_{out} active
	X	X	X	0	X	1	X	X	X	A	Read or write, D_{out} active
Read Addressed Memory Location Into Output Latch	0	0	0	X	0	X	0	X	X	R/A	If $\overline{WE}$ = 0, D_{in} = D_{out}
Disable Reading From Memory	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	X	X	0	X	R/A	
Write Into Memory	0	0	0	X	X	X	0	0	A	R/A	
Write Disabled	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	X	X	1	X	R/A	
Output Latch Enabled	0	0	0	X	0	X	0	X	X	R/A	
Output Latch Disabled	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	1	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	

R = High resistance state at D_{out}.
A = An active level of either V_{DD} or V_{SS}.
R/A = An R or A condition depending on the don't care condition.
X = Don't care condition (must be in the "1" or "0" state).
1 = A high level at V_{DD}.
0 = A low level at V_{SS}.

FIGURE 5 – 512 WORD x 16 BIT MEMORY BOARD



MOTOROLA

MC14553B

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

THREE-DIGIT BCD COUNTER

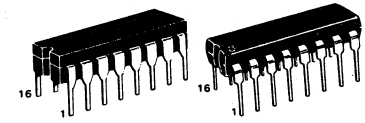
THREE-DIGIT BCD COUNTER

The MC14553B three-digit BCD counter consists of three negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on-chip oscillator provides the low-frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

- TTL Outputs
- On-Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

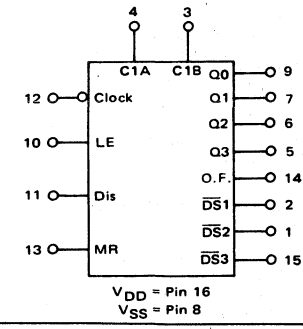
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
DC Current per Pin, All Outputs	I	20	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUTS				
MASTER RESET	CLOCK	DISABLE	LE	OUTPUTS
0	⎍	0	0	No Change
0	⎍	0	0	Advance
0	X	1	X	No Change
0	1	⎍	0	Advance
0	1	⎍	0	No Change
0	0	X	X	No Change
0	X	X	⎍	Latched
0	X	X	1	Latched
1	X	X	0	Q0 = Q1 = Q2 = Q3 = 0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 4.6 Vdc) Source		5.0	-0.25	–	-0.20	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	−0.62	–	−0.50	−0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	−1.8	–	−1.5	−3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink-Pin 3	I_{OL}	5.0	0.23	–	0.2	0.88	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.5	2.25	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.80	–	1.5	8.8	–	1.20	–	
(V_{OL} = 0.4 Vdc) Sink-Other Outputs	I_{OL}	5.0	2.4	–	2.5	4.0	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	3.8	–	5.0	8.0	–	3.5	–	
(V_{OL} = 1.5 Vdc)		15	10	–	15	20	–	10	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 4.6 Vdc) Source		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	−0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	−3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink-Pin 3	I_{OL}	5.0	0.23	–	0.2	0.88	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.5	2.25	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.80	–	1.5	8.8	–	1.20	–	
(V_{OL} = 0.4 Vdc) Sink-Other Outputs	I_{OL}	5.0	2.4	–	2.0	4.0	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	3.8	–	3.0	8.0	–	2.5	–	
(V_{OL} = 1.5 Vdc)		15	10	–	8.4	20	–	7.0	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	μAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.35 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.85 μA/kHz) f + I_{DD}							
		15	I_T = (1.50 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	3a	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns			5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns			10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns			15	–	65	130	
Output Fall Time	3a	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns			5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns			10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns			15	–	40	80	
Clock to BCD Out	3a	t_{PLH}, t_{PHL}	5.0	–	900	1800	ns
			10	–	500	1000	
			15	–	300	600	
Clock to Overflow	3a	t_{PHL}	5.0	–	600	1200	ns
			10	–	400	800	
			15	–	200	400	
Reset to BCD Out	3b	t_{PHL}	5.0	–	900	1800	ns
			10	–	500	1000	
			15	–	300	600	
Clock to Latch Enable Setup Time	3b	t_{su}	5.0	600	300	–	ns
			10	400	200	–	
			15	200	100	–	
Clock Pulse Width	3a	$t_{WH(cl)}$	5.0	550	275	–	ns
			10	200	100	–	
			15	150	75	–	
Reset Pulse Width	3b	$t_{WH(R)}$	5.0	1200	600	–	ns
			10	600	300	–	
			15	450	225	–	
Input Clock Frequency	3a	f_{cl}	5.0	–	1.5	0.9	MHz
			10	–	5.0	2.5	
			15	–	7.0	3.5	
Input Clock Rise Time	3b	t_{TLH}	5.0	No Limit			ns
			10				
			15				
Scan Oscillator Frequency	2	f_{osc}	5.0	–	0.4/C1	–	Hz
			10	–	1.2/C1	–	
(C1 measured in μF)			15	–	1.6/C1	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING

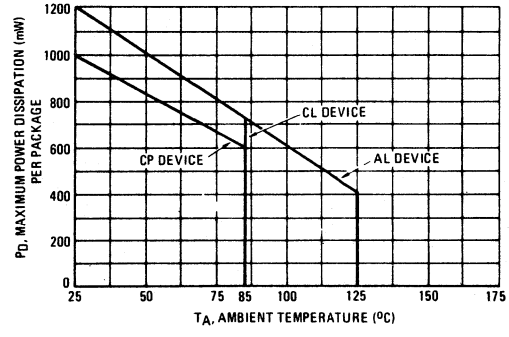


FIGURE 2 – 3-DIGIT COUNTER TIMING DIAGRAM (Reference Figure 4)

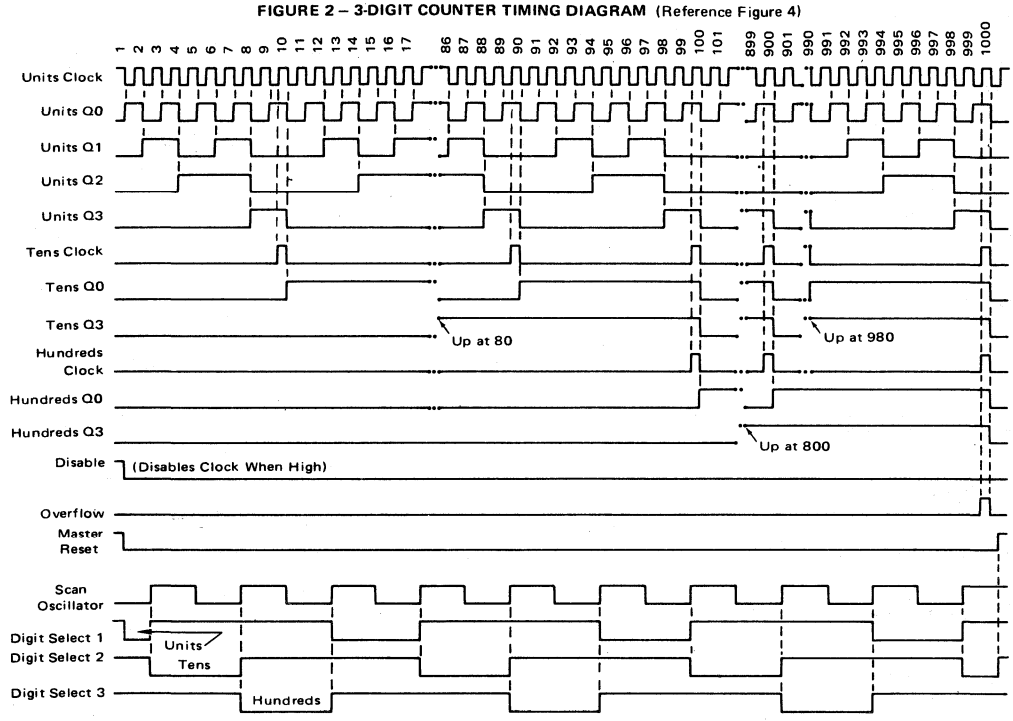
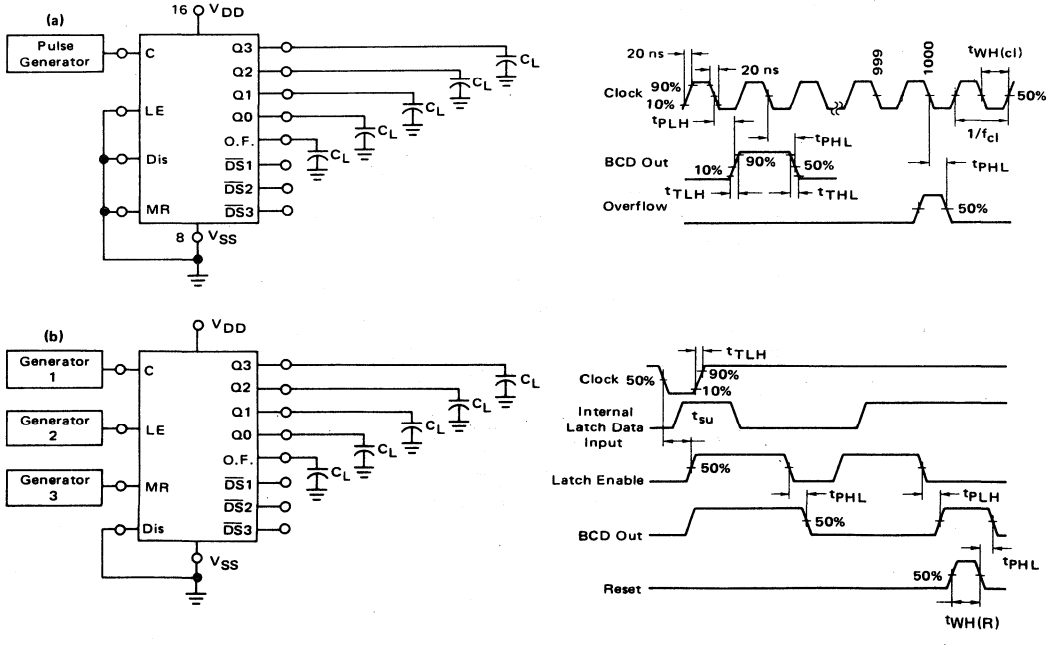


FIGURE 3 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



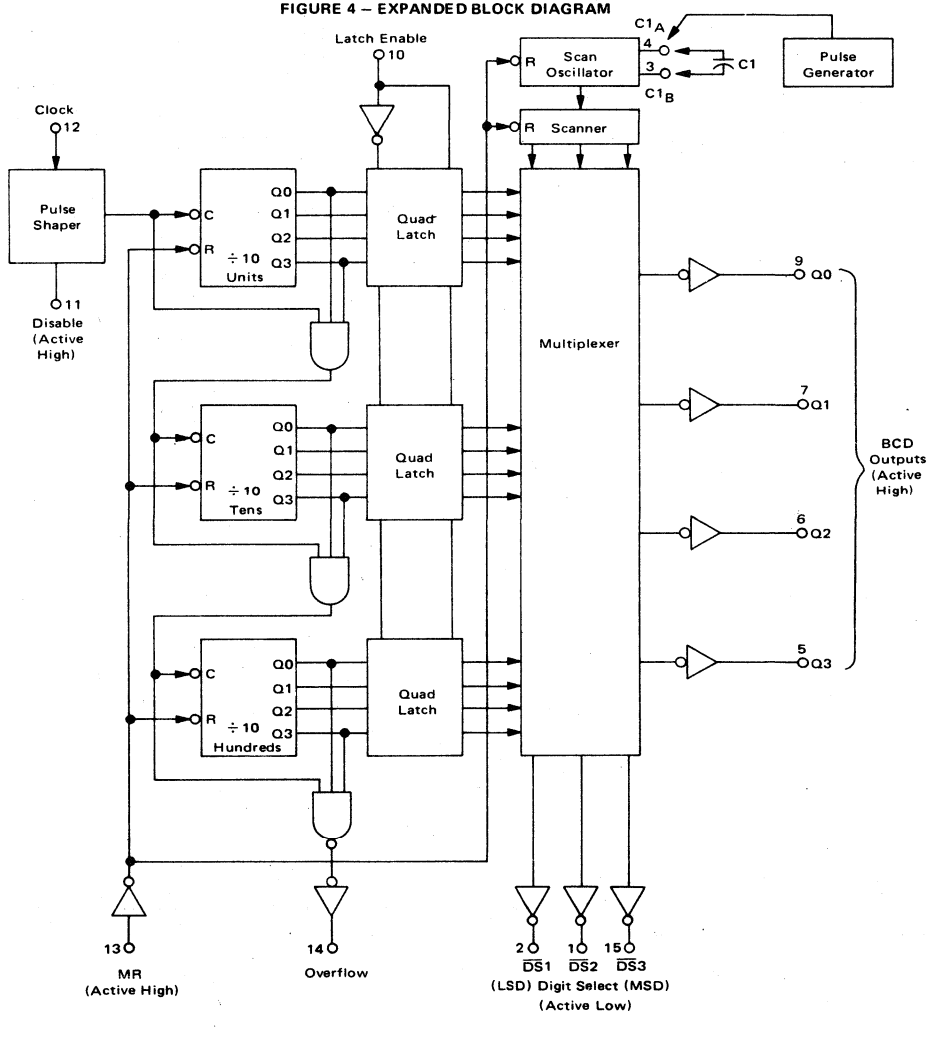
OPERATING CHARACTERISTICS

The MC14553B three-digit counter, shown in Figure 4, consists of three negative edge-triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible.

An on-chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4, or it can be overridden and driven with an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is high the digit scanner is set to digit one; but all three digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.

FIGURE 4 – EXPANDED BLOCK DIAGRAM



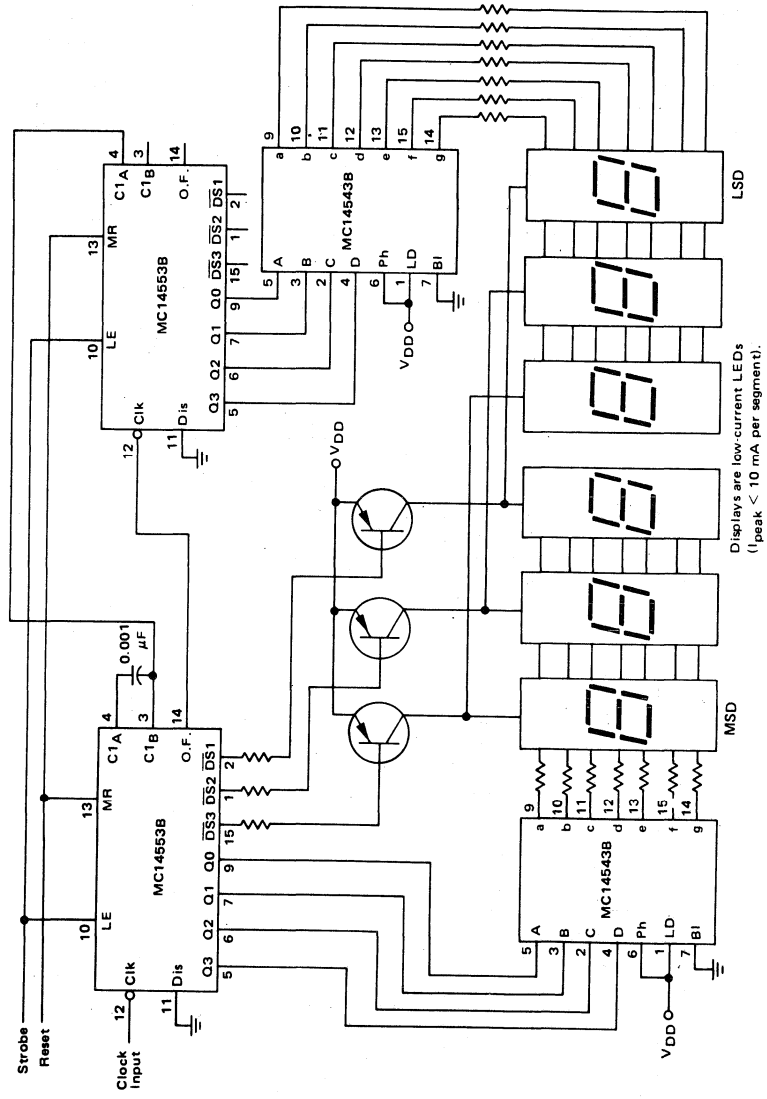


FIGURE 5 – SIX-DIGIT DISPLAY

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14554B

2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER

The MC14554B 2 x 2-bit parallel binary multiplier is constructed with complementary MOS (CMOS) enhancement mode devices. The multiplier can perform the multiplication of two binary numbers and simultaneously add two other binary numbers to the product. The MC14554B has two multiplicand inputs (X0 and X1), two multiplier inputs (Y0 and Y1), five cascading or adding inputs (K0, K1, M0, M1, and M2), and five sum and carry outputs (S0, S1, S2, C1 [S3], and C0). The basic multiplier can be expanded into a straightforward m-bit by n-bit parallel multiplier without additional logic elements.

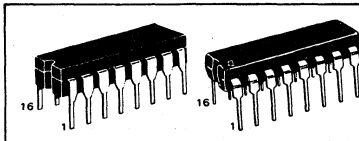
Application areas include arithmetic processing (multiplying/adding, obtaining square roots, polynomial evaluation, obtaining reciprocals, and dividing), Fast Fourier Transform processing, digital filtering, communications (convoluation and correlation), and process and machine controls.

- Diode Protection on All Inputs
- All Outputs Buffered
- Quiescent Current = 5.0 nA typical @ 5 Vdc
- Straight-forward m-Bit By n-Bit Expansion
- No Additional Logic Elements Needed for Expansion
- Multiplies and Adds Simultaneously
- Positive Logic Design
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes:
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

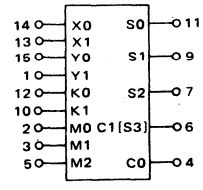
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

EQUATIONS

$S = (X \times Y) + K + M$

Where:
x Means Arithmetic Times.
+ Means Arithmetic Plus.
S = S3 S2 S1 S0, X = X1X0, Y = Y1Y0,
K = K1 K0, M = M1 M0 (Binary Numbers).

Example:

Given: X = 2(10), Y = 3(11)
K = 1(01), M = 2(10)

Then: S = (2 x 3) + 1 + 2 = 9
S = (10 x 11) + 01 + 10 = 1001

Note: C0 connected to M2 for this size multiplier.
See general expansion diagram for other size multipliers.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.0\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (2.0\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.0\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50)\ V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
K0 to C0						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 185 ns		5.0	–	270	675	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 82 ns		10	–	115	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	–	85	215	
M0 to S2						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 595 ns		5.0	–	680	1700	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 247 ns		10	–	280	750	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns		15	–	210	570	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION WAVEFORMS

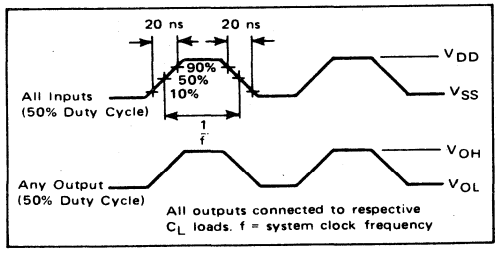
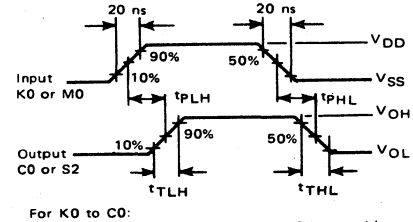
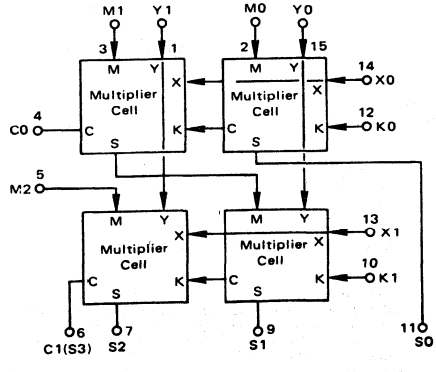


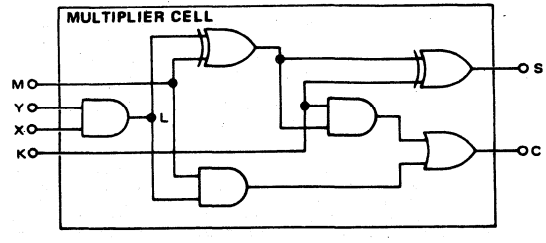
FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



For K0 to C0:
Inputs X0, X1, Y0, Y1, K1, and M2 low, and inputs M0 and M1 high.
For M0 to S2:
Inputs X1, Y1, and K0 low, and inputs X0, Y0, K1, M1, and M2 high.

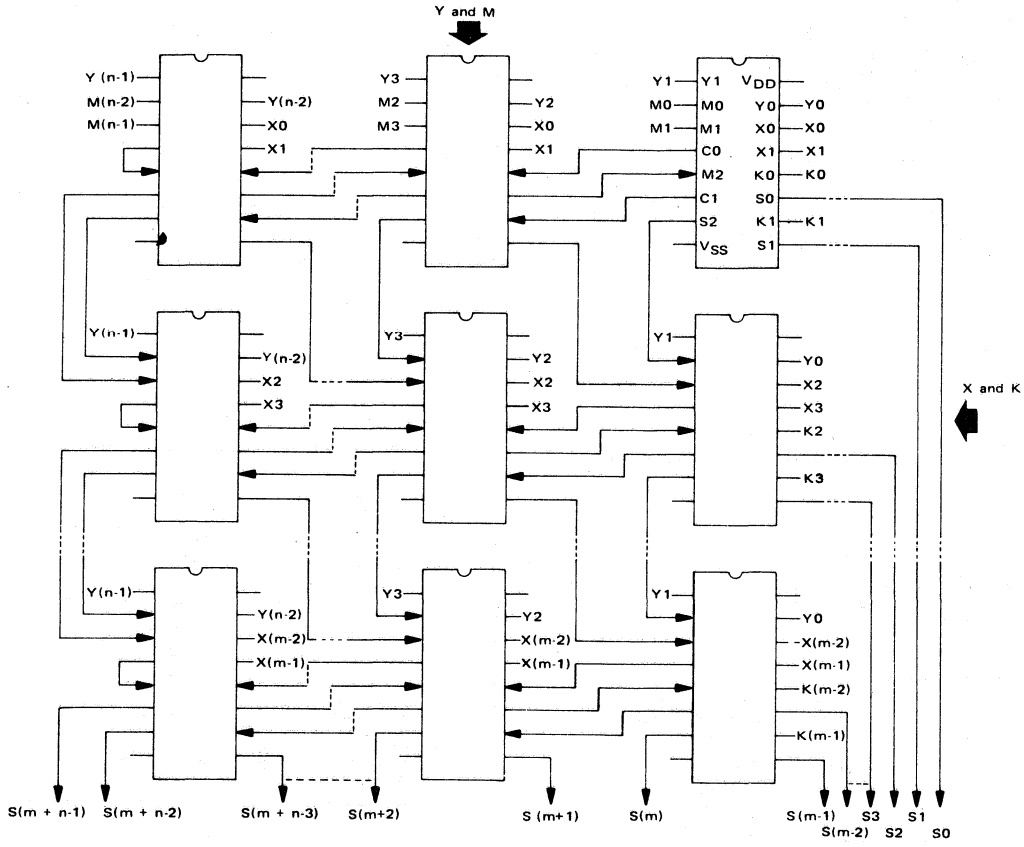
LOGIC DIAGRAM





EXPANSION DIAGRAM

m-Bit by n-Bit Parallel Binary Multiplier (Top View)



S = (X x Y) + K + M Where: x means Arithmetic Times.
+ means Arithmetic Plus.

S = S(m + n-1) S(m + n-2) - - - S2 S1 S0
X = X(m-1) X (m-2) - - - X2 X1 X0, Y = Y(n-1) Y(n-2) - - - Y2 Y1 Y0
K = K(m-1) K(m-2) - - - K2 K1 K0 and M = M(n-1) M(n-2) - - - M2 M1 M0
(Binary Numbers).

Number of output binary digits = m + n
Number of packages = mxn/4 (For m or n or both odd select next highest even number.)

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14555B
MC14556B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

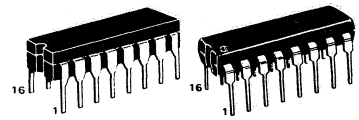
Active High Outputs – MC14555B
Active Low Outputs – MC14556B

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the "high" state, and the MC14556B has the selected output go to the "low" state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other MC14555B or MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Active High or Active Low Outputs
- Low Quiescent Current – 5.0 nA/package typical @ 5 Vdc
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

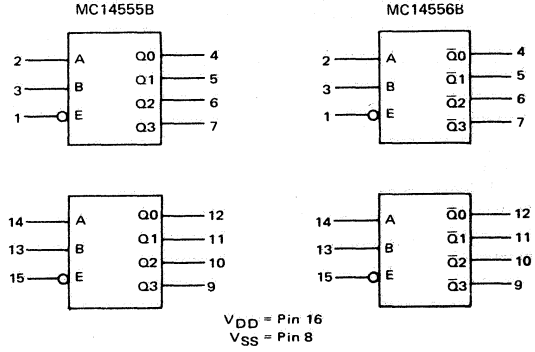
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS MC14555B				OUTPUTS MC14556B			
ENABLE	SELECT									
$\overline{E}$	B	A	Q3	Q2	Q1	Q0	$\overline{Q3}$	$\overline{Q2}$	$\overline{Q1}$	$\overline{Q0}$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.85 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.7 μA/kHz) f + I_{DD}							
		15	I_T = (2.6 μA/kHz) f + I_{DD}							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

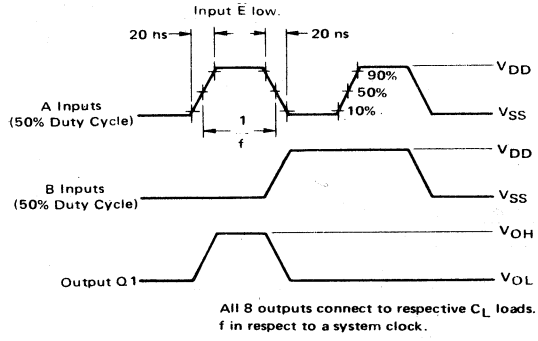
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time – A, B to Output	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns	t_{PHL}	5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 62 ns		10	–	95	190	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	140	
Propagation Delay Time – E to Output	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 115 ns	t_{PHL}	5.0	–	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 52 ns		10	–	85	170	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 40 ns		15	–	65	130	

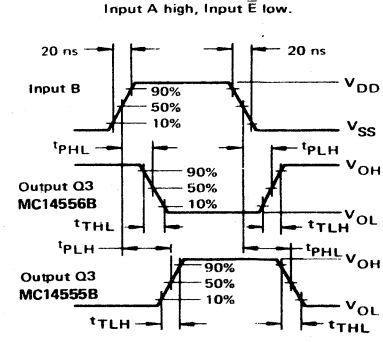
*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

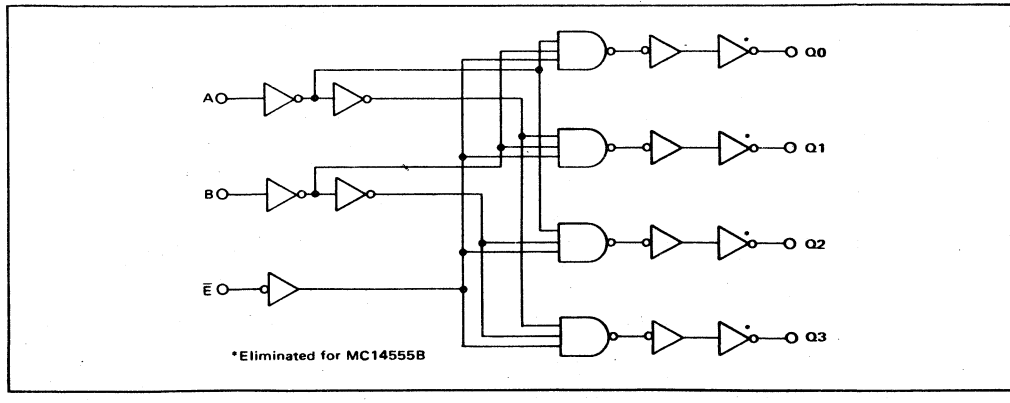


All 8 outputs connect to respective C_L loads.
f in respect to a system clock.

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



LOGIC DIAGRAM
(1/2 of Dual)



MOTOROLA

MC14557B

1-TO-64 BIT VARIABLE LENGTH SHIFT REGISTER

The MC14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers. characteristics can be found on the Family Data Sheet.

- Quiescent Current = 10 nA/package typical @ 5 Vdc
- 1-64 Bit Programmable Length
- Q and $\overline{Q}$ Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- 8 MHz Operation @ V_{DD} = 10 Vdc Typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range -- AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LENGTH SELECT TRUTH TABLE

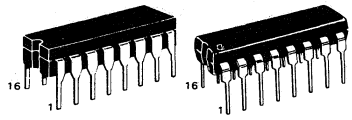
L32	L16	L8	L4	L2	L1	Register Length
0	0	0	0	0	0	1-Bit
0	0	0	0	0	1	2-Bits
0	0	0	0	1	0	3-Bits
0	0	0	0	1	1	4-Bits
0	0	0	1	0	0	5-Bits
0	0	0	1	0	1	6-Bits
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	0	0	0	0	0	33-Bits
1	0	0	0	0	1	34-Bits
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	0	0	61-Bits
1	1	1	1	0	1	62-Bits
1	1	1	1	1	0	63-Bits
1	1	1	1	1	1	64-Bits

Note: Length equals the sum of the binary length control subscripts plus one.

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

1-TO-64 BIT
VARIABLE LENGTH
SHIFT REGISTER



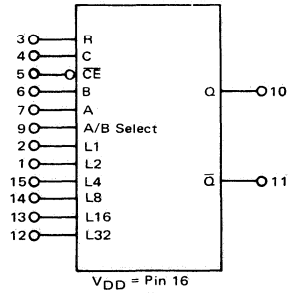
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

Inputs				Output
R	A/B	Clock	$\overline{CE}$	Q
0	0	↑	0	B
0	1	↑	0	A
0	0	1	↓	B
0	1	1	↓	A
1	X	X	X	0

Q is the output of the first selected shift register stage.
X = Don't Care.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.75 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.5 µA/kHz) f + I_{DD}							
		15	I_T = (5.25 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Minimum No. of Bits Selected	Typical Setup Time B → $\overline{CE}$ ns	Length Select Lines = 1
1	180	None
2	120	L1
3	90	L2
5	60	L4
9	30	L8
17	0	L16
33	-30	L32

SETUP TIME CHART

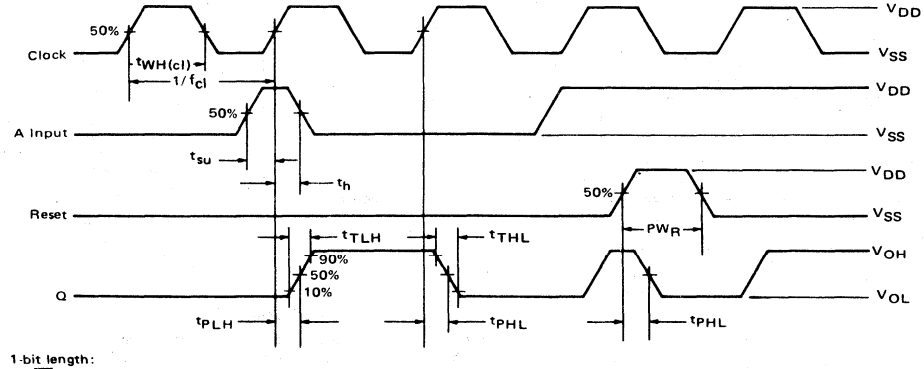
The nature of the length select logic causes the setup time to vary with the number of bits selected. The following table summarizes the typical variation at V_{DD} = 10 V, T_A = 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{PLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{PHL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
(C or CE to Q or Q)						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 167 ns		10	–	200	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
(R to Q or Q)						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 390 ns		5.0	–	475	550	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 157 ns		10	–	190	380	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	–	140	280	
Clock Pulse Width	$t_{WH(C)}$	5.0	440	220	–	ns
		10	136	68	–	
		15	100	50	–	
Reset Pulse Width	$t_{WH(R)}$	5.0	600	300	–	ns
		10	180	90	–	
		15	120	60	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.7	MHz
		10	–	8.0	5.0	
		15	–	10.5	6.7	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Data to Clock Setup Time (A or B to C or CE)	t_{su}	5.0	900	450	–	ns
L1, L2, L4, L8, L16, L32 = 0		10	360	180	–	
		15	170	135	–	
Data to Clock Hold Time (A or B to C or CE)	t_h	5.0	-225	-450	–	ns
L1, L2, L4, L8, L16, L32 = 0		10	- 90	-180	–	
		15	- 60	-135	–	
Reset Fall Time	t_{TLH}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	

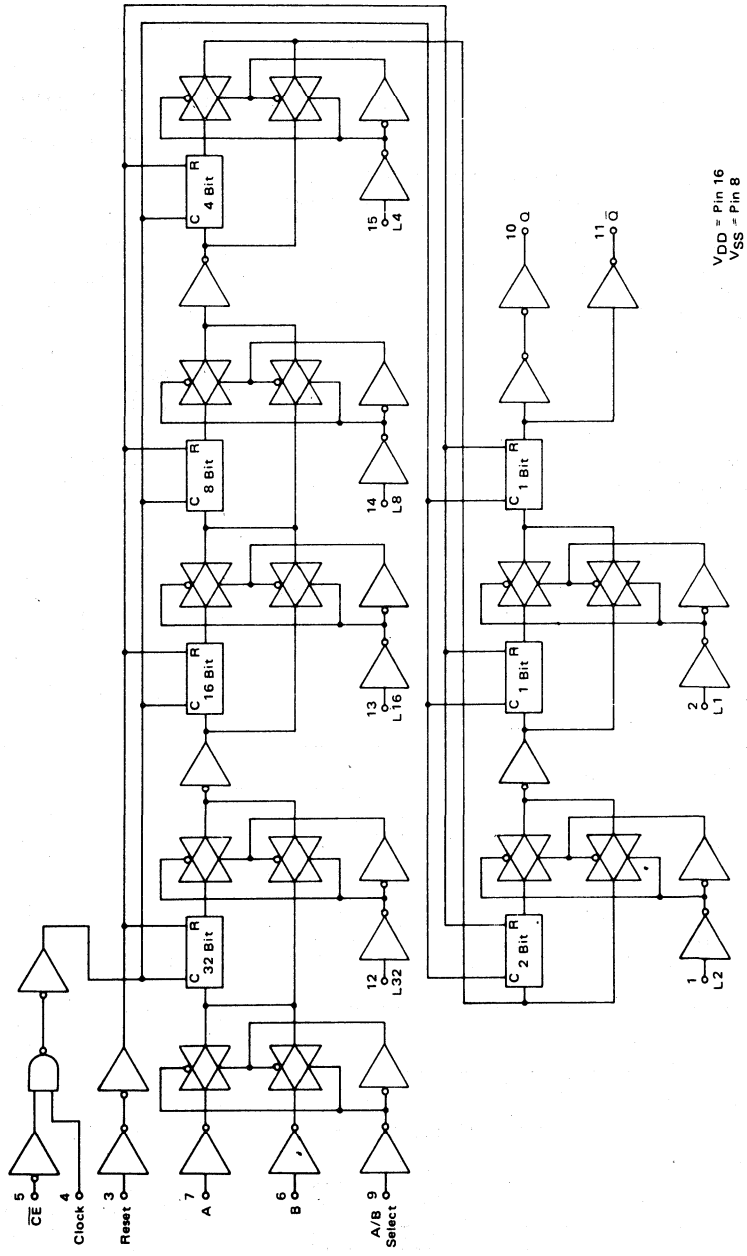
*The formula given is for the typical characteristics only.

TIMING DIAGRAM



1-bit length:
$\overline{CE}$ = 0
A/B = 1
L1 = L2 = L4 = L8 = L16 = L32 = 0

LOGIC DIAGRAM



MOTOROLA

MC14558B

BCD-TO-SEVEN SEGMENT DECODER

The MC14558B decodes 4-bit binary coded decimal data dependent on the state of auxiliary inputs, Enable and RBI, and provides an active high seven-segment output for a display driver.

An auxiliary input truth table is shown, in addition to the BCD to seven-segment truth table, to indicate the functions available with the two auxiliary inputs.

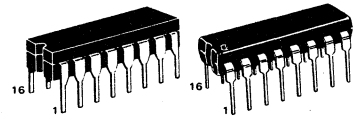
Leading Zero blanking is easily obtained with an external flip-flop in time division multiplexed systems displaying most significant decade first.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Segment Blanking for All Illegal Input Combinations
- Lamp Test Function
- Capability for Suppression of Non-Significant Zeros
- Lamp Intensity Function
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT DECODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

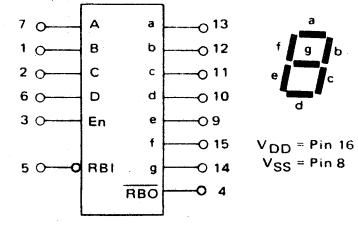
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

AUXILIARY INPUT TRUTH TABLE

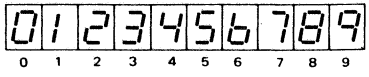
Enable Pin 3	RBI Pin 5	BCD Input Code	RBO Pin 4	Function Performed
0	0	X	0	Lamp Test
0	1	X	1	Blank Segments
1	1	0	1	Display Zero
1	0	0	0	Blank Segments
1	X	1-9	1	1-9 Displayed

X = Don't Care
RBI = Ripple Blanking Input
RBO = Ripple Blanking Output

BLOCK DIAGRAM



DISPLAY



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.4 µA/kHz) f + I_{DD}							
		15	I_T = (3.6 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C; see Figure 1)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 495 ns		5.0	–	580	1160	
t_{PLH} = (0.66 ns/pF) C_L + 187 ns		10	–	220	440	
t_{PLH} = (0.5 ns/pF) C_L + 120 ns		15	–	145	230	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 695 ns		5.0	–	780	1560	
t_{PHL} = (0.66 ns/pF) C_L + 242 ns		10	–	275	550	
t_{PHL} = (0.5 ns/pF) C_L + 160 ns		15	–	185	370	

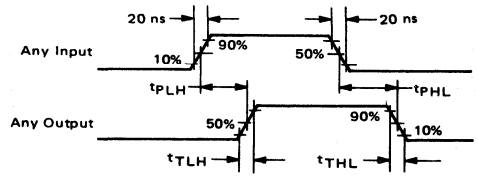
*The formula given is for the typical characteristics only.

TRUTH TABLE

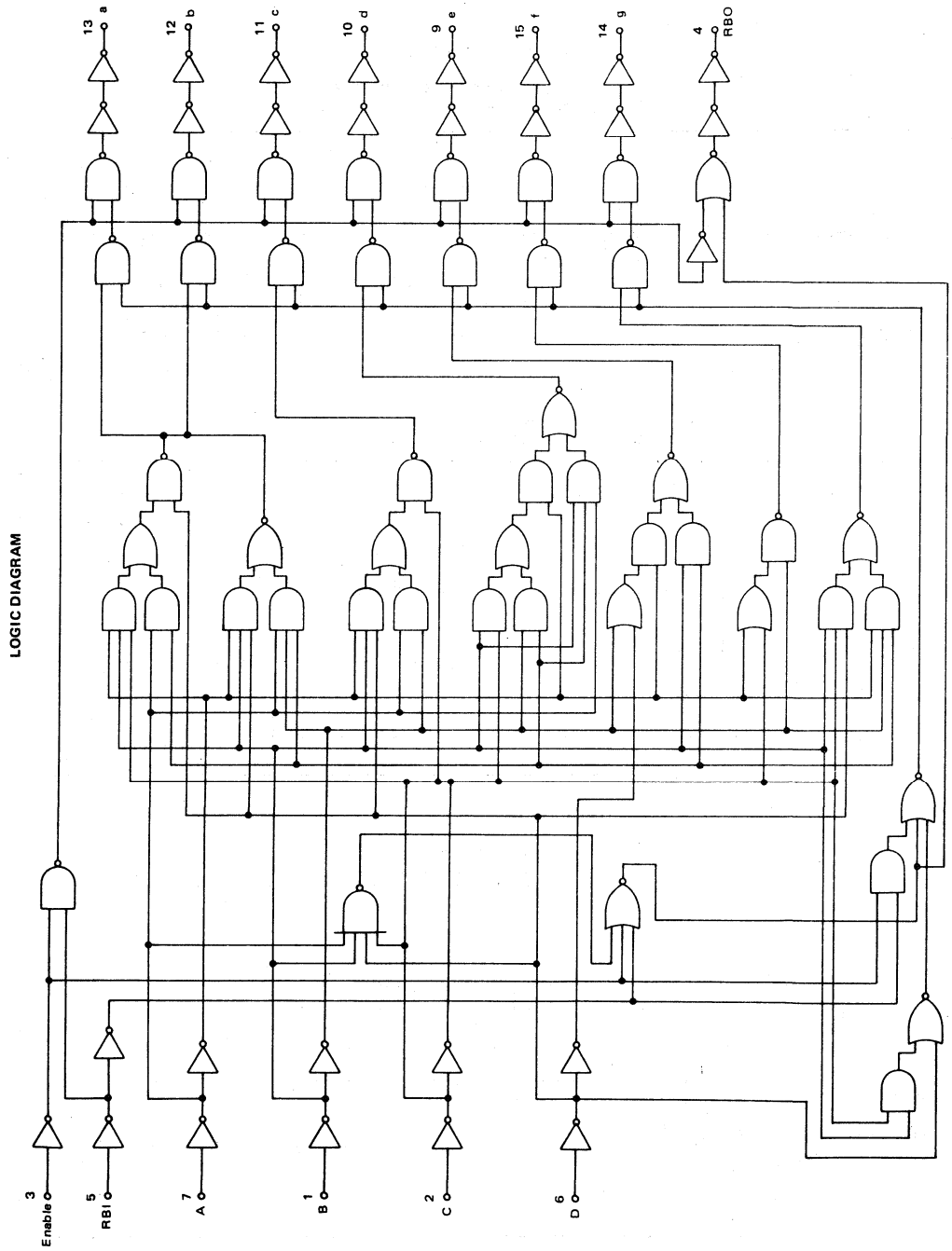
INPUTS						OUTPUTS*								
En Pin 3	$\overline{RBI}$ Pin 5	D Pin 6	C Pin 2	B Pin 1	A Pin 7	a Pin 13	b Pin 12	c Pin 11	d Pin 10	e Pin 9	f Pin 15	g Pin 14	$\overline{RBO}$ Pin 4	DISPLAY
1	1	0	0	0	0	1	1	1	1	1	1	0	1	0
1	X	0	0	0	1	0	0	0	0	1	1	0	1	1
1	X	0	0	1	0	1	1	0	1	1	0	1	1	2
1	X	0	0	1	1	1	1	1	1	0	0	1	1	3
1	X	0	1	0	0	0	1	1	0	0	1	1	1	4
1	X	0	1	0	1	1	0	1	1	0	1	1	1	5
1	X	0	1	1	0	0	0	1	1	1	1	1	1	6
1	X	0	1	1	1	1	1	1	0	0	0	0	1	7
1	X	1	0	0	0	1	1	1	1	1	1	1	1	8
1	X	1	0	0	1	1	1	1	0	0	1	1	1	9
1	0	0	0	0	0	0	0	0	0	0	0	0	0	Blank
0	0	X	X	X	X	1	1	1	1	1	1	1	0	8
0	1	X	X	X	X	0	0	0	0	0	0	0	1	Blank

*All non-valid BCD input codes produce a blank display.
X = Don't Care

FIGURE 1 – SIGNAL WAVEFORMS



LOGIC DIAGRAM



TYPICAL APPLICATIONS

FIGURE 2 – LEADING AND TRAILING ZERO SUPPRESSION WITH LAMP TEST

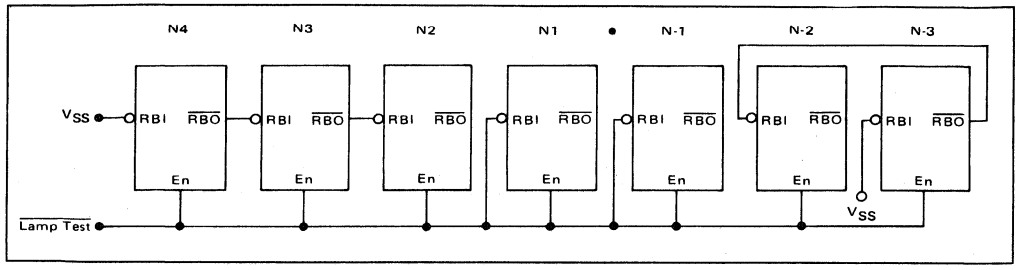


FIGURE 3 – LEADING AND TRAILING ZERO SUPPRESSION WITH PWM INTENSITY BLANKING AND NO LAMP TEST

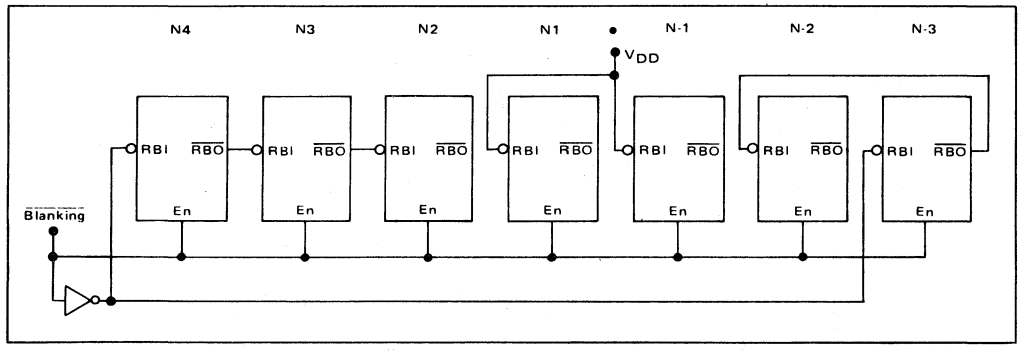
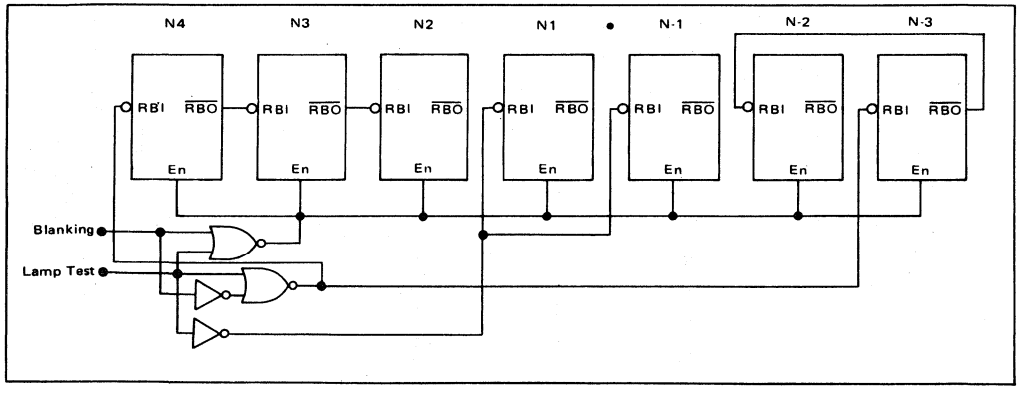


FIGURE 4 – ZERO SUPPRESSION WITH LAMP TEST AND INTENSITY BLANKING



MOTOROLA

MC14559B

FOR COMPLETE DATA
SEE MC14549B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

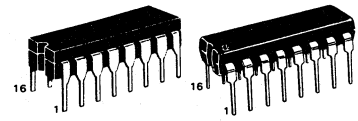
SUCCESSIVE APPROXIMATION REGISTERS

SUCCESSIVE APPROXIMATION REGISTERS

The MC14549B and MC14559B successive approximation registers are 8-bit registers providing all the digital control and storage necessary for successive approximation analog-to-digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the MC14549B is required in the cascaded mode when greater than 8 bits are desired. The Feed Forward (FF) of the MC14559B is used for register shortening where End-of-Conversion (EOC) is required after less than eight cycles.

Applications for the MC14549B and MC14559B include analog-to-digital conversion, with serial and parallel outputs.

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the MC1408 8-Bit D/A Converter
- All Control Inputs Positive-Edge Triggered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



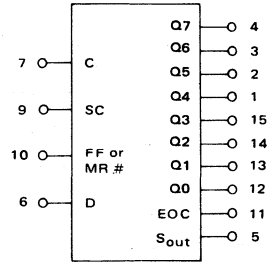
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

#For MC14549B Pin 10 is MR input
For MC14559B Pin 10 is FF input

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLES

MC14549B

SC	$SC_{(t-1)}$	MR	$MR_{(t-1)}$	Clock	Action
X	X	X	X	⌐_	None
X	X	1	X	_⌐	Reset
1	0	0	0	_⌐	Start Conversion
1	X	0	1	_⌐	Start Conversion
1	1	0	0	_⌐	Continue Conversion
0	X	0	X	_⌐	Continue Previous Operation

MC14559B

SC	$SC_{(t-1)}$	EOC	Clock	Action
X	X	X	⌐_	None
1	0	0	_⌐	Start Conversion
X	1	0	_⌐	Continue Conversion
0	0	0	_⌐	Continue Conversion
0	X	1	_⌐	Retain Conversion Result
1	X	1	_⌐	Start Conversion

X = Don't Care
t-1 = State at Previous Clock _⌐

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14560B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

NBCD ADDER

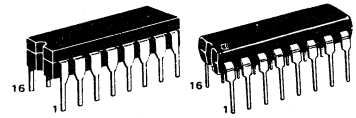
NBCD ADDER

The MC14560B adds two 4-bit numbers in NBCD (natural binary coded decimal) format, resulting in sum and carry outputs in NBCD code.

This device can also subtract when one set of inputs is complemented with a 9's Complementer (MC14561B).

All inputs and outputs are active high. The carry input for the least significant digit is connected to V_{SS} for no carry in.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Single Supply Operation – Positive or Negative
- Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

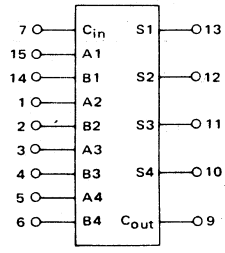
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE*

INPUT									OUTPUT				
A4	A3	A2	A1	B4	B3	B2	B1	C_{in}	C_{out}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	1	1	1	1	0	0	1

*Partial truth table to show logic operation for representative input values.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	–0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	**0.005**	5.0	–	150	μAdc
(Per Package)		10	–	10	–	**0.010**	10	–	300	
		15	–	20	–	**0.015**	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	**0.005**	20	–	150	μAdc
(Per Package)		10	–	40	–	**0.010**	40	–	300	
		15	–	80	–	**0.015**	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.68 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.35 μA/kHz) f + I_{DD}							
		15	I_T = (5.03 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
A or B to S						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns		5.0	–	750	2100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 297 ns		10	–	330	900	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 195 ns		15	–	220	675	
A or B to C_{out}						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	–	650	1800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	450	
C_{in} to C_{out}						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	550	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 187 ns		10	–	220	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	–	160	450	
Turn-Off Delay Time	t_{PLH}					ns
C_{in} to S						
t_{PLH} = (1.7 ns/pF) C_L + 715 ns		5.0	–	800	2250	
t_{PLH} = (0.66 ns/pF) C_L + 197 ns		10	–	350	975	
t_{PLH} = (0.5 ns/pF) C_L + 215 ns		15	–	240	750	
Turn-On Delay Time	t_{PHL}					ns
C_{in} to S						
t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	–	650	1800	
t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	600	
t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	450	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION WAVEFORMS

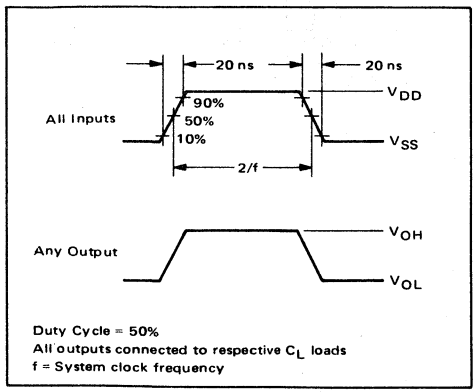
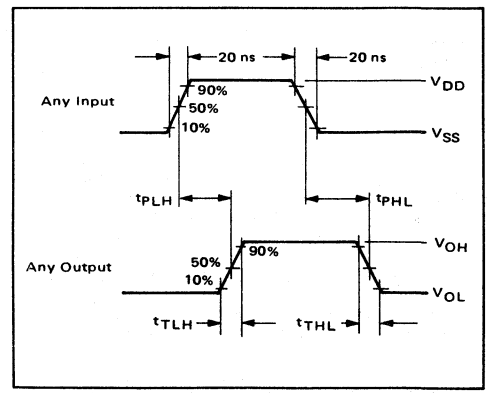


FIGURE 2 – SWITCHING TIME WAVEFORMS



FUNCTIONAL EQUIVALENT LOGIC DIAGRAM

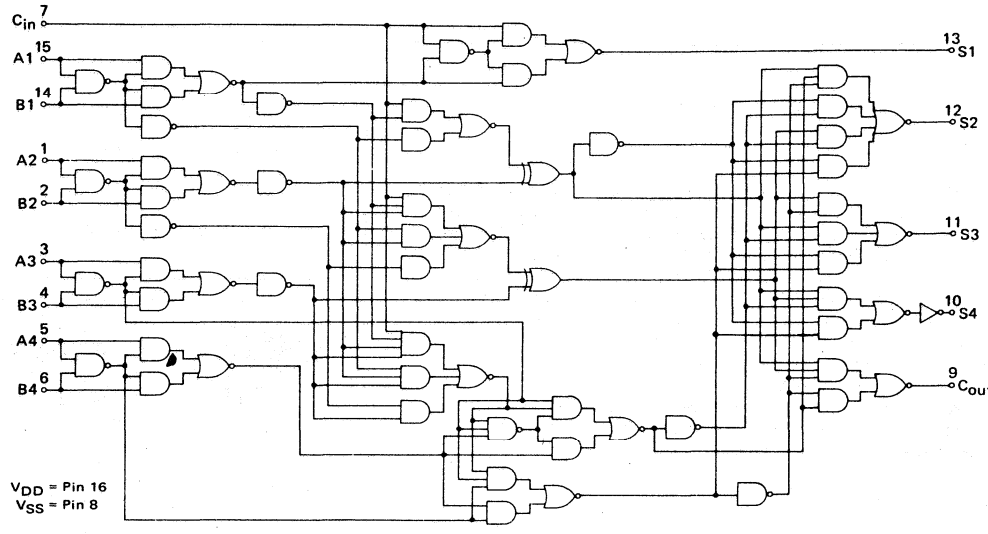
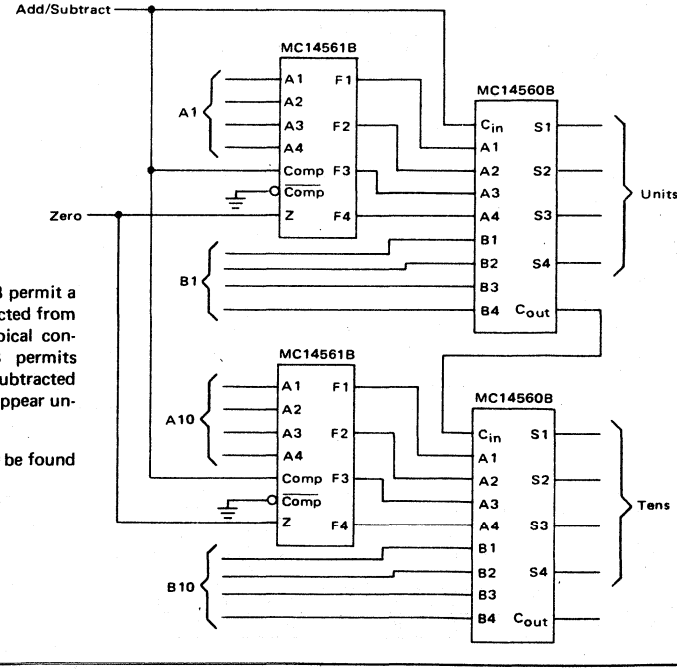


FIGURE 3 – PARALLEL ADD/SUBTRACT CIRCUIT



One MC14560B and MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in this typical configuration. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

Additional applications data may be found in Application Note AN-738.

TRUTH TABLE

Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	B

X = Don't Care

MOTOROLA

MC14561B

9's COMPLEMENTER

The MC14561B 9's complementer is a companion to the MC14560B NBCD adder to allow BCD subtraction. A BCD number (8-4-2-1 code) is applied to the inputs ($A1 = 2^0$, $A2 = 2^1$, $A3 = 2^2$, $A4 = 2^3$). If the complement control (Comp) is low, the BCD number appears at the outputs unmodified. The complement disable (Comp) allows the complement control to be gated, or an inverted control signal to be used. If the complement input is high and the disable input low, the 9's complement of the number is displayed at the outputs. The zero control (Z), when high, forces the outputs low regardless of the state of the other inputs.

When the MC14561B is used to perform BCD subtraction in conjunction with the MC14560B NBCD adder, the complement control becomes an add/subtract control.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Propagation Delay = 160 ns typical at V_{DD} = 10 Vdc
- All Inputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

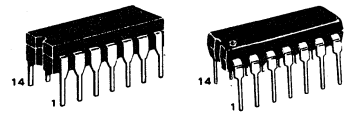
Z	Comp	$\overline{Comp}$	F1	F2	F3	F4	Mode
0	0	0	A1	A2	A3	A4	Straight-through
0	0	1					
0	1	1					
0	1	0	$\overline{A1}$	A2	$A2\overline{A3} + \overline{A2}A3$	$\overline{A2}A3\overline{A4}$	Complement
1	X	X	0	0	0	0	Zero

X = Don't Care.

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

9's COMPLEMENTER



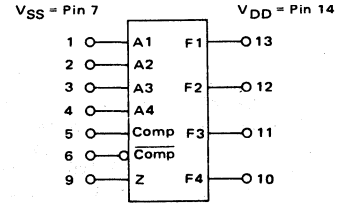
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.5 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.0 µA/kHz) f + I_{DD}							
		15	I_T = (4.5 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

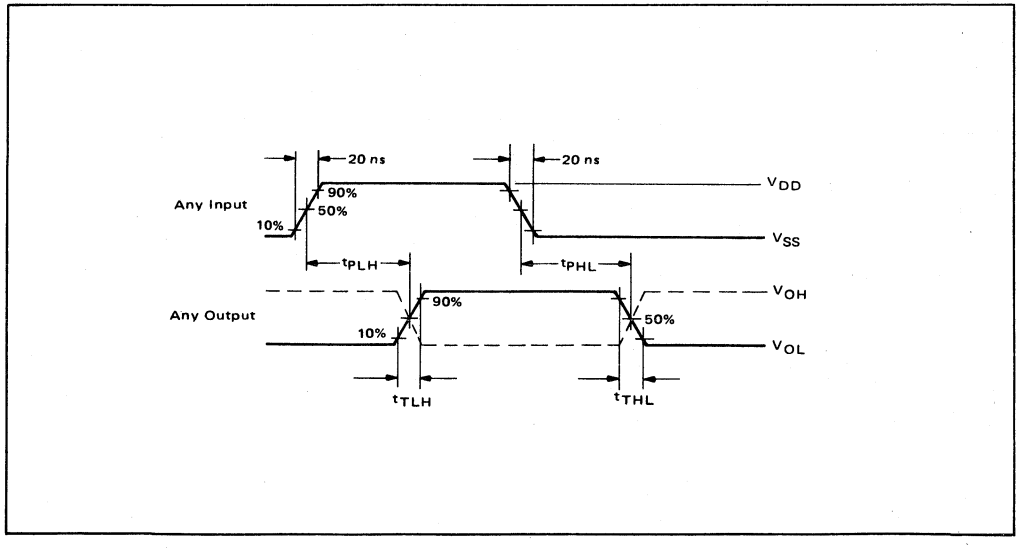
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

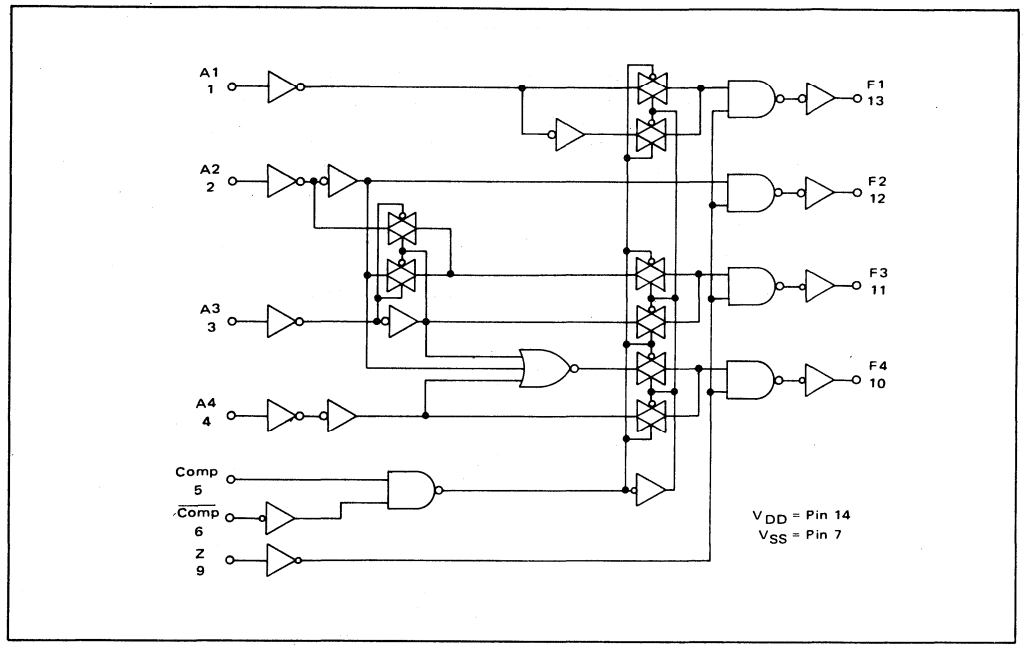
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns	t_{PHL}	5.0	–	400	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 127 ns		10	–	160	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	120	300	

*The formula given is for the typical characteristics only.

FIGURE 1 – SWITCHING TIME WAVEFORMS



LOGIC DIAGRAM



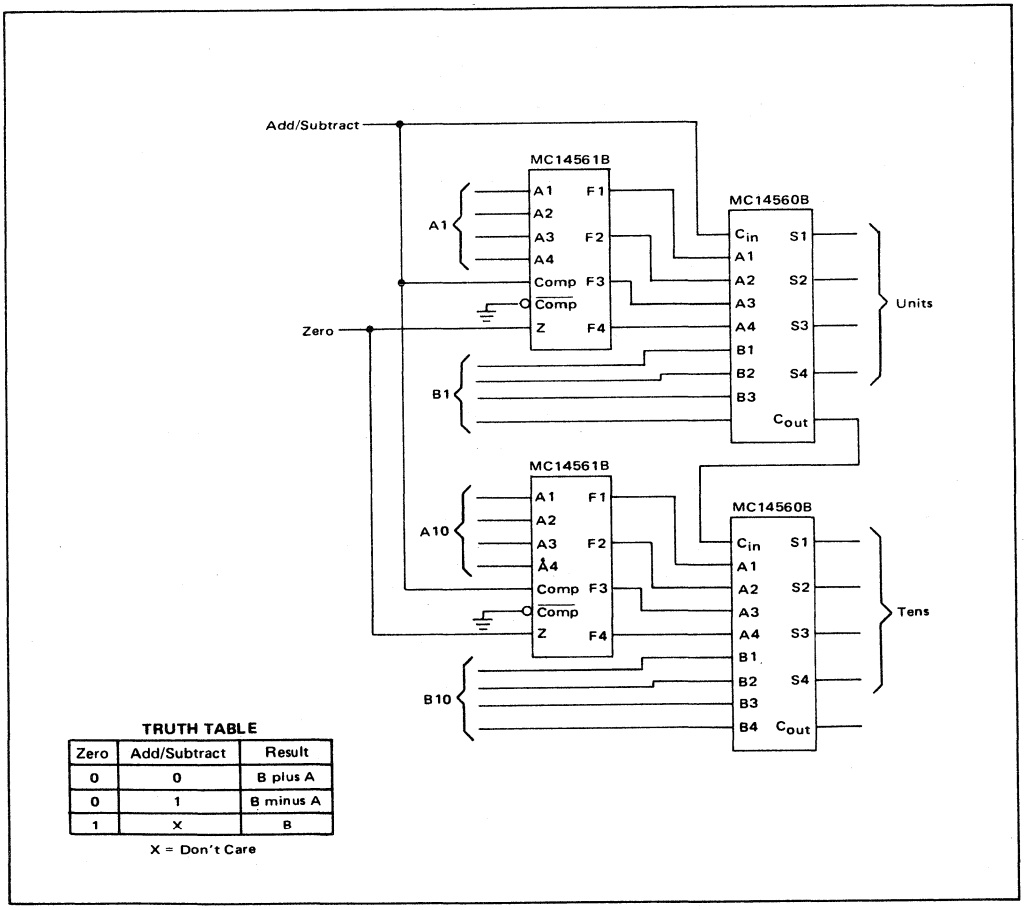
TRUTH TABLE – COMPLEMENT MODE
(Z = 0, Comp = 1, $\overline{\text{Comp}}$ = 0)

	Decimal Equivalent Input	Inputs				Decimal Equivalent Output	Outputs			
		A4	A3	A2	A1		F4	F3	F2	F1
	0	0	0	0	0	9	1	0	0	1
	1	0	0	0	1	8	1	0	0	0
	2	0	0	1	0	7	0	1	1	1
	3	0	0	1	1	6	0	1	1	0
	4	0	1	0	0	5	0	1	0	1
	5	0	1	0	1	4	0	1	0	0
	6	0	1	1	0	3	0	0	1	1
	7	0	1	1	1	2	0	0	1	0
	8	1	0	0	0	1	0	0	0	1
	9	1	0	0	1	0	0	0	0	0
Illegal BCD Input Codes	10	1	0	1	0	7	0	1	1	1
	11	1	0	1	1	6	0	1	1	0
	12	1	1	0	0	5	0	1	0	1
	13	1	1	0	1	4	0	1	0	0
	14	1	1	1	0	3	0	0	1	1
	15	1	1	1	1	2	0	0	1	0

TYPICAL APPLICATIONS

One MC14560B and one MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in the typical configurations in Figures 2 and 3. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

FIGURE 2 – PARALLEL ADD/SUBTRACT CIRCUIT (10's COMPLEMENT)

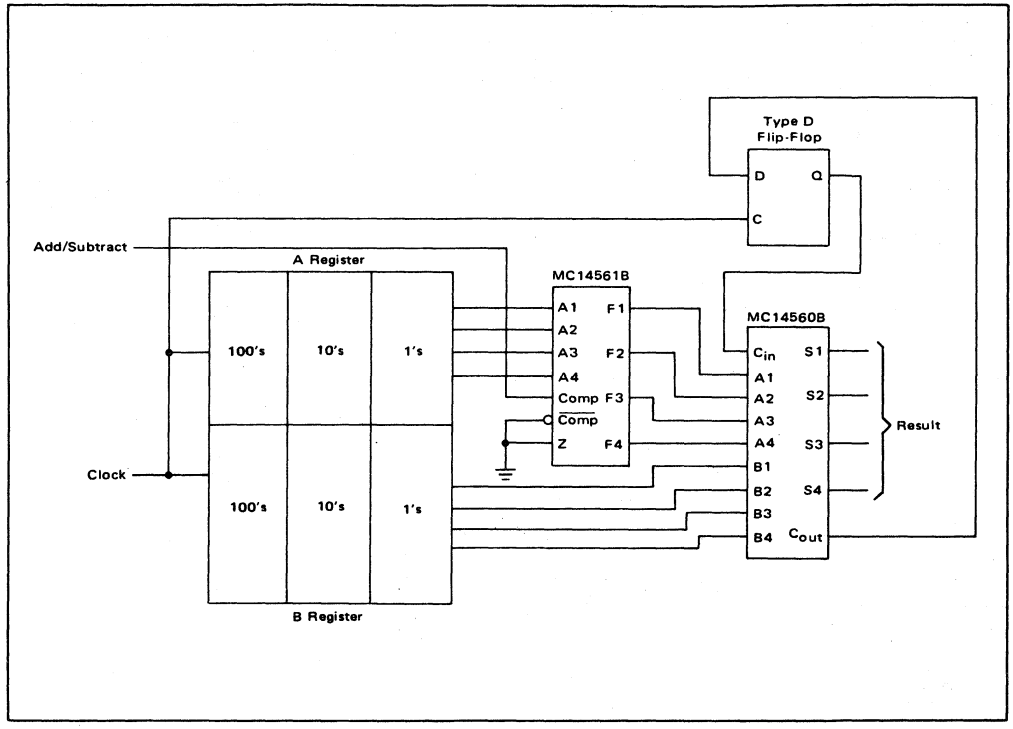


TRUTH TABLE

Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	B

X = Don't Care

FIGURE 3 – SERIAL ADD/SUBTRACT CIRCUIT



Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14562B

128-BIT STATIC SHIFT REGISTER

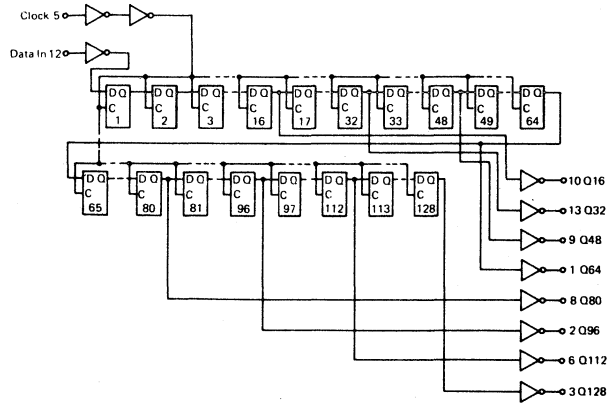
The MC14562B is a 128-bit static shift register constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data is clocked in and out of the shift register on the positive edge of the clock input. Data outputs are available every 16 bits, from 16 through bit 128. This complementary MOS shift register is primarily used where low power dissipation and/or high noise immunity is desired.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- Single Supply Operation – Positive or Negative
- Fully Static Operation
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 5.6 MHz Operation @ V_{DD} = 10 Vdc
- Cascadable to Provide Longer Shift Register Lengths – 1.5 MHz Operation @ V_{DD} = 10 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

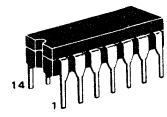
LOGIC DIAGRAM



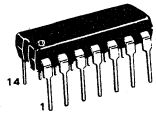
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

128-BIT STATIC SHIFT REGISTER.



L SUFFIX
CERAMIC PACKAGE
CASE 632

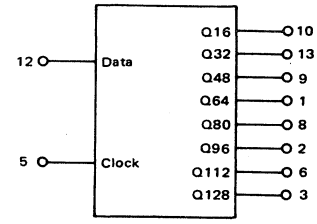


P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



Pins 4 and 11 not used.

V_{DD} = Pin 14
V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.94 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.81 µA/kHz) f + I_{DD}							
		15	I_T = (5.52 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

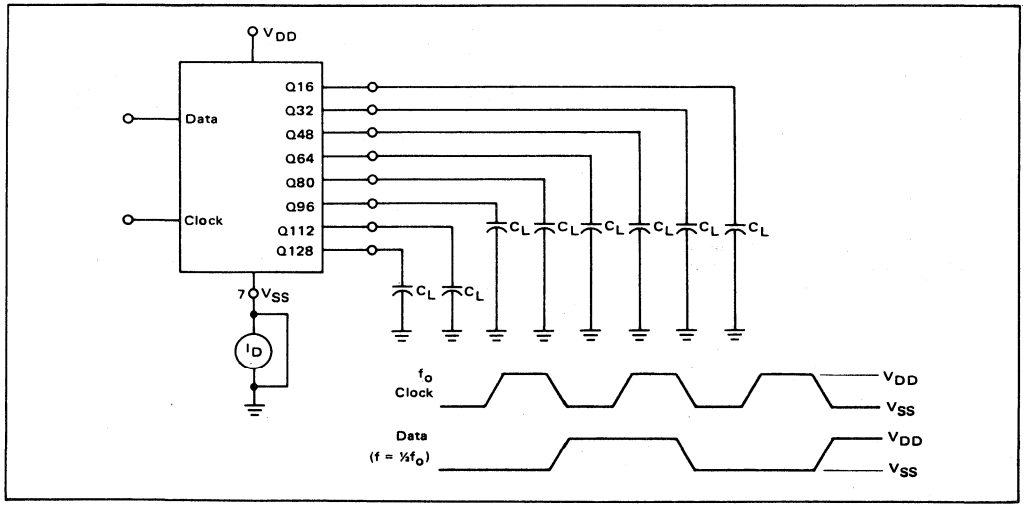
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

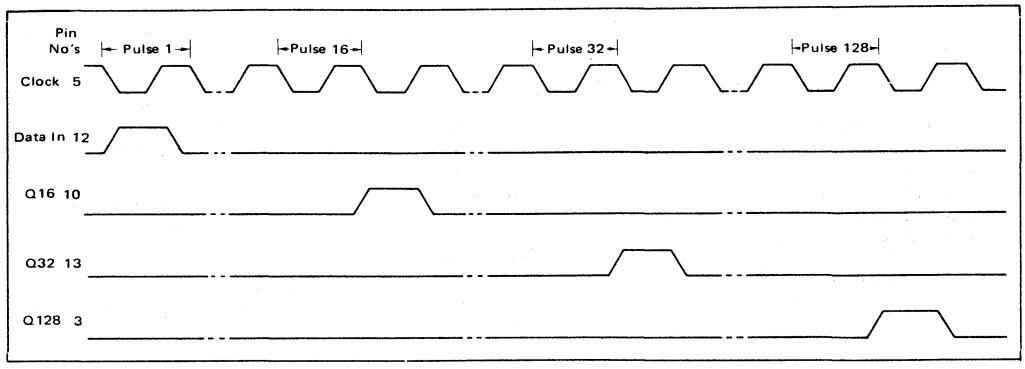
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 515 ns		5.0	–	600	1200	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	–	250	500	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	340	
Clock Pulse Width	t_{WH}	5.0	600	300	–	ns
(50% Duty Cycle)		10	220	110	–	
		15	150	75	–	
Clock Pulse Frequency	f_{cl}	5.0	–	1.9	1.1	MHz
		10	–	5.6	3.0	
		15	–	8.0	4.0	
Data to Clock Setup Time	$t_{su(1)}$	5.0	-20	-170	–	ns
		10	-10	-64	–	
		15	0	-60	–	
	$t_{su(0)}$	5.0	-20	-91	–	ns
		10	-10	-58	–	
		15	0	-48	–	
Data to Clock Hold Time	$t_{h(1)}$	5.0	350	263	–	ns
		10	165	109	–	
		15	155	100	–	
	$t_{h(0)}$	5.0	350	267	–	ns
		10	200	140	–	
		15	140	93	–	

* The formula given is for the typical characteristics only.

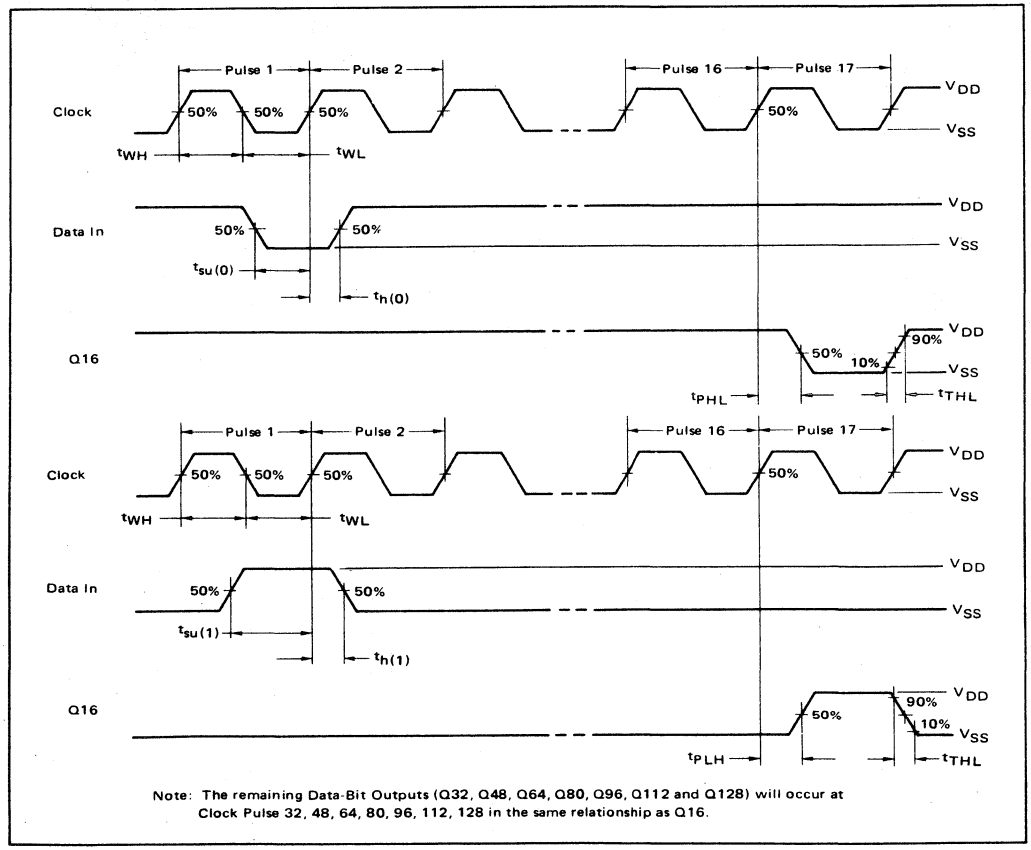
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



TIMING DIAGRAM



AC TEST WAVEFORMS



Note: The remaining Data-Bit Outputs (Q32, Q48, Q64, Q80, Q96, Q112 and Q128) will occur at Clock Pulse 32, 48, 64, 80, 96, 112, 128 in the same relationship as Q16.

MOTOROLA

MC14566B

INDUSTRIAL TIME BASE GENERATOR

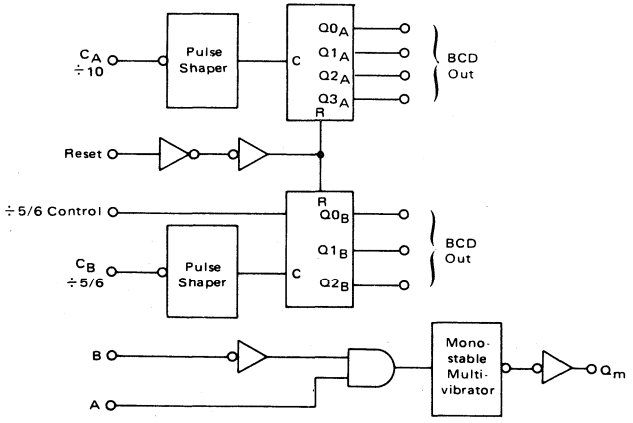
The MC14566B industrial time base generator is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of a divide-by-10 ripple counter and a divide-by-5 or divide-by-6 ripple counter to permit stable time generation from a 50 or 60 Hz line. By cascading this device as divide-by-60 counters, seconds and minutes can be counted and are available in BCD format at the circuit outputs. An internal monostable multivibrator is included whose output can be used as a reset or clock pulse providing additional frequency flexibility. Also a pin has been included to allow divide-by-5 counting for generating 1.0 Hz from European 50 Hz line.

- Negative Edge Triggered Counters for Ease of Cascading
- Pulse Shapers on Counter Inputs Accept Slow Input Rise Times
- Monostable Multivibrator Positive or Negative Edge Triggered
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

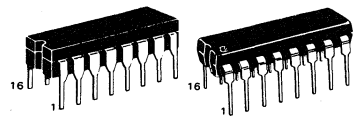
EXPANDED BLOCK DIAGRAM



CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

INDUSTRIAL
TIME BASE GENERATOR



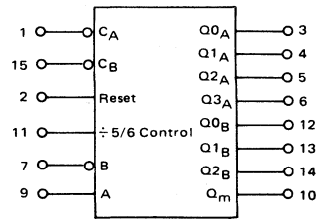
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.0 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.0 µA/kHz) f + I_{DD}							
		15	I_T = (3.0 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time, Clock to $Q3_A$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1365 ns		5.0	–	1450	4500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 497 ns		10	–	530	1500	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 295 ns		15	–	320	1000	
Propagation Delay Time, Reset to $Q3_A$	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 845 ns		5.0	–	930	3000	
t_{PHL} = (0.66 ns/pF) C_L + 282 ns		10	–	315	1000	
t_{PHL} = (0.5 ns/pF) C_L + 185 ns		15	–	210	750	
Clock Pulse Width	$t_{WH(cl)}$					ns
		5.0	1200	400	–	
		10	400	125	–	
		15	270	90	–	
Reset Pulse Width	$t_{WH(R)}$					ns
		5.0	1200	400	–	
		10	400	125	–	
		15	270	90	–	
Clock Pulse Frequency	f_{cl}					MHz
		5.0	–	1.0	0.3	
		10	–	2.5	1.0	
		15	–	4.2	1.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Monostable Multivibrator Pulse Width	$t_{WH(Q_m)}$					ns
		5.0	1200	2800	–	
		10	400	900	–	
		15	300	600	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

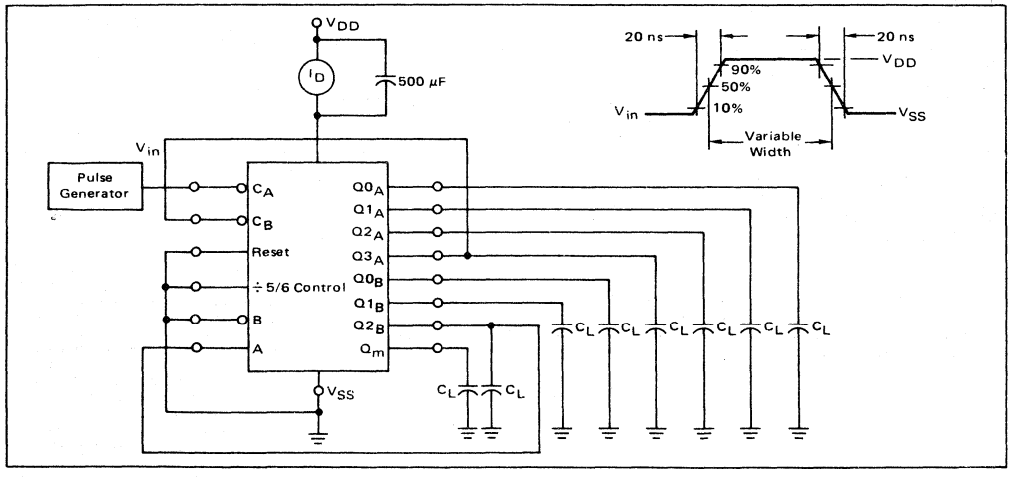
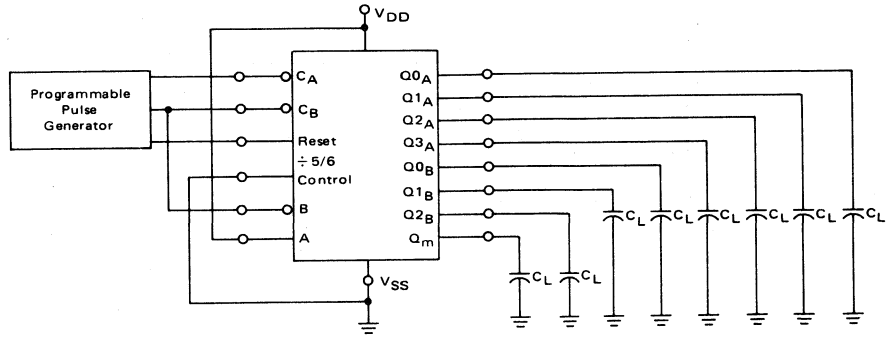
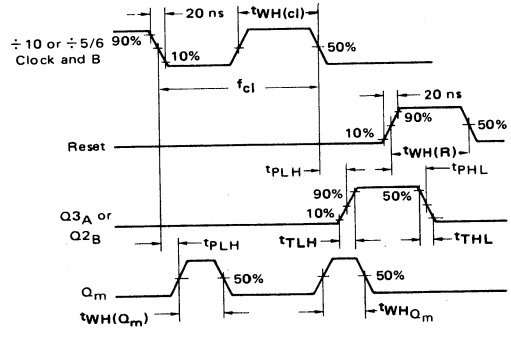


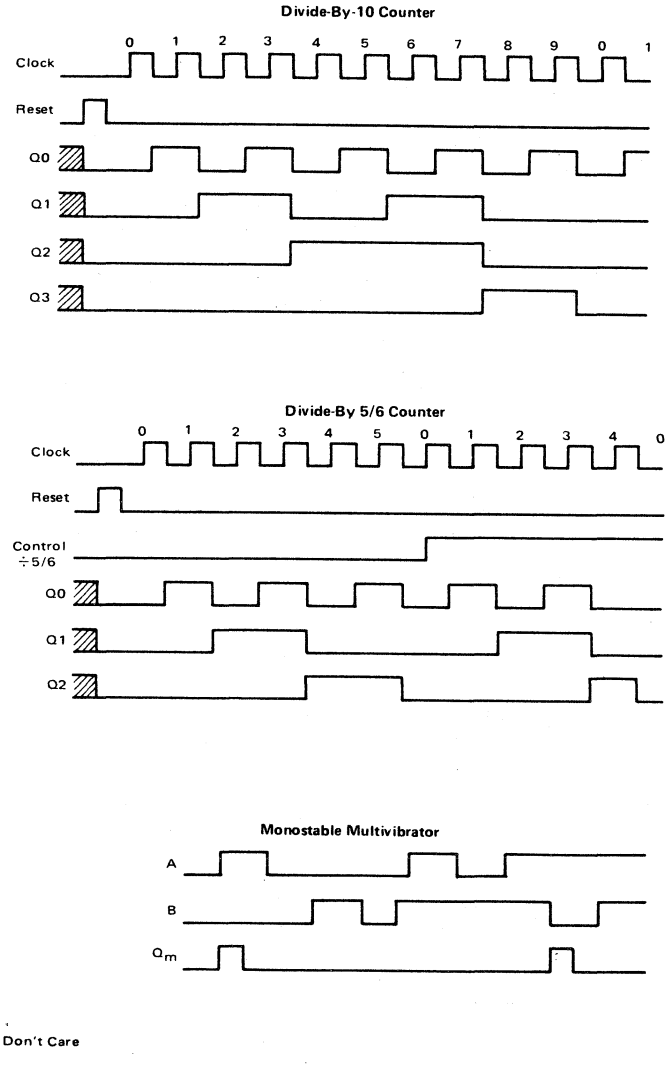
FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



Note: Assume ÷10 Counter at "6" and ÷5/6 Counter at "2" at beginning of sequence.

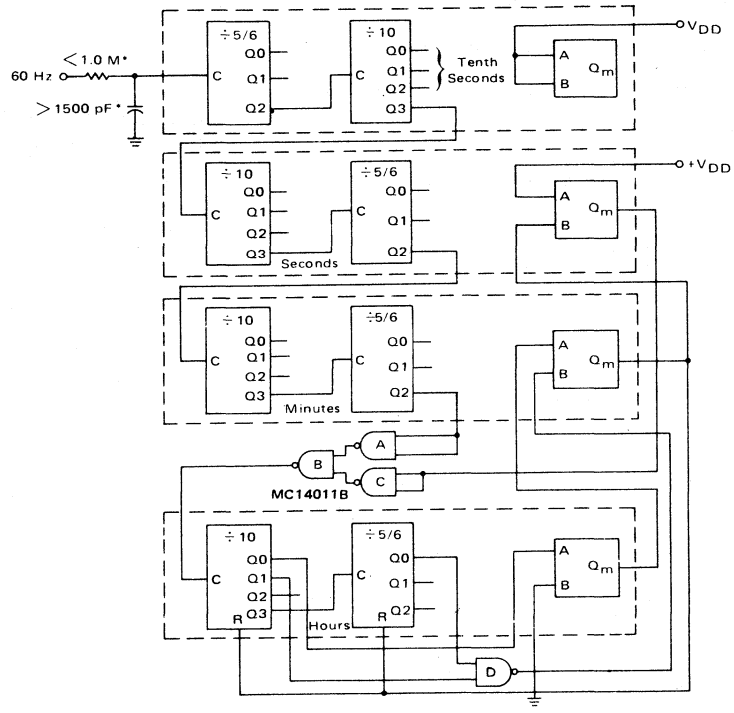


TIMING DIAGRAM



▨ = Don't Care

APPLICATION – 12 HOUR CLOCK



÷ 5/6 Control not shown = V_{SS}

Reset pins not shown = V_{SS}

*Care must be taken in the indicated circuit to filter line transients which may cause "false" counting.

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14568B

PHASE COMPARATOR AND PROGRAMMABLE COUNTERS

The MC14568B consists of a phase comparator, a divide-by-4, 16, 64 or 100 counter and a programmable divide-by-N 4-bit binary counter (all positive-edge triggered) constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a single monolithic structure.

The MC14568B has been designed for use in conjunction with a programmable divide-by-N counter for frequency synthesizers and phase-locked loop applications requiring low power dissipation and/or high noise immunity.

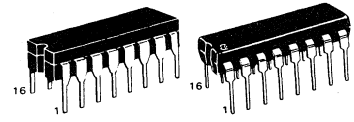
This device can be used with both counters cascaded and the output of the second counter connected to the phase comparator (CTL high), or used separate of the programmable divide-by-N counter, for example cascaded with MC14569B (CTL low), MC14522B or MC14526B.

- Quiescent Current = 5.0 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PHASE COMPARATOR AND PROGRAMMABLE COUNTERS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

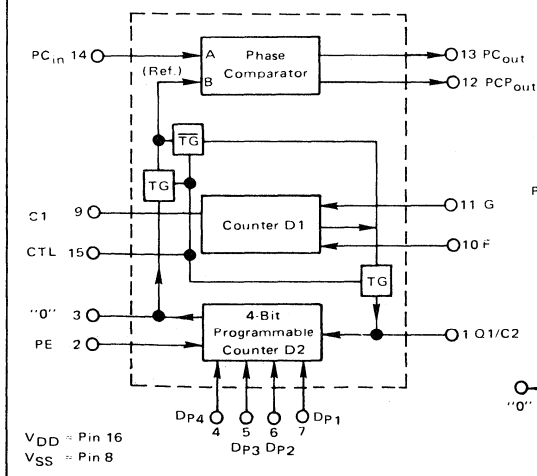
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

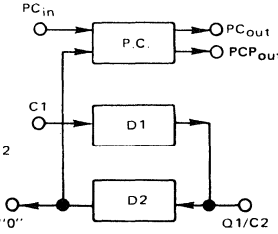
F Pin 10	G Pin 11	Division Ratio of Counter D1
0	0	4
0	1	16
1	0	64
1	1	100

The divide-by-zero state on the programmable divide-by-N 4-bit binary counter, D2, is illegal.

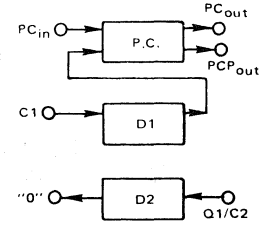
BLOCK DIAGRAM



CTL HIGH



CTL LOW



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage#† "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.2\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (0.4\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (0.9\ \mu A/kHz)\ f + I_{DD}$							
Three-State Leakage Current, Pins 1, 13 (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current, Pins 1, 13 (CL/CP Devices)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50)\ V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

†Pin 15 is connected to V_{SS} or V_{DD} for input voltage test.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	5.0	–	180	360	ns
		10	–	90	180	
		15	–	65	130	
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Minimum Pulse Width, C1, Q1/C2, or PC_{in} Input	t_{WH}	5.0	–	125	250	ns
		10	–	60	120	
		15	–	45	90	
Maximum Clock Rise and Fall Time, C1, Q1/C2, or PC_{in} Input	t_{TLH}, t_{THL}	5.0	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
PHASE COMPARATOR						
Input Resistance	Rin	5.0 to 15	–	10^6	–	MΩ
Input Sensitivity, DC Coupled	–	5.0 to 15	See Input Voltage			
Turn-Off Delay Time, PC_{out} and PCP_{out} Outputs	t_{PHL}	5.0	–	550	1100	ns
		10	–	195	390	
		15	–	120	240	
Turn-On Delay Time, PC_{out} and PCP_{out} Outputs	t_{PHL}	5.0	–	675	1350	ns
		10	–	300	600	
		15	–	190	380	
DIVIDE-BY-4, 16, 64 OR 100 COUNTER (D1)						
Maximum Clock Pulse Frequency	f_{cl}					MHz
Division Ratio = 4, 64 or 100		5.0	3.0	6.0	–	
		10	8.0	16	–	
		15	10	22	–	
Division Ratio = 16		5.0	1.0	2.5	–	MHz
		10	3.0	6.3	–	
		15	5.0	9.7	–	
Propagation Delay Time, Q1/C2 Output	t_{PLH}, t_{PHL}					ns
Division Ratio = 4, 64 or 100		5.0	–	450	900	
		10	–	190	380	
		15	–	130	260	
Division Ratio = 16		5.0	–	720	1440	ns
		10	–	300	600	
		15	–	200	400	
PROGRAMMABLE DIVIDE-BY-N-4-BIT COUNTER (D2)						
Maximum Clock Pulse Frequency (Figure 3a)	f_{cl}	5.0	1.2	1.8	–	MHz
		10	3.0	8.5	–	
		15	4.0	12	–	
Turn-On Delay Time, "0" Output (Figure 3a)	t_{PLH}	5.0	–	450	900	ns
		10	–	190	380	
		15	–	130	260	
Turn-Off Delay Time, "0" Output (Figure 3a)	t_{PHL}	5.0	–	225	450	ns
		10	–	85	170	
		15	–	60	150	
Minimum Preset Enable Pulse Width	$t_{WH(PE)}$	5.0	–	75	250	ns
		10	–	40	100	
		15	–	30	75	

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 1 – PHASE COMPARATOR

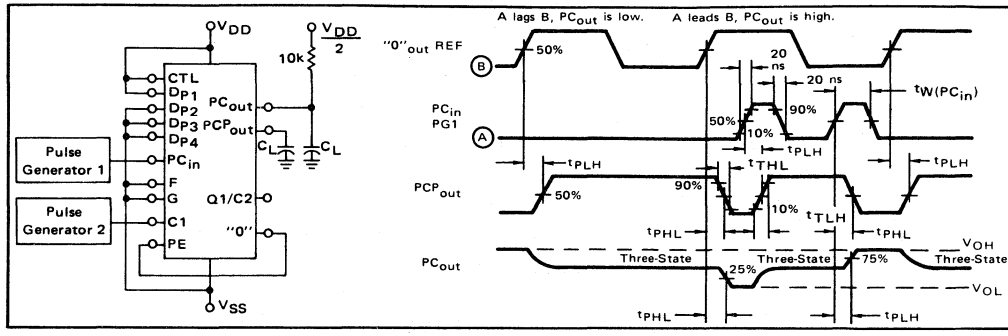


FIGURE 2 – COUNTER D1

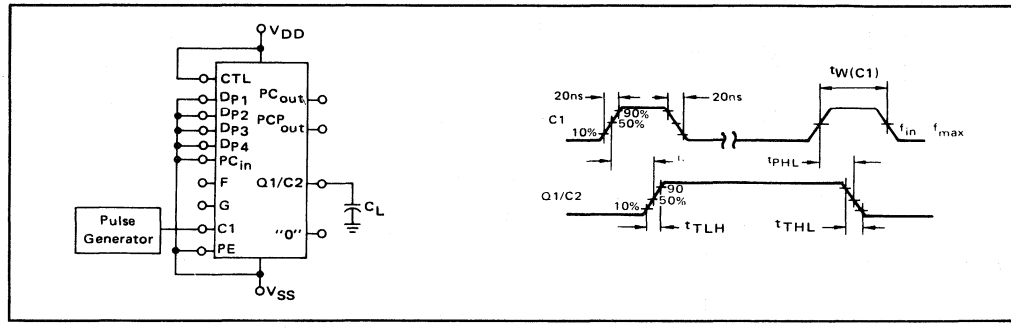
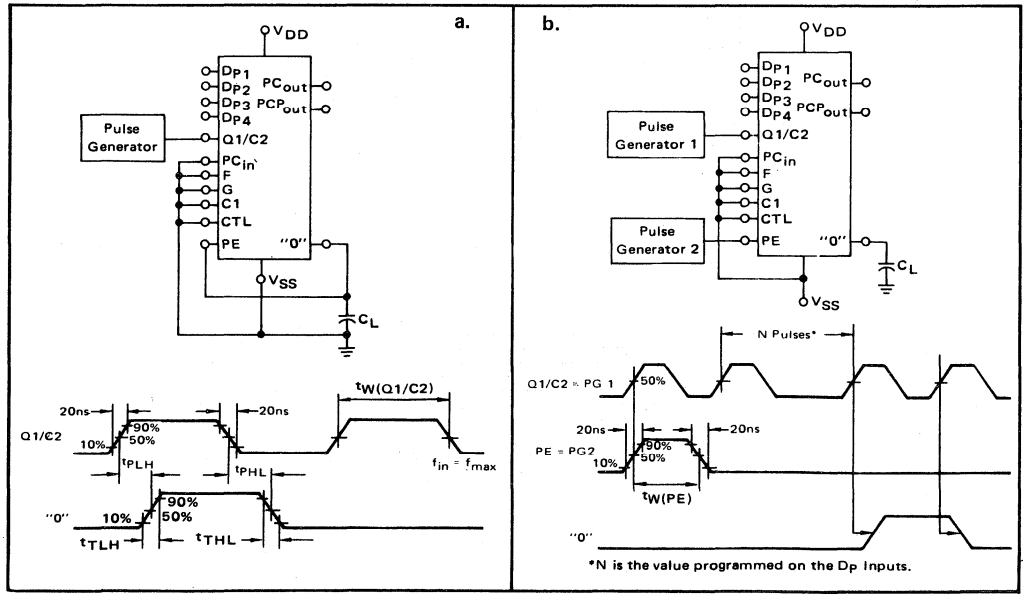
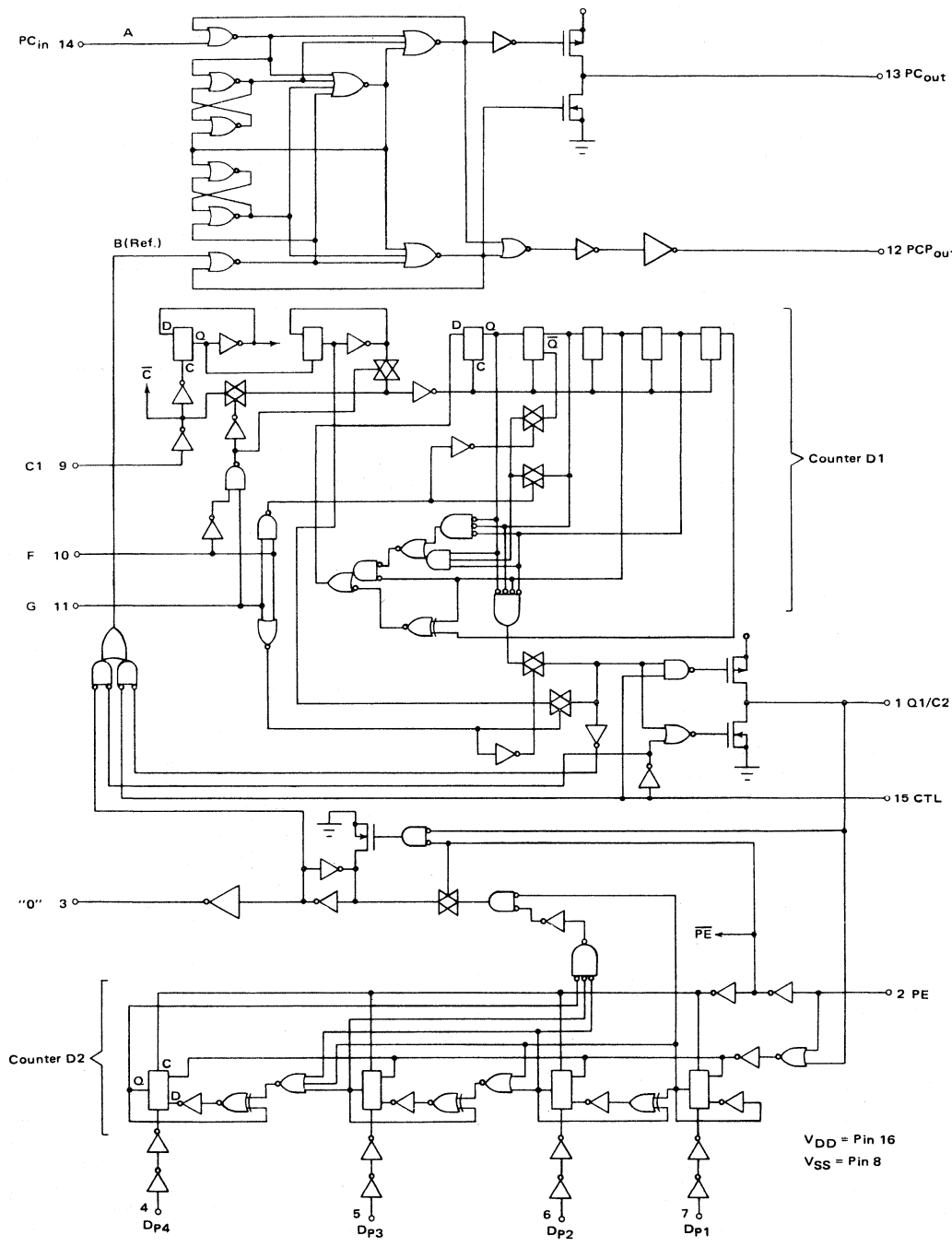


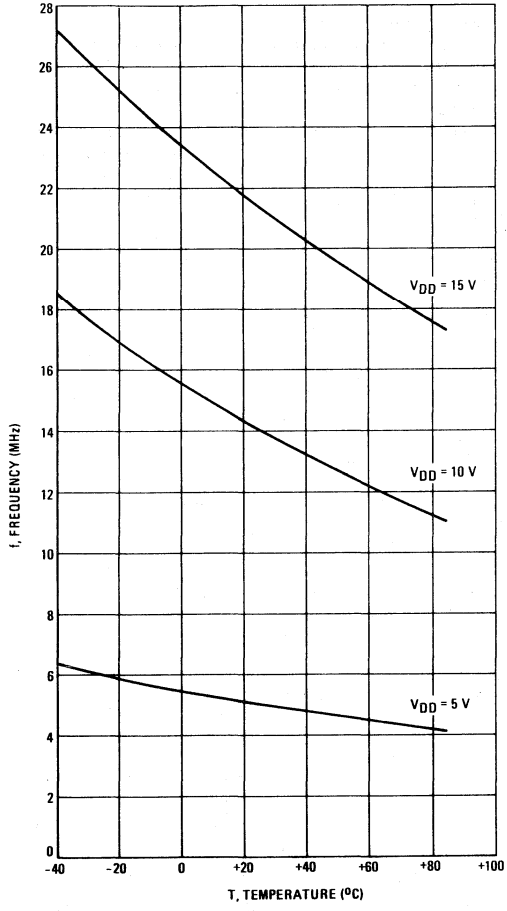
FIGURE 3 – COUNTER D2



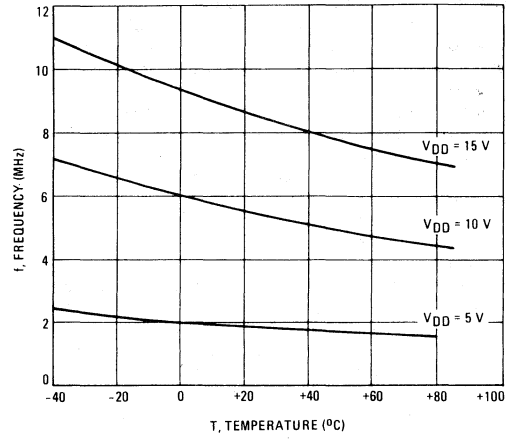
LOGIC DIAGRAM



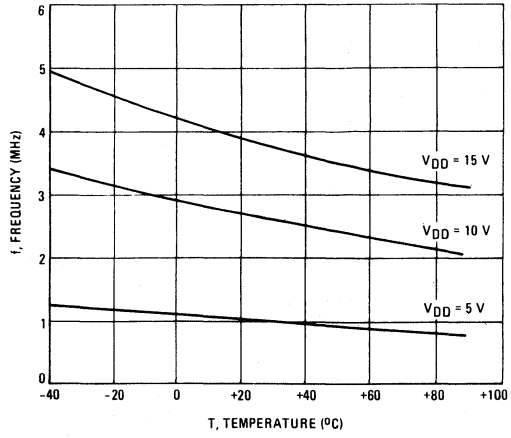
Typical Maximum Frequency Divider D1
Division ratios: 4, 64 or 100 (CL = 50 pF)



Typical Maximum Frequency Divider D1
Division ratio: 16 (CL = 50 pF)



Typical Maximum Frequency Divider D2
Division ratio: 2 (CL = 50 pF)



OPERATING CHARACTERISTICS

The MC14568B contains a phase comparator, a fixed divider (÷ 4, ÷ 16, ÷ 64, ÷ 100) and a programmable divide-by-N 4-bit counter.

PHASE COMPARATOR

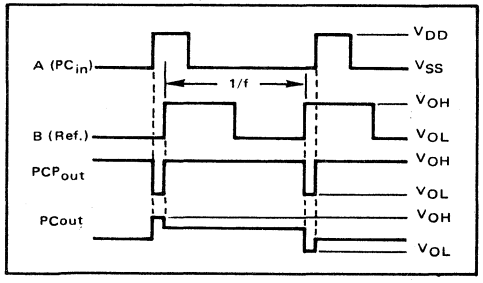
The phase comparator is a positive edge controlled logic circuit. It essentially consists of four flip-flops and an output pair of MOS transistors. Only one of its inputs (PC_{in}, pin 14) is accessible externally. The second is connected to the output of one of the two counters D1 or D2 (see block diagram).

Duty cycles of both input signals (at A and B) need not be taken into consideration since the comparator responds to leading edges only.

If both input signals have identical frequencies but different phases, with signal A (pin 14) leading signal B (Ref.), the comparator output will be high for the time equal to the phase difference.

If signal A lags signal B, the output will be low for the same time. In between, the output will be in a three-state condition and the voltage on the capacitor of an RC filter normally connected at this point will have some intermediate value (see Figure 4). When used in a phase locked loop, this value will adjust the Voltage Controlled Oscillator frequency by reducing the phase difference between the reference signal and the divided VCO frequency to zero.

FIGURE 4 – PHASE COMPARATOR WAVEFORMS



If the input signals have different frequencies, the output signal will be high when signal B has a lower frequency than signal A, and low otherwise.

Under the same conditions of frequency difference, the output will vary between V_{OH} (or V_{OL}) and some intermediate value until the frequencies of both signals are equal and their phase difference equal to zero, i.e. until locked condition is obtained.

Capture and lock range will be determined by the VCO frequency range. The comparator is provided with a lock indicator output, which will stay at logic 1 in locked conditions.

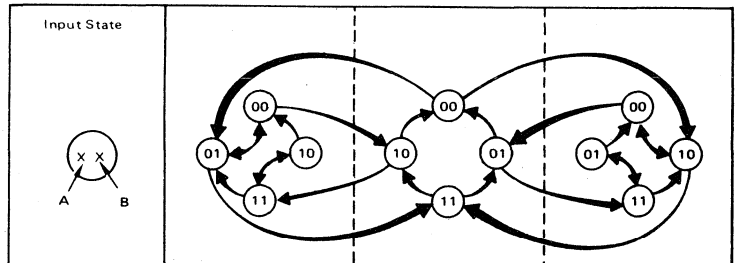
The state diagram (Figure 5) depicts the internal state transitions. It assumes that only one transition on either signal occurs at any time. It shows that a change of the output state is always associated with a positive transition of either signal. For a negative transition, the output does not change state. A positive transition may not cause the output to change; this happens when the signals have different frequencies.

DIVIDE BY 4, 16, 64 OR 100 COUNTER (D1)

This counter is able to work at an input frequency of 5 MHz for a V_{DD} value of 10 volts over the standard temperature range when dividing by 4, 64 and 100. Programming is accomplished by use of inputs F and G (pins 10 and 11) according to the truth table shown. Connecting the Control input (CTL, pin 15) to V_{DD} allows cascading this counter with the programmable divide-by-N counter provided in the same package. Independent operation is obtained when the Control input is connected to V_{SS}.

The different division ratios have been chosen to generate the reference frequences corresponding to the channel spacings normally required in frequency synthesizer applications. For example, with the division ratio 100 and a 5 MHz crystal stabilized source a reference frequency of 50 kHz is supplied to the comparator. The lower division ratios permit operation with low frequency crystals.

FIGURE 5 – PHASE COMPARATOR STATE DIAGRAM



PC_{out}	0	3-State Output Disconnected	1
PCP_{out} (Lock Indicator)	0	1	0

If used in cascade with the programmable divide-by-N counter, practically all usual reference frequencies, or channel spacings of 25, 20, 12.5, 10, 6.25 kHz, etc. are easily achievable.

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (D2)

This counter is programmable by using inputs D_{P1} . . . D_{P4} (pins 7 . . . 4). The Preset Enable input enables the parallel preset inputs D_{P1} . . . D_{P4}. The "0" output must be externally connected to the PE input for single stage applications. Since there is not a cascade feedback input, this counter, when cascaded, must be used as the most significant digit. Because of this, it can be cascaded with binary counters as well as with BCD counters (MC14569B, MC14522B, MC14526B).

TYPICAL APPLICATIONS

FIGURE 6 – CASCADING MC14568B AND MC14522B OR MC14526B WITH MC14569B

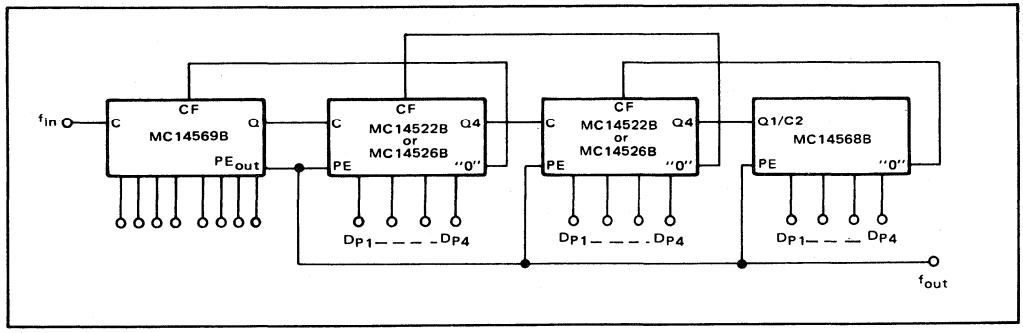


FIGURE 7 – FREQUENCY SYNTHESIZER WITH MC14568B and MC14569B USING A MIXER
(Channel Spacing 10 kHz)

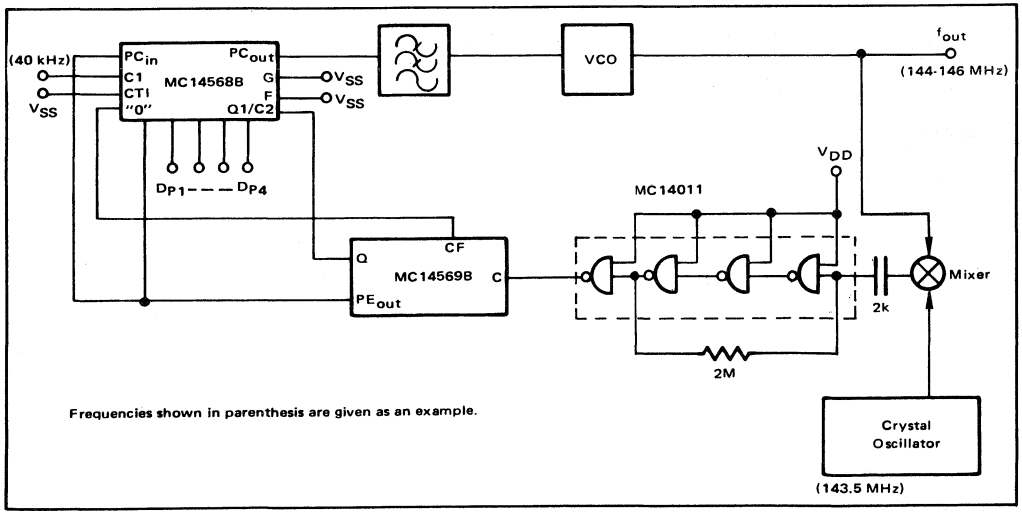
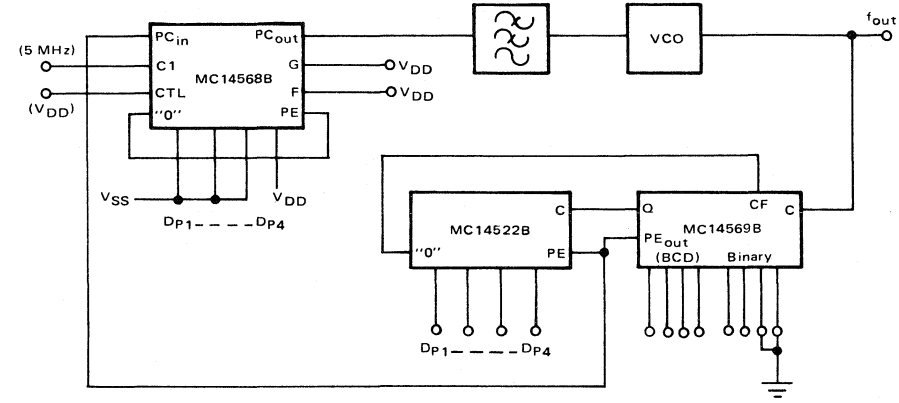


FIGURE 8 – FREQUENCY SYNTHESIZER USING MC14568B, MC14569B AND MC14522B
(Without Mixer)



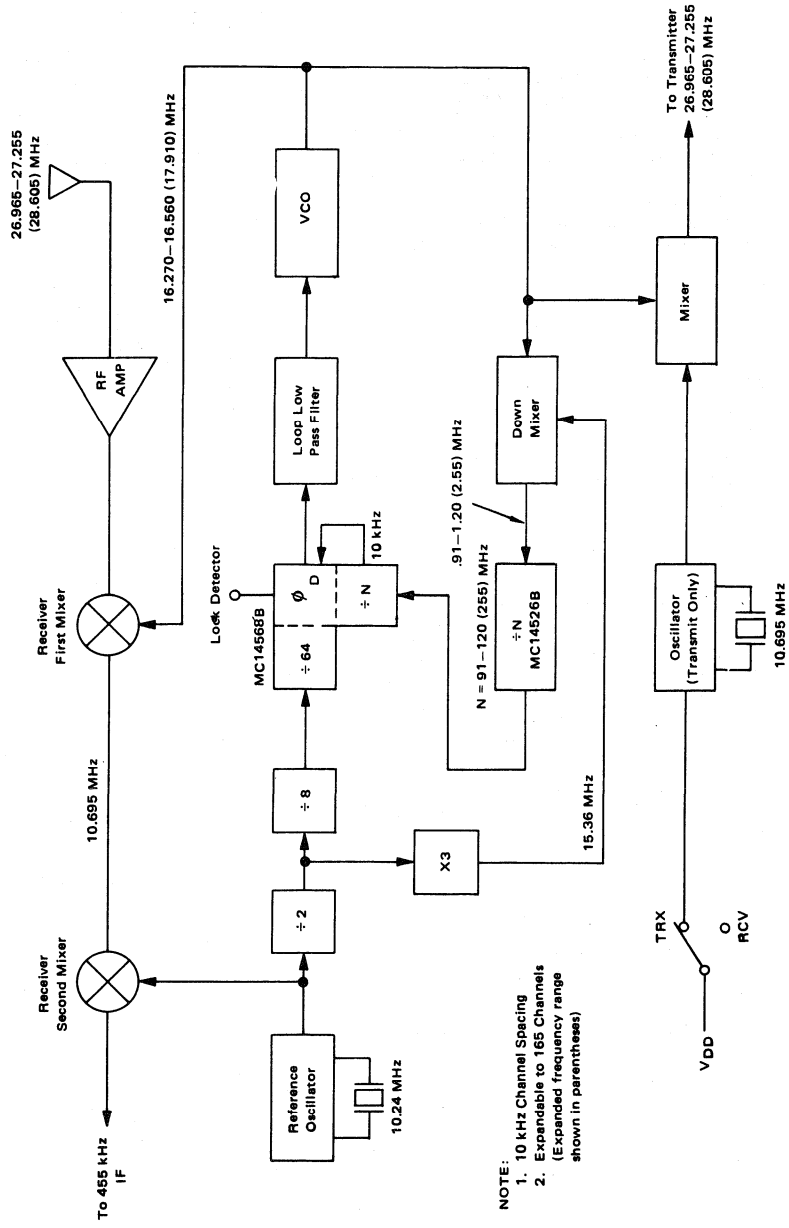
N_1	N_2	N_3
(0–5)	(0–9)	(0, 4, 8, 12)
(625 kHz steps)	(62.5 kHz steps)	(6.25 kHz steps)

Divide ratio = $160N_1 + 16N_2 + N_3$

Example:
$f_{out} = N_1$ (MHz) + N_2 (x100 kHz) + N_3 (x25 kHz)
Frequency range = 5 MHz
Channel spacing = 25 kHz
Reference frequency = 6.25 kHz

Figures shown in parenthesis refer to example.

FIGURE 9 – TYPICAL 23-CHANNEL CB FREQUENCY SYNTHESIZER FOR DOUBLE CONVERSION TRANSCEIVERS



MOTOROLA

MC14569B

HIGH SPEED PROGRAMMABLE DIVIDE-BY-N DUAL 4-BIT BCD/BINARY COUNTER

The MC14569B is a high speed programmable divide-by-N dual 4-bit BCD or binary down counter constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a single monolithic structure.

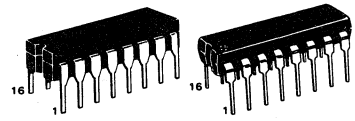
It has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- 9.5 MHz Typical Counting Rate at 10 V for Any Division Ratio Greater Than 1
- Speed-up Circuitry for Zero Detection and Preset Enable
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Quiescent Current = 5 nA typ/pkg @ 5 Vdc
- Can be Cascaded With MC14568B, MC14522B and MC14526B for Frequency Synthesizer Applications

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

HIGH SPEED PROGRAMMABLE DIVIDE-BY-N DUAL 4-BIT BCD/BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

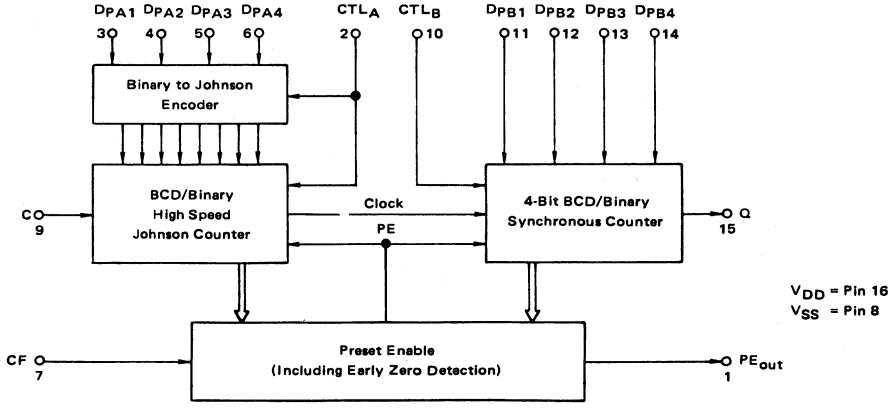
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM

CTL = "0" for Binary Count
CTL = "1" for BCD Count



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-0.88	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.005	50	–	150	μAdc
(Per Package)		10	–	100	–	0.010	100	–	300	
		15	–	200	–	0.015	200	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	(0.58 μA/kHz) f + I_{DD}							μAdc
		10	(1.20 μA/kHz) f + I_{DD}							
		15	(1.95 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_{TLH}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Turn-On Delay Time	t_{PLH}					ns
PE_{out}		5.0	–	420	700	
		10	–	175	300	
		15	–	125	250	
Q Output		5.0	–	675	1200	ns
		10	–	285	500	
		15	–	200	400	
Turn-Off Delay Time	t_{PHL}					ns
PE_{out}		5.0	–	380	600	
		10	–	150	300	
		15	–	100	200	
Q Output		5.0	–	530	1000	ns
		10	–	225	400	
		15	–	155	300	
Clock Pulse Width	t_{WH}	5.0	300	100	–	ns
		10	150	45	–	
		15	115	30	–	
Clock Pulse Frequency #	f_{cl}	5.0	–	3.5	2.1	MHz
		10	–	9.5	5.7	
		15	–	13.0	7.8	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	NO LIMIT			μs
		10				
		15				

#This inplies that zero detection and preset enable is done while the clock is running at the specified frequency.

SWITCHING WAVEFORMS

FIGURE 1

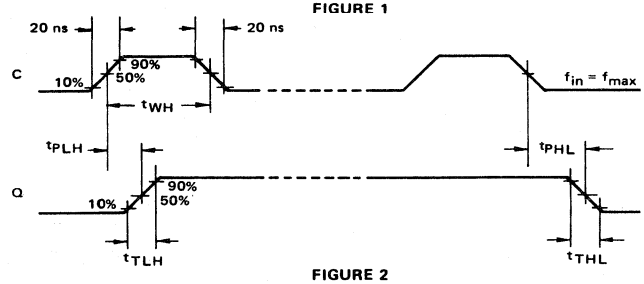
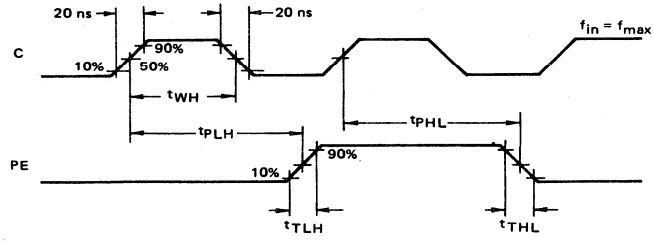


FIGURE 2



OPERATING CHARACTERISTICS

The MC14569B includes a high speed Johnson counter followed by a BCD/binary 4-bit synchronous counter (see block diagram). The use of an encoder allows the Johnson counter to be programmed (i.e. preset) in BCD or binary code through inputs D_{PA1}, D_{PA2}, D_{PA3}, and D_{PA4}.

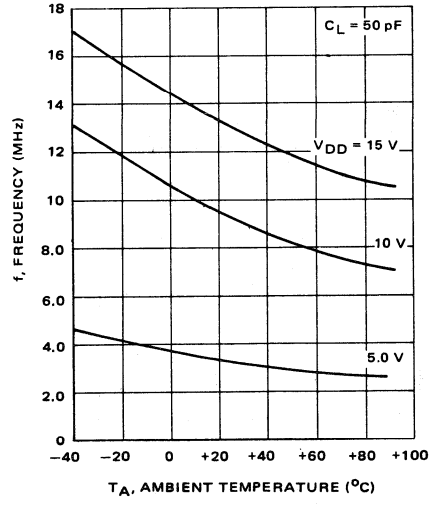
The BCD/binary counter can be programmed through inputs D_{PB1}, D_{PB2}, D_{PB3}, and D_{PB4}. For each counter a divide ratio of 10 (BCD count) or 16 (binary count) can be chosen independently by inputs CTL_A and CTL_B respectively. When one of those inputs is set high, the divide ratio of the corresponding counter is 10 (BCD); when it is set low, the division ratio is 16 (binary).

A Cascade Feedback input (pin 7), a Q output (pin 15) and a Preset Enable output (pin 1) made it possible to cascade the MC14568B, MC14522B and MC14526B with this device. CF, Q and PE_{out} of MC14569B must be respectively connected to "0", C and PE of the following counter.

When MC14569B is used alone, CF must be connected to V_{DD}. One pulse will appear on output PE_{out} every N clock periods (N being the value programmed on the Dp inputs). Both counters included in MC14569B, and eventually all the counters which are cascaded, should normally be preset at the programmed values during the clock period where they all reach the count zero. For best speed performance, preset is started as soon as count 1 is detected. As a consequence, it is not possible to program a frequency division ratio of one. However, it is possible to program a division ratio of 11 (i.e. D_{PA1}, . . . D_{PA4} = 1,0,0,0 and D_{PB1}, . . . D_{PB4} = 1,0,0,0), or a division ratio of 101 if another counter is cascaded with the MC14569B.

This high speed configuration makes it possible to guarantee a maximum clock pulse frequency of 5.7 MHz for a 10 V V_{DD} supply for any division ratio greater than one. Due to the presence of the early zero detection, the circuit must be used in the two least significant digit positions.

Because all the circuitry is static, there is no minimum frequency specification for the Clock input, C (pin 9).



MOTOROLA

MC14572UB

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

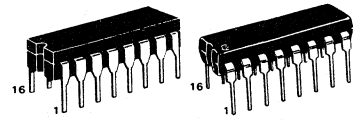
HEX GATE

4 INVERTERS PLUS
2-INPUT NOR GATE PLUS
2-INPUT NAND GATE

HEX GATE

The MC14572UB hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Input Impedance = 10^{12} ohms typical
- NOR Input Pin Adjacent to V_{SS} Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to V_{DD} Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

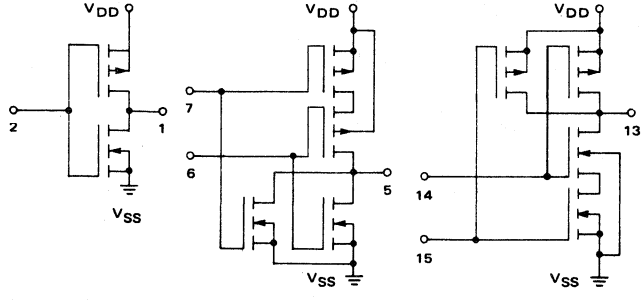
ORDERING INFORMATION

MC14XXXUB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

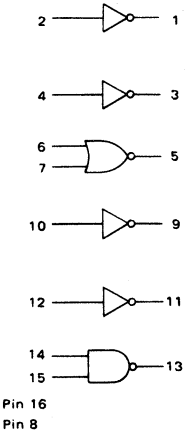
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.4	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.6	
"1" Level	V_{IH}									
(V_O = 1.4 or 3.6 Vdc)		5.0	3.6	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.1	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.89 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.80 µA/kHz) f + I_{DD}							
		15	I_T = (5.68 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50)\ V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

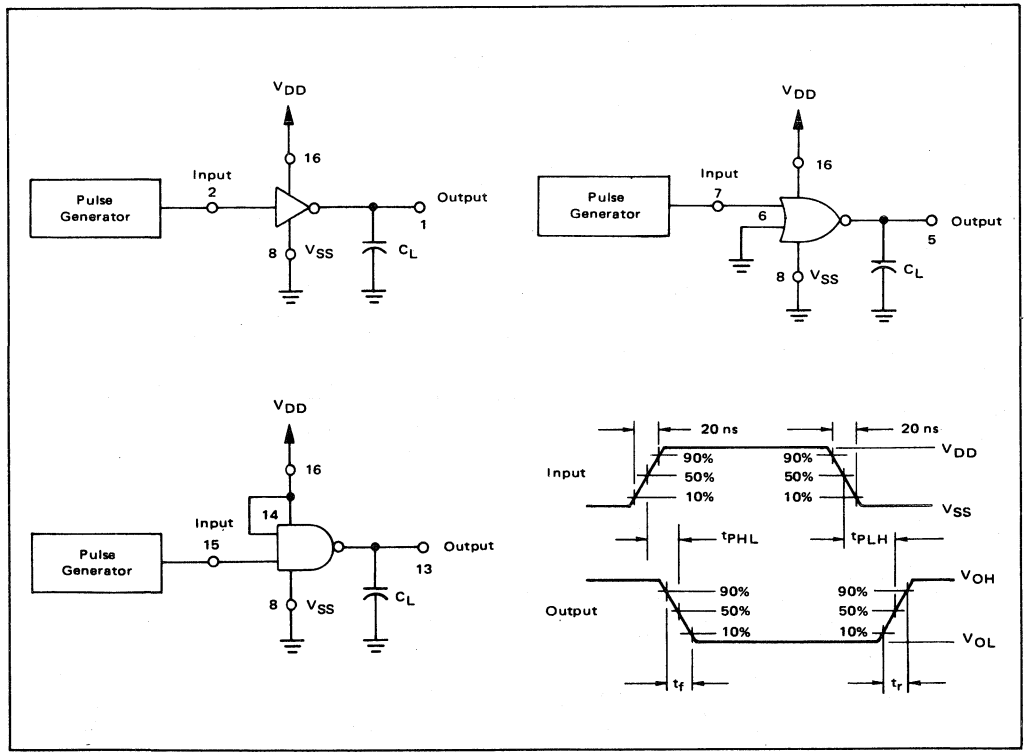
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns		5.0	–	115	200	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	–	55	110	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 15 ns		15	–	40	85	

*The formula given is for the typical characteristics only.

FIGURE 1 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



MOTOROLA

MC14573
MC14574
MC14575

ADVANCE INFORMATION

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER
QUAD PROGRAMMABLE COMPARATOR
DUAL/DUAL PROGRAMMABLE AMPLIFIER-COMPARATOR

The MC14573, MC14574, and MC14575 are a family of quad operational low power amplifiers and comparators using the complementary P-channel and N-channel enhancement MOS devices in a single monolithic structure. The operating current is externally programmed with a resistor to provide a choice in the tradeoff of power dissipation and slew rates. The operational amplifiers are internally compensated.

These low cost units are excellent building blocks in consumer, industrial, automotive and instrument applications. Active filters, voltage reference, function generators, oscillators, limit set alarms, TTL to CMOS or CMOS to CMOS up converters, A to D converters and zero crossing detectors are some applications. These units are useful in both battery operated and line operated systems.

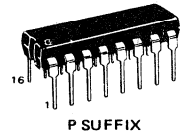
- Low Cost Quads
- Power Supply—Single 3.0 to 15 Vdc
  Dual ±1.5 to ±7.5 Vdc
- Wide Input Voltage Range
- Common Mode Range 0.0 to V_{CC} – 2.0 Vdc for Single Supply
- Externally Programmable with One or Two Resistors
- Two Offset Ranges—10 mV max and 50 mV max
- Internally Compensated Operational Amplifiers
- High Input Impedance
- Comparators—JEDEC B-Series Compatible
- CMOS and TTL Compatible

CMOS MSI

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER
QUAD PROGRAMMABLE COMPARATOR
DUAL/DUAL PROGRAMMABLE OPERATIONAL AMPLIFIER-COMPARATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXX* — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

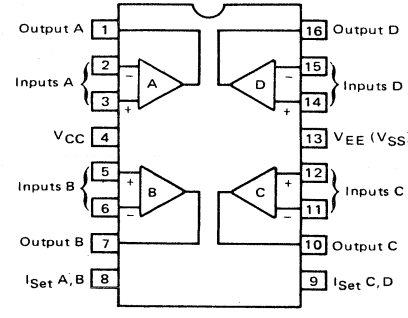
*Add a -1 to part number when ordering parts selected to a maximum of 10 mV offset voltage

PIN ASSIGNMENT

MC14573/MC14573-1
Quad Op Amplifier

MC14574/MC14574-1
Quad Comparator

MC14575/MC14575-1
Dual Op Amplifier (Segments A & B) plus
Dual Comparator (Segments C & D)



MAXIMUM RATINGS (Voltages referenced to V_{EE})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{CC} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING RANGE

DC Supply Voltage	V_{CC} to V_{EE}	+3.0 to +15 Vdc

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{CC} or V_{EE}.

OPERATIONAL AMPLIFIER

ELECTRICAL CHARACTERISTICS (V_{EE} = 0 V, T_A = 25°C)

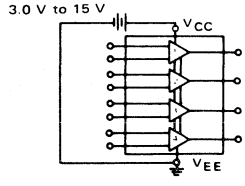
Characteristic	Symbol	V_{CC} Vdc	Min	All Types Typ	Max	Unit
Input Common Mode Voltage Range (I_{Set} = 200 μA)	V_{ICR}	 5.0 10 15	 0 0 0	 – – –	 3.0 8.0 13	Vdc
Output Voltage Range (I_{Set} = 50 μA) (R_L = 100 k connected to V_{EE})	V_{OR}	 5.0 10 15	 1.05 1.05 1.05	 – – –	 4.0 9.0 14	Vdc
Input Offset Voltage (I_{Set} = 50 μA) MC14573, MC14575 MC14573-1, MC14575-1	V_{IO}	 10 10	 – –	 ±10 ±5.0	 ±50 ±10	mVdc
Average Temperature Coefficient of Input Offset Voltage	–	–	–	20	–	μV/°C
Input Bias Current	I_{IB}	10	–	–	1.0	nA
Input Offset Current	I_{IO}	10	–	–	200	pA
Open Loop Voltage Gain (I_{Set} = 50 μA)	A_{VOL}	10	–	90	–	dB
Power Supply Rejection Ratio	PSRR	10	–	70	–	dB
Common Mode Rejection Ratio	CMRR	10	–	80	–	dB
Channel Separation	–	10	–	-100	–	dB
Slew Rate (I_{Set} = 40 μA)	SR	10	–	2.5	–	V/μs
Phase Margin	ϕm	10	–	45	–	Degrees
Supply Current, Per pair MC14573, MC14575 (R_{Set} = 1 MΩ)	I_{CC}	 5 10 15	 – – –	 50 100 150	 – – –	μA
Supply Current, Per pair MC14574, MC14575 (R_{Set} = 100 k)	I_{CC}	5 10 15	– – –	0.5 1.2 1.8	– – –	mA

COMPARATOR

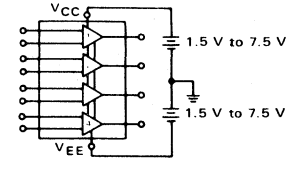
ELECTRICAL CHARACTERISTICS (V_{EE} = 0 Vdc, T_A = 25°C)

Characteristic	Symbol	V_{CC} Vdc	Min	Typ	Max	Unit
Input Common Mode Voltage Range (I_{Set} = 200 μA)	V_{ICR}	5.0	0	–	3.0	Vdc
		10	0	–	8.0	
		15	0	–	13	
Output Voltage "0" Level	V_{OL}	5.0	–	0	0.05	Vdc
		10	–	0	0.05	
		15	–	0	0.05	
"1" Level	V_{OH}	5.0	4.95	5.0	–	Vdc
		10	9.99	10	–	
		15	14.95	15	–	
Output Drive Current (AL Device)	I_{OH}					mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.4	-4.2	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.51	-0.88	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	-2.25	–	
(V_{OH} = 13.5 Vdc)		15	-3.4	8.8	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.25	2.25	–	mAdc
(V_{OL} = 0.5 Vdc)		10	3.25	5.6	–	
(V_{OL} = 1.5 Vdc)		15	8.5	20	–	
Output Drive Current (CL/CP Device)	I_{OH}					mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.1	-4.2	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.44	-0.88	–	
(V_{OH} = 9.5 Vdc)		10	-1.1	-2.25	–	
(V_{OH} = 13.5 Vdc)		15	-3.0	-8.8	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.2	2.25	–	mAdc
(V_{OL} = 0.5 Vdc)		10	2.6	5.6	–	
(V_{OL} = 1.5 Vdc)		15	7.5	20	–	
Input Offset Voltage (I_{Set} = 50 μA) MC14574, MC14575	V_{IO}	10	–	–	50	±mVdc
MC14574-1, MC14575-1		10	–	–	10	
Average Temperature Coefficient of Input Offset Voltage	–	–	–	20	–	μV/°C
Input Bias Current	I_{IB}	10	–	–	1.0	nA
Input Offset Current	I_{IO}	10	–	–	200	pA
Open Loop Voltage Gain (I_{Set} = 50 μA)	A_{VOL}	10	–	96	–	dB
Power Supply Rejection Ratio	PSRR	10	–	70	–	dB
Common Mode Rejection Ratio	CMRR	10	–	80	–	dB
Channel Separation	–	10	–	-100	–	dB
Output Rise and Fall Time (C_L = 50 pF)	t_{TLH}, t_{THL}	10	–	100	–	ns
Propagation Delay Time, 5 mV Overdrive (I_{Set} = 50 μA, C_L = 50 pF)	t_d	10	–	1000	–	ns
Supply Current – Per pair MC14574, MC14575 (R_{Set} = 1 MΩ)	I_{CC}	5	–	50	–	μA
		10	–	100	–	
		15	–	150	–	
Supply Current – Per pair MC14574, MC14575 (R_{Set} = 100 k)	I_{CC}	5	–	0.45	–	mA
		10	–	1.0	–	
		15	–	1.5	–	

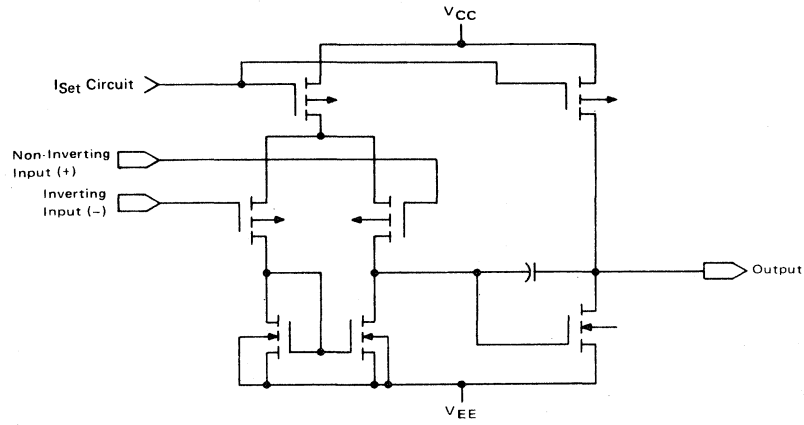
SINGLE SUPPLY



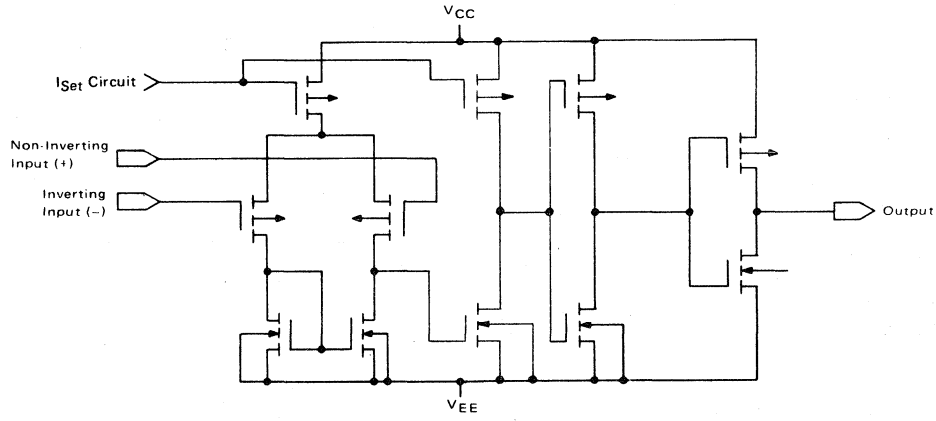
SPLIT SUPPLIES



CIRCUIT DIAGRAM OPERATIONAL AMPLIFIER 1/4th CIRCUIT



CIRCUIT DIAGRAM COMPARATOR 1/4th CIRCUIT



The programming current I_{Set} is fixed by an external resistor R_{Set} connected between V_{EE} and either one or both of the I_{Set} pins (8 and 9). When two external programming resistors are used, the set currents for each op amp pair or comparator are given by:

$$I_{Set}(\mu A) \approx \frac{V_{CC} - V_{EE} - 1}{R_{Set}(M\Omega)}$$

Pins 8 and 9 may be tied together for use with a single programming resistor. The set currents for each op amp pair or comparator pair are then given by:

$$I_{Set\,A,B} = I_{Set\,C,D}(\mu A) \approx \frac{V_{CC} - V_{EE} - 1}{2\,R_{Set}(M\Omega)}$$

If a pair of op amps or comparators are not used, the I_{Set} pin for that pair may be tied to V_{CC} for minimum power consumption.

It should be noted that increasing I_{Set} for comparators will decrease propagation delay for that comparator.

For operational amplifiers, the maximum obtainable output voltage (V_{OH}) for a given load resistor connected to V_{EE} is given by:

$$V_{OH} = (4 \times 10^{-3}\, I_{Set})R_L - 0.05\ v,\ R_L \text{ in } k\Omega$$

$$\text{if } (4 \times 10^{-3}\, I_{Set})R_L < V_{DD},\ I_{Set} \text{ in } \mu A$$

Typical op amp slew rates are given by:

$$S_R \approx 0.05\, I_{Set}\ (V/\mu s),\ I_{Set} \text{ in } \mu A$$

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MOTOROLA

MC14580B

4 x 4 MULTIPORT REGISTER

The MC14580B is a 4 by 4 multiport register useful in small scratch pad memories, arithmetic operations when coupled with an adder, and other data storage applications. It allows independent reading of any two words (or the same word at both outputs) while writing into any one of four words.

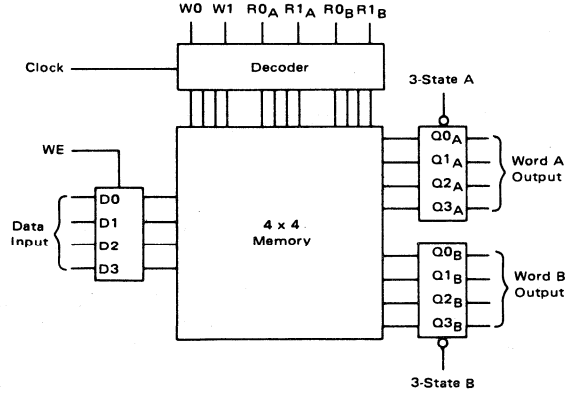
Address changing and data entry occur on the rising edge of the clock. When the write enable input is low, the contents of any word may be accessed but not altered.

- Logic Swing Independent of Fanout
- No Restrictions on Clock Input Rise or Fall Times
- 3-State Outputs
- Single Phase Clocking
- Quiescent Current = 10 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

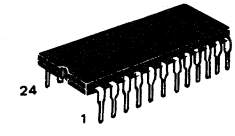
BLOCK DIAGRAM



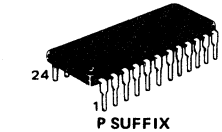
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

4 x 4 MULTIPORT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 623

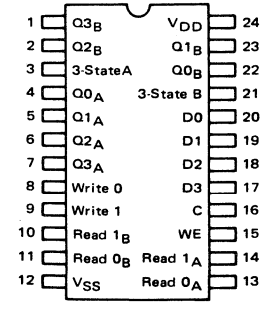


P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



V_{DD} = Pin 24
V_{SS} = Pin 12

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	μAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.18 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.91 μA/kHz) f + I_{DD}							
		15	I_T = (2.67 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

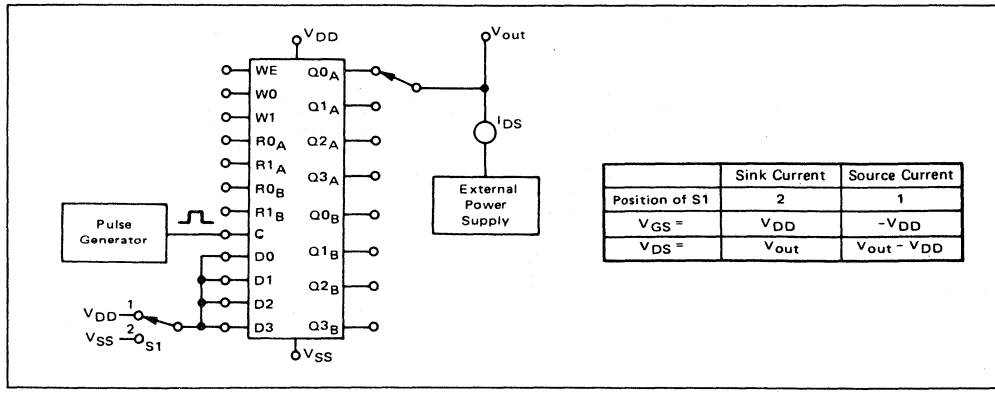
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time, Clock to Output	t_{PLH},					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 1415 ns	t_{PHL}	5.0	–	1500	4500	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 467 ns		10	–	500	1500	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 325 ns		15	–	350	1125	
Write Enable Setup Time	$t_{su(WE)}$	5.0	–	800	2000	ns
		10	–	300	750	
		15	–	180	550	
Write Enable Setup Time	$t_{su(WE)}$	5.0	–	-300	+150	ns
		10	–	-100	+75	
		15	–	-60	+55	
Write Enable Hold Time	$t_{h(WE)}$	5.0	–	-800	-200	ns
		10	–	-300	-75	
		15	–	-180	-45	
Address and Data Setup Time	$t_{su(D)}$,	5.0	–	150	450	ns
	$t_{su(W)}$	10	–	70	210	
		15	–	50	160	
Address and Data Hold Time	$t_{h(D)}$,	5.0	–	160	480	ns
	$t_{h(W)}$	10	–	65	195	
		15	–	50	150	
3-State Enable/Disable Delay Time**	t_{PHZ}, t_{PLZ},	5.0	–	355	900	ns
	t_{PZH}, t_{PZL}	10	–	140	350	
		15	–	85	250	
Positive Clock Pulse Width (minimum)	t_{WH}	5.0	–	1000	3000	ns
		10	–	350	1050	
		15	–	200	800	
Negative Clock Pulse Width (minimum)	t_{WL}	5.0	–	400	1200	ns
		10	–	85	255	
		15	–	60	200	

*The formula given is for the typical characteristics only.

**Measured at the point of 10% change at output when the output load is 1.0 Ω and 50 pF.

FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



	Sink Current	Source Current
Position of S1	2	1
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS (3-State Inputs are High)

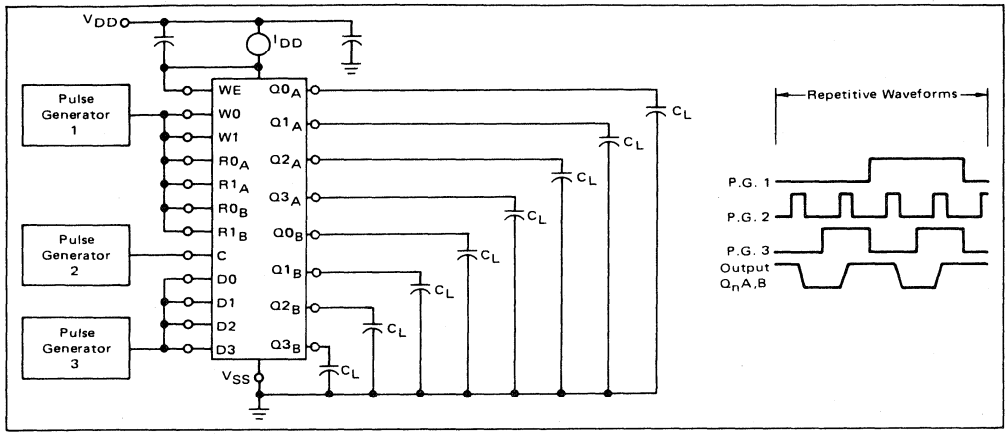
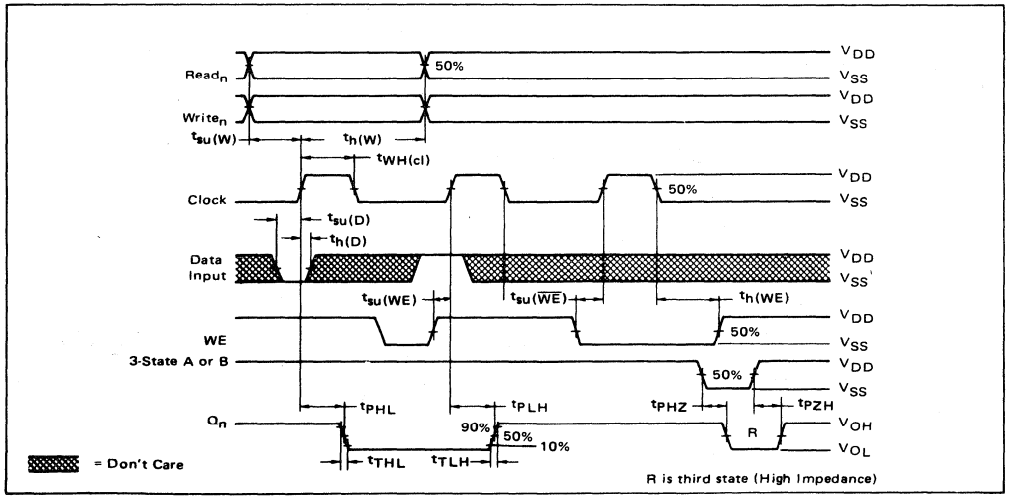
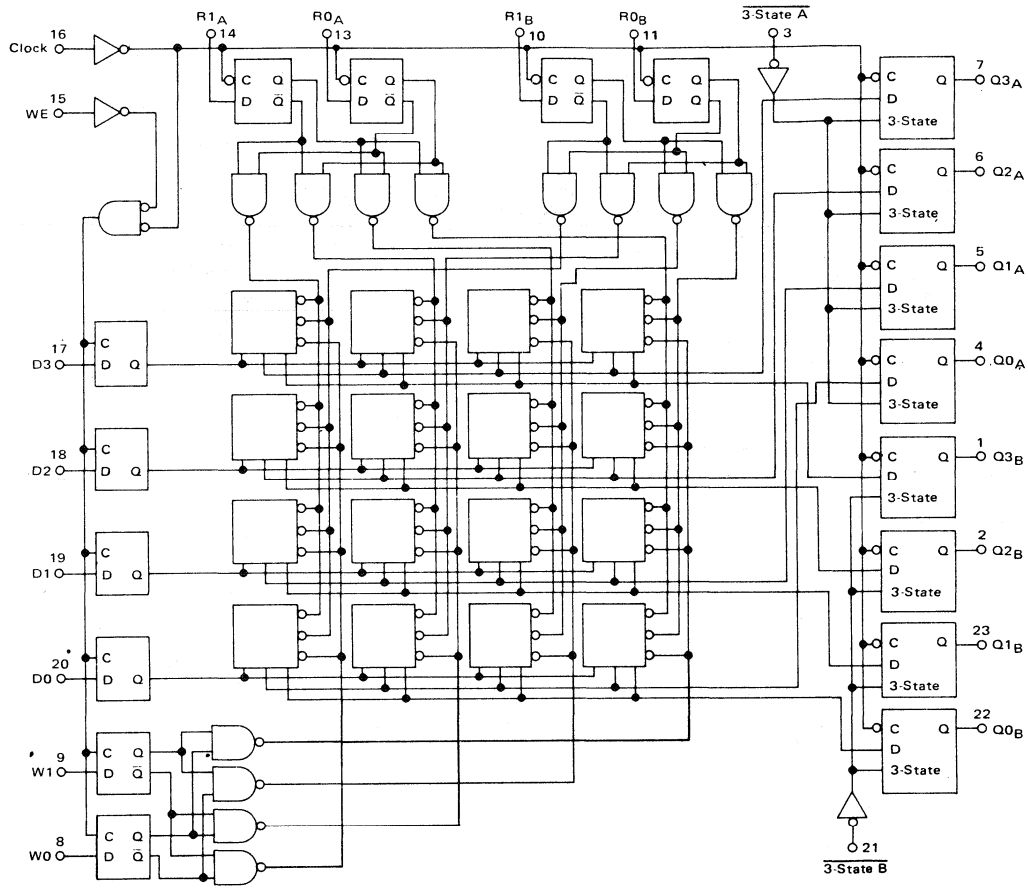


FIGURE 3 – AC WAVEFORMS AND DEFINITIONS



LOGIC DIAGRAM



TRUTH TABLE

Clock	WE	Write 1	Write 0	Read 1_A	Read 0_A	Read 1_B	Read 0_B	3-State A	3-State B	D_n	Q_nA	Q_nB
⎍	1	S1	S2	S1	S2	S1	S2	1	1	1	1	1
⎍	1	S1	S2	S1	S2	S1	S2	1	1	0	0	0
⎍	X	X	X	X	X	X	X	1	1	X	No Change	No Change
X	X	X	X	X	X	X	X	0	0	X	R	R
0	X	X	X	X	X	X	X	1	1	X	No Change	No Change
1	X	X	X	X	X	X	X	1	1	X	No Change	No Change
⎍	1	0	0	0	1	1	0	1	1	D_n to word 0	Contents of word 1 displayed	Contents of word 2 displayed
⎍	0	0	0	0	1	1	0	1	1	Word 0 not altered	Contents of word 1 displayed	Contents of word 2 displayed

S1 and S2 refer to input states of either "1" or "0".
R implies high resistance ~ 10^9 ohms .
X = Don't care

MOTOROLA

MC14581B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT ARITHMETIC LOGIC UNIT

4-BIT ARITHMETIC LOGIC UNIT

The MC14581B is a CMOS 4-bit ALU logic unit capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 4-bit words. The level of the mode control input determines whether the output funciton is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the select inputs (S0 thru S3) with the mode control input high, while the desired arithmetic operation is selected by applying a low voltage to the mode control input, the required level to carry in, and the appropriate word to the select inputs. The word inputs and function outputs can be operated with either active high or active low data.

Carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the MC14582B as a second order look ahead block. An inverted ripple carry input (C_n) and a ripple carry output (C_{n+4}) are included for ripple through operation.

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the $\overline{A}$ and $\overline{B}$ inputs is provided using the A = B output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the C_{n+4} output can be used to indicate relative magnitude as shown in this table:

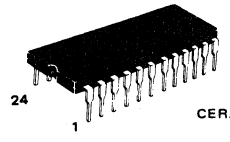
Data Level	C_n	C_{n+4}	Magnitude
Active High	H	H	$A \leq B$
	L	H	$A < B$
	H	L	$A > B$
	L	L	$A \geq B$
Active Low	L	L	$A \leq B$
	H	L	$A < B$
	L	H	$A > B$
	H	H	$A \geq B$

FEATURES:

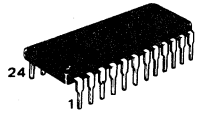
- Functional and Pinout Equivalent to 74181.
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- High Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Low Input Capacitance — 5.0 pF typical
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Load, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



L SUFFIX
CERAMIC PACKAGE
CASE 623

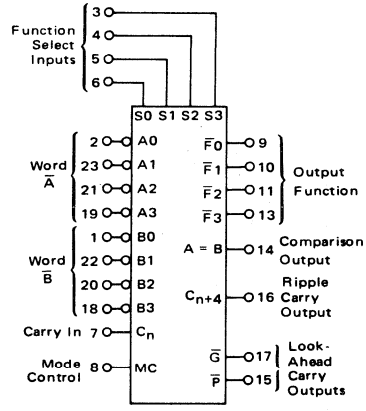


P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	**0.005**	5.0	–	150	μAdc
(Per Package)		10	–	10	–	**0.010**	10	–	300	
		15	–	20	–	**0.015**	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	**0.005**	20	–	150	μAdc
(Per Package)		10	–	40	–	**0.010**	40	–	300	
		15	–	80	–	**0.015**	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.8 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.7 μA/kHz) f + I_{DD}							
		15	I_T = (5.5 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 8 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Sum in to Sum Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 620 ns		5.0	–	705	1410	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	–	250	500	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	180	360	
Sum in to Sum Out (Logic Mode)	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 520 ns		5.0	–	605	1210	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 182 ns		10	–	215	430	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	180	360	
Sum in to A = B	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 870 ns		5.0	–	955	1910	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 297 ns		10	–	330	660	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 220 ns		15	–	245	490	
Sum In to P or G	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 400 ns		5.0	–	485	970	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	–	130	260	
Sum In to C_{n+4}	t_{PLH}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 530 ns		5.0	–	615	1230	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 187 ns		10	–	220	440	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	–	160	360	
Carry In to Sum Out	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	–	380	760	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 112 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 80 ns		15	–	105	210	
Carry in to C_{n+4}	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 220 ns		5.0	–	305	610	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns		10	–	120	240	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	–	85	170	

*The formula given is for the typical characteristics only.

AC TEST SETUP REFERENCE TABLE

TEST	AC PATHS		DC DATA INPUTS		MODE	FIG. 3 WAVEFORM
	INPUTS	OUTPUTS	TO V_{SS}	TO V_{DD}		
Sum_{in} to Sum_{out} Delay Time	$\overline{A}0$	Any $\overline{F}$	Remaining $\overline{A}$'s C_n	All $\overline{B}$'s	Add	#1
Sum_{in} to $\overline{P}$ Delay Time	$\overline{A}0$	$\overline{P}$	Remaining $\overline{A}$'s C_n	All $\overline{B}$'s	Add	#1
Sum_{in} to $\overline{G}$ Delay Time	$\overline{B}0$	C_{n+y}	All $\overline{A}$'s C_n	Remaining $\overline{B}$'s	Add	#1
Sum_{in} to C_{n+4} Delay Time	$\overline{B}0$	$\overline{G}$	All $\overline{A}$'s C_n	Remaining $\overline{B}$'s	Add	#2
C_n to Sum_{out} Delay Time	C_n	Any $\overline{F}$	All $\overline{A}$'s	All $\overline{B}$'s	Add	#1
C_n to C_{n+4} Delay Time	C_n	C_{n+4}	All $\overline{A}$'s	All $\overline{B}$'s	Add	#1
Sum_{in} to A = B Delay Time	$\overline{A}0$	A = B	All $\overline{B}$'s Remaining $\overline{A}$'s	C_n	Sub	#2
Sum_{in} to Sum_{out} Delay Time (Logic Mode)	All $\overline{B}$'s	Any $\overline{F}$	All A's	M	Exclusive OR	#2

FIGURE 1 – TYPICAL SOURCE CURRENT TEST CIRCUIT

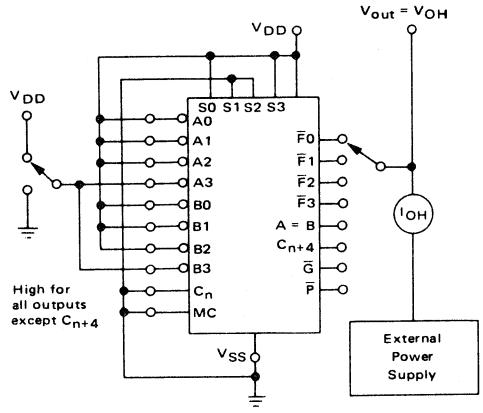


FIGURE 2 – TYPICAL SINK CURRENT TEST CIRCUIT

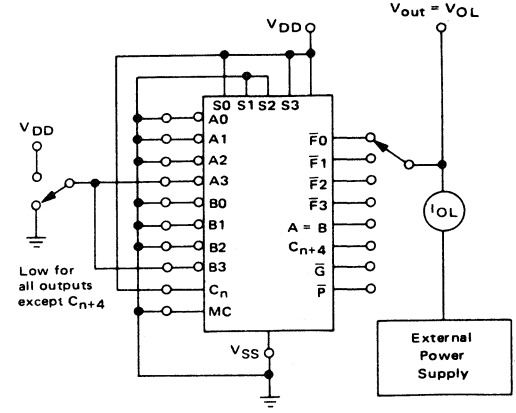


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

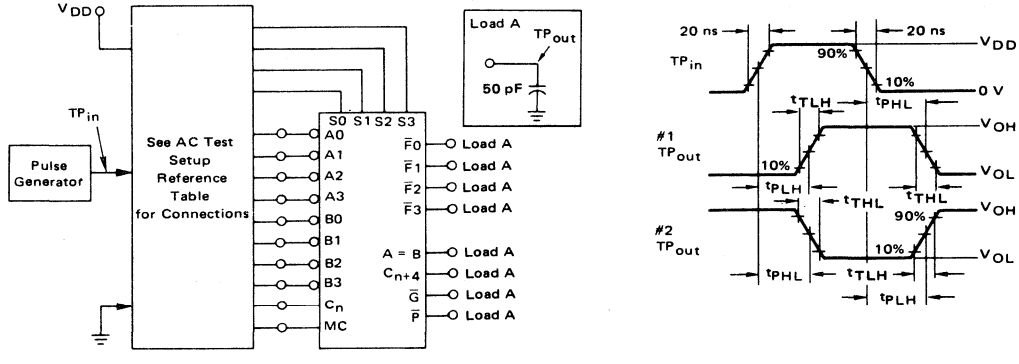
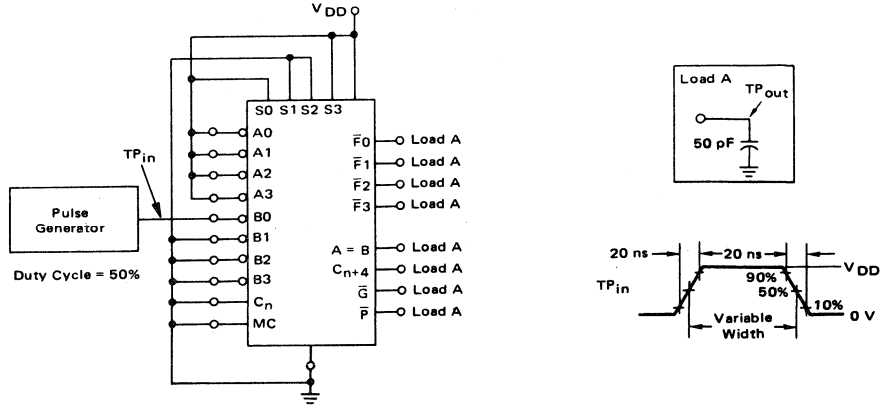
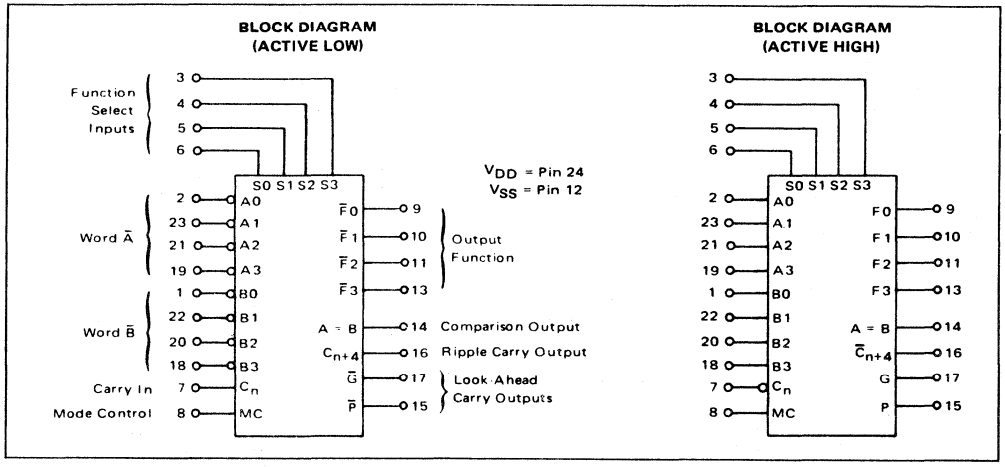


FIGURE 4 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM





TRUTH TABLE

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW		INPUTS/OUTPUTS ACTIVE HIGH	
S3	S2	S1	S0	LOGIC FUNCTION (MC = H)	ARITHMETIC* FUNCTION (MC = L, C_n = L)	LOGIC FUNCTION (MC = H)	ARITHMETIC* FUNCTION (MC = L, $\bar{C}_n$ = H)
L	L	L	L	$\bar{A}$	A minus 1	$\bar{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A+B
L	L	H	L	$\bar{A}+B$	$A\bar{B}$ minus 1	$\bar{A}B$	$A+\bar{B}$
L	L	H	H	Logic "1"	minus 1	Logic "0"	minus 1
L	H	L	L	$\overline{A+B}$	A plus $(A+\bar{B})$	$\overline{AB}$	A plus $A\bar{B}$
L	H	L	H	$\bar{B}$	AB plus $(A+\bar{B})$	$\bar{B}$	$(A+B)$ plus $A\bar{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A+\bar{B}$	$A+\bar{B}$	$A\bar{B}$	$A\bar{B}$ minus 1
H	L	L	L	$\bar{A}B$	A plus $(A+B)$	$\overline{A+B}$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\bar{B}$ plus $(A+B)$	B	$(A+\bar{B})$ plus AB
H	L	H	H	A+B	A+B	AB	AB minus 1
H	H	L	L	Logic "0"	A plus A	Logic "1"	A plus A
H	H	L	H	$A\bar{B}$	AB plus A	$A+\bar{B}$	$(A+B)$ plus A
H	H	H	L	AB	$A\bar{B}$ plus A	A+B	$(A+\bar{B})$ plus A
H	H	H	H	A	A	A	A minus 1

* Expressed as two's complements. For arithmetic function with C_n in the opposite state, the resulting function is as shown plus 1.

MOTOROLA

MC14582B

LOOK-AHEAD CARRY BLOCK

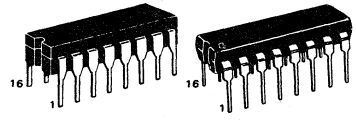
The MC14582B is a CMOS look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The device is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table shown below.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- High Speed Operation – 140 ns typical @ V_{DD} = 10 Vdc (from Data-in to Carry-out)
- Expandable to any Number of Bits
- Noise Immunity = 45% of V_{DD} typical
- All Buffered Outputs
- Low Power Dissipation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

LOOK-AHEAD CARRY BLOCK



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC EQUATIONS

$C_{n+x} = \overline{G0} + (\overline{P0} \bullet C_n)$

$C_{n+y} = \overline{G1} + (\overline{P1} \bullet \overline{G0}) + (\overline{P1} \bullet \overline{P0} \bullet C_n)$

$C_{n+z} = \overline{G2} + (\overline{P2} \bullet \overline{G1}) + (\overline{P2} \bullet \overline{P1} \bullet \overline{G0}) + (\overline{P2} \bullet \overline{P1} \bullet \overline{P0} \bullet C_n)$

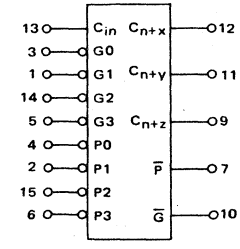
$\overline{G} = \overline{G3} + (\overline{P3} \bullet \overline{G2}) + (\overline{P3} \bullet \overline{P2} \bullet \overline{G1}) + (\overline{P1} \bullet \overline{P2} \bullet \overline{P3} \bullet \overline{G0})$

$\overline{P} = \overline{P3} \bullet \overline{P2} \bullet \overline{P1} \bullet \overline{P0}$

PIN DESIGNATIONS

DESIGNATION	PIN NO's	FUNCTION
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	3,1,14,5	Active-Low Carry-Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	4,2,15,6	Active-Low Carry-Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y} C_{n+z}	12,11,9	Carry Outputs
$\overline{G}$	10	Active-Low Group Carry-Generate Output
$\overline{P}$	7	Active-Low Group Carry-Propagate Output

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.4 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.8 μA/kHz) f + I_{DD}							
		15	I_T = (4.3 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 260 ns	t_{PHL}	Clock to Q	–	345	690	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 107 ns		10	–	140	280	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	

*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

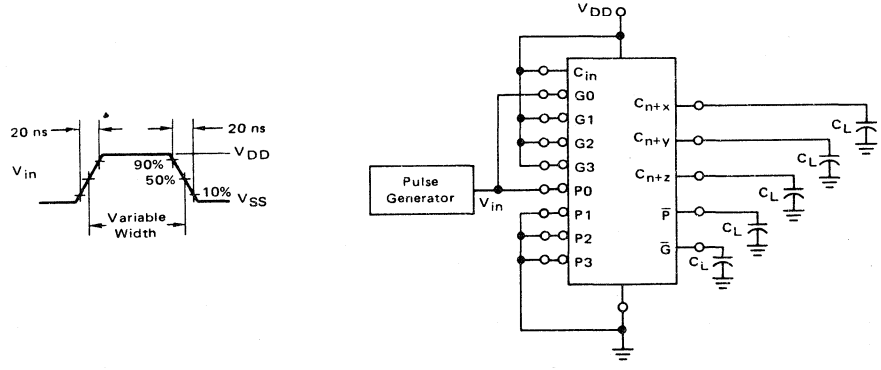


FIGURE 2 – SOURCE CURRENT TEST CIRCUIT

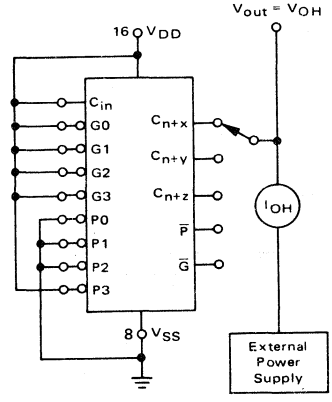


FIGURE 3 – SINK CURRENT TEST CIRCUIT

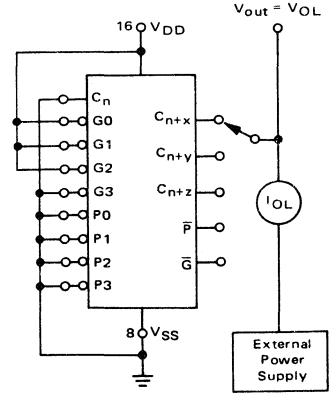
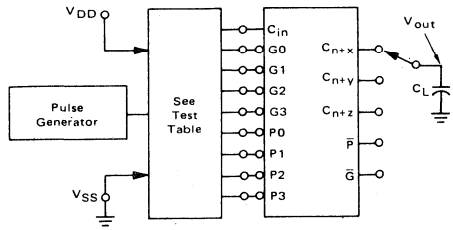
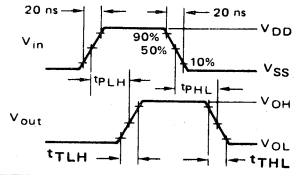


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

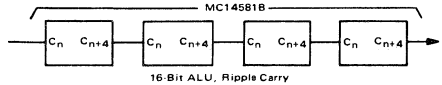


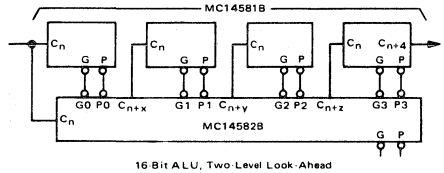
TEST TABLE

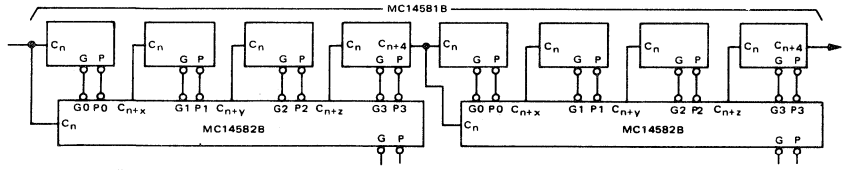
AC PATHS		DC DATA	
INPUT	OUTPUT	To V_{SS}	To V_{DD}
$\bar{P}0$	$\bar{P}$	Remaining $\bar{P}$'s, C_n	$\bar{G}$'s
$\bar{G}0$	$\bar{G}$	$\bar{P}$'s, C_n	Remaining $\bar{G}$'s
C_n	C_{n+x}, C_{n+y} C_{n+z}	$\bar{P}$'s	$\bar{G}$'s

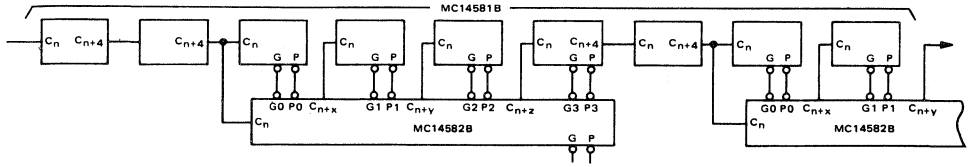


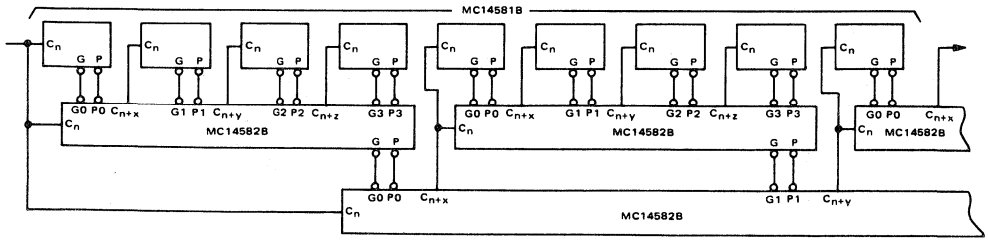
TYPICAL APPLICATIONS











A and B inputs and F outputs are not shown (MC14581B).

MOTOROLA

MC14583B

CMOS SSI

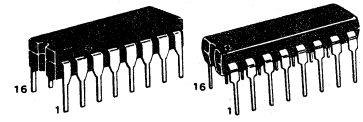
(LOW-POWER COMPLEMENTARY MOS)

DUAL SCHMITT TRIGGER

DUAL SCHMITT TRIGGER

The MC14583B is a dual Schmitt trigger constructed with complementary P-channel and N-channel MOS devices on a monolithic silicon substrate. Each Schmitt trigger is functionally independent except for a common 3-state input and an internally-connected Exclusive OR output for use in line receiver applications. Trigger levels are adjustable through the positive, negative, and common terminals with the use of external resistors. Applications include the speed-up of a slow waveform edge in interface receivers, level detectors, etc.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Schmitt Trigger Input Noise Immunity = 60% of V_{DD} Typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Resistor Adjustable Trigger Levels



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

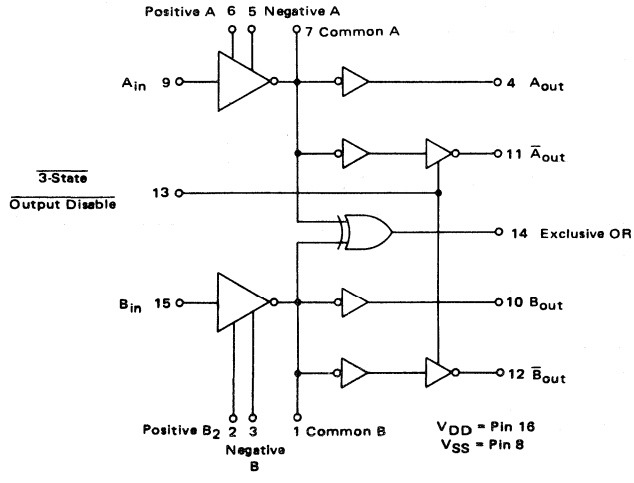
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

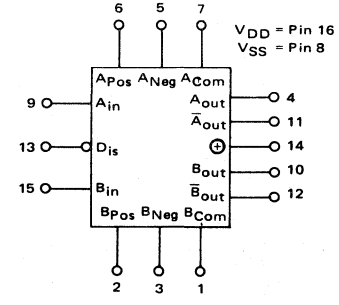
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS				
A	B	$\overline{Dis}$	A_{out}	$\bar{A}_{out}$	B_{out}	$\bar{B}_{out}$	⊕
0	0	0	0	R	0	R	0
0	0	1	0	1	0	1	0
0	1	0	0	R	1	R	1
0	1	1	0	1	0	1	1
1	0	0	1	R	0	R	1
1	0	1	1	0	0	1	1
1	1	0	1	R	1	R	0
1	1	1	1	0	1	0	0

R = High resistance at output

ELECTRICAL CHARACTERISTICS ($R1 = R2 = \infty$)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# A and B "0" Level	V_{IL}									Vdc
($V_O = 4.5$ or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
($V_O = 9.0$ or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
($V_O = 13.5$ or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
($V_O = 0.5$ or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
($V_O = 1.0$ or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
($V_O = 1.5$ or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
($V_{OH} = 2.5$ Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
($V_{OH} = 4.6$ Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
($V_{OH} = 9.5$ Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
($V_{OH} = 13.5$ Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
($V_{OL} = 0.4$ Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
($V_{OL} = 0.5$ Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
($V_{OL} = 1.5$ Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
($V_{OH} = 2.5$ Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
($V_{OH} = 4.6$ Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
($V_{OH} = 9.5$ Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
($V_{OH} = 13.5$ Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
($V_{OL} = 0.4$ Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
($V_{OL} = 0.5$ Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
($V_{OL} = 1.5$ Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance ($V_{in} = 0$)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.33\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (2.65\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.98\ \mu A/kHz)\ f + I_{DD}$							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*$T_{low} = -55°C$ for AL Device, $-40°C$ for CL/CP Device.
$T_{high} = +125°C$ for AL Device, $+85°C$ for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

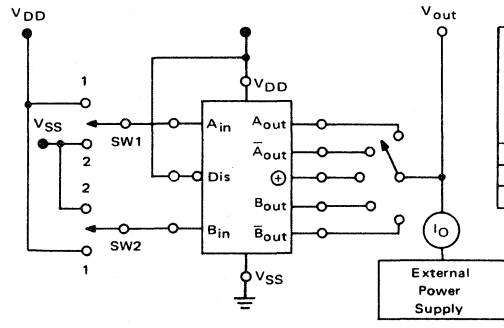
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
A_{in}, B_{in} to A_{out}, B_{out}	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	–	650	1300	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
A_{in}, B_{in} to A_{out}, B_{out}	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1015 ns	t_{PHL}	5.0	–	1100	2200	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 347 ns		10	–	380	760	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 235 ns		15	–	260	520	
A_{in}, B_{in} to Exclusive OR	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns	t_{PHL}	5.0	–	750	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns		10	–	280	560	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	340	
3-State Enable, Disable Delay Time (see figure 5)	t_{on},					ns
t_{on}, t_{off} = (1.7 ns/pF) C_L + 140 ns	t_{off}	5.0	–	225	450	
t_{on}, t_{off} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{on}, t_{off} = (0.5 ns/pF) C_L + 30 ns		15	–	55	110	
Positive Threshold Voltage	V_P	5.0	–	3.30	–	Vdc
(R1, R2 = 5.0 kΩ)		10	–	5.70	–	
		15	–	8.20	–	
Negative Threshold Voltage	V_N	5.0	–	1.70	–	Vdc
(R1, R2 = 5.0 kΩ)		10	–	4.30	–	
		15	–	6.80	–	
Hysteresis Voltage	V_H	5.0	0.85	1.70	3.40	Vdc
(R1, R2 = 5.0 kΩ)		10	0.70	1.40	2.80	
		15	0.70	1.40	2.80	
Threshold Voltage Variation, A to B	ΔV_T	5.0	–	0.1	–	Vdc
(R1, R2 = 5.0 kΩ)		10	–	0.15	–	
		15	–	0.20	–	

*The formula given is for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CHARACTERISTICS TEST CIRCUIT



OUTPUT UNDER TEST	OUTPUT SOURCE CHARACTERISTICS		OUTPUT SINK CHARACTERISTICS	
	TEST VALUE $V_{GS} = -V_{DD}$, $V_{DS} = V_{out} - V_{DD}$		TEST VALUE $V_{GS} = V_{DD}$, $V_{DS} = V_{out}$	
	SWITCH POSITION		SWITCH POSITION	
	SW1	SW2	SW1	SW2
A_{out}, B_{out}	1	1	2	2
$\bar{A}_{out}$, $\bar{B}_{out}$	2	2	1	1
Exclusive OR	1	2	1	1

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

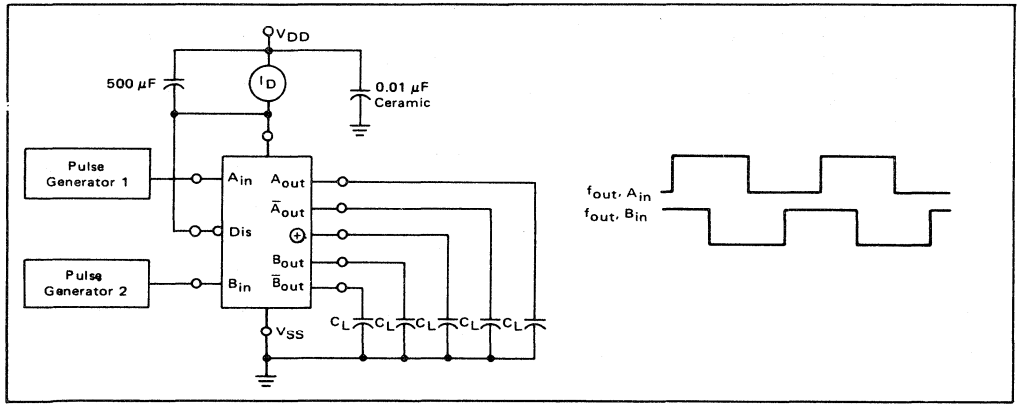
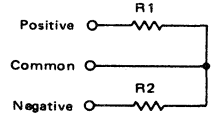
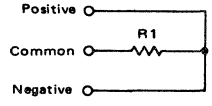


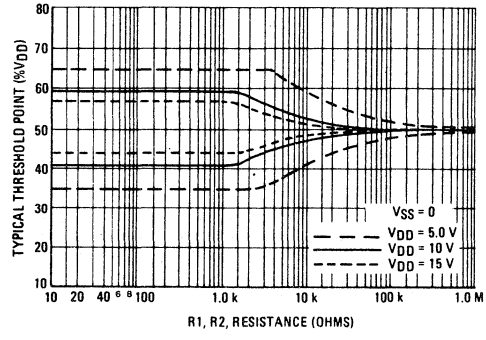
FIGURE 3 – TYPICAL THRESHOLD POINTS

A – Feedback scheme for independent threshold adjustment:



B – Feedback scheme for hysteresis adjustment:





MOTOROLA

MC14584B

CMOS SSI

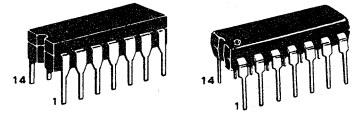
(LOW-POWER COMPLEMENTARY MOS)

HEX SCHMITT TRIGGER

HEX SCHMITT TRIGGER

The MC14584B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14584B may be used in place of the MC14069B hex inverter for enhanced noise immunity or to "square up" slowly changing waveforms.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD40106B and MM74C14
- Can Be Used to Replace MC14069B



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

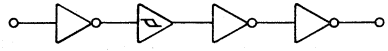
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

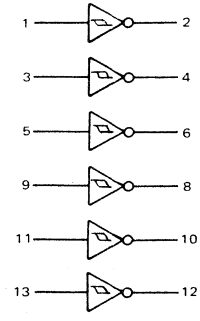
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

EQUIVALENT CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	34	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.8\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (3.6\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (5.4\ \mu A/kHz)\ f + I_{DD}$							
Hysteresis Voltage	V_H‡	5.0	0.27	1.0	0.25	0.55	1.0	0.21	1.0	Vdc
		10	0.36	1.3	0.30	0.70	1.2	0.25	1.2	
		15	0.77	1.7	0.60	1.1	1.5	0.50	1.4	
Threshold Voltage Positive-Going	V_{T+}	5.0	1.9	3.5	1.8	2.7	3.4	1.7	3.4	Vdc
		10	3.4	7.0	3.3	5.3	6.9	3.2	6.9	
		15	5.2	10.6	5.2	8.0	10.5	5.2	10.5	
Negative-Going	V_{T-}	5.0	1.6	3.3	1.6	2.1	3.2	1.5	3.2	Vdc
		10	3.0	6.7	3.0	4.6	6.7	3.0	6.7	
		15	4.5	9.7	4.6	6.9	9.8	4.7	9.9	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

‡$V_H = V_{T+} - V_{T-}$ (But maximum variation of V_H is specified as less than $V_{T+\,max} - V_{T-\,min}$).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0	–	125	250	ns
		10	–	50	100	
		15	–	40	80	

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

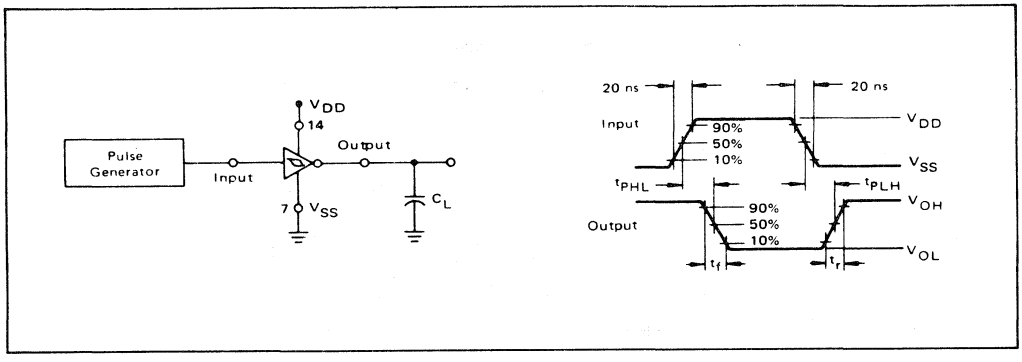


FIGURE 2 – TYPICAL SCHMITT TRIGGER APPLICATIONS

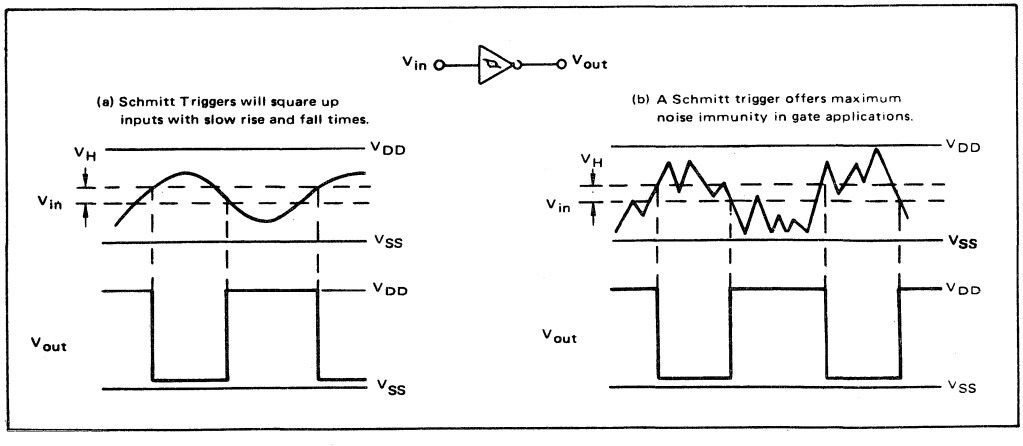
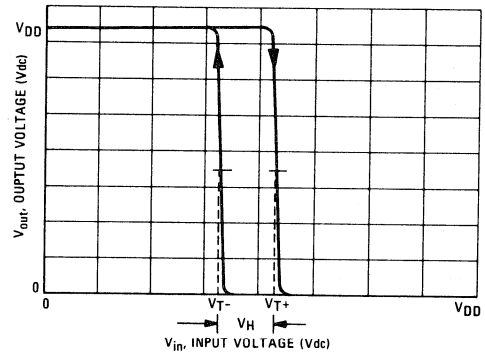


FIGURE 3 – TYPICAL TRANSFER CHARACTERISTICS



MOTOROLA

MC14585B

4-BIT MAGNITUDE COMPARATOR

The MC14585B 4-Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A<B, A=B, and A>B), and three outputs (A<B, A=B, and A>B). This device compares two 4-bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output. For words greater than 4-bits, units can be cascaded by connecting outputs (A<B), and (A=B) to the corresponding inputs of the next significant comparator (input A>B is connected to a high). Inputs (A<B), (A=B), and (A>B) on the least significant (first) comparator are connected to a low, a high, and a high, respectively.

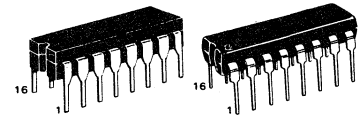
Applications include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- High Fanout > 50
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Expandable
- Applicable to Binary or 8421-BCD Code
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW POWER COMPLEMENTARY MOS)

4-BIT MAGNITUDE COMPARATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

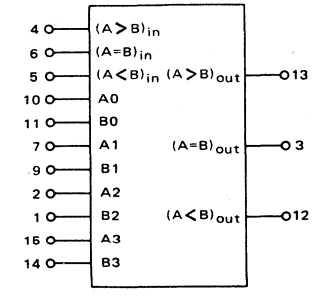
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	1	0	0	1
A3=B3	A2>B2	X	X	X	X	1	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	1	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	1	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	1	0	0

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.6 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.8 μA/kHz) f + I_{DD}							

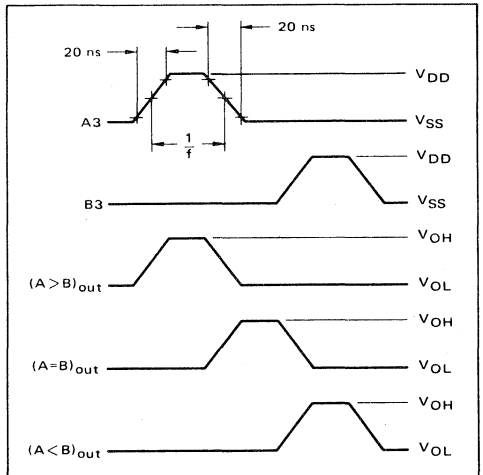
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Turn-Off Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 345 ns	t_{PHL}	5.0	–	430	860	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	–	130	260	

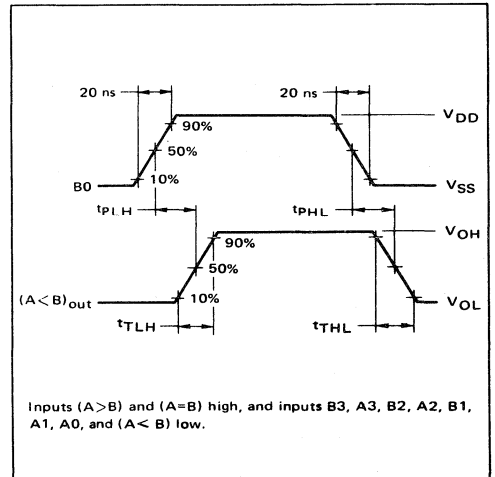
*The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS



Inputs (A>B) and (A=B) high, and inputs B2, A2, B1, A1, B0, A0 and (A<B) low
f in respect to a system clock.

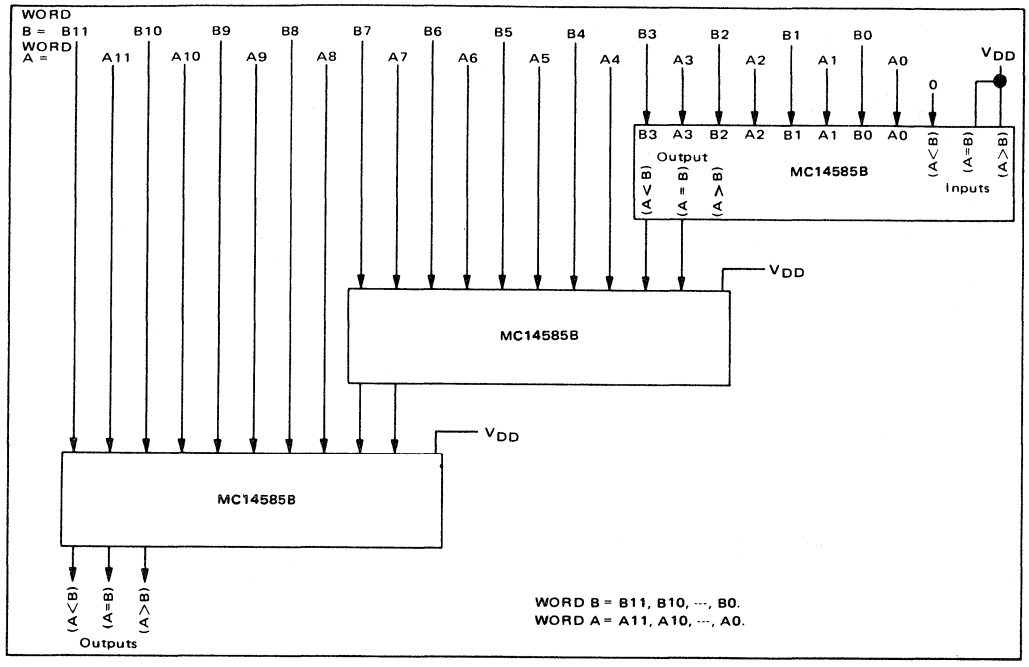
FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



Inputs (A>B) and (A=B) high, and inputs B3, A3, B2, A2, B1, A1, A0, and (A< B) low.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 3 – CASCADING COMPARATORS



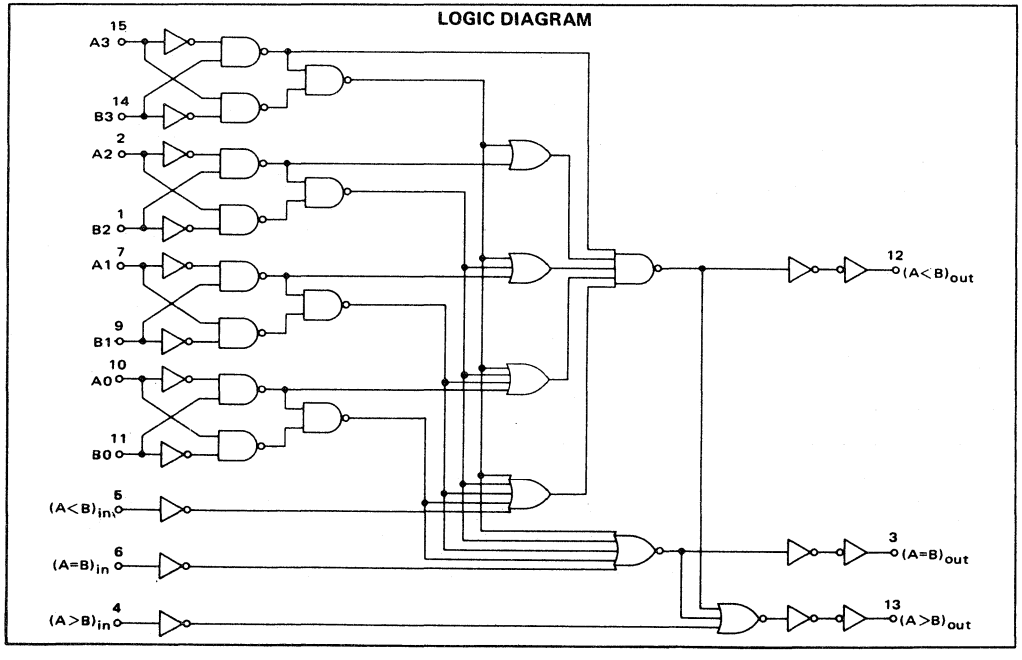
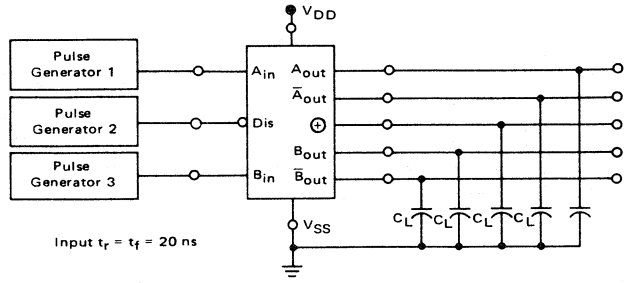
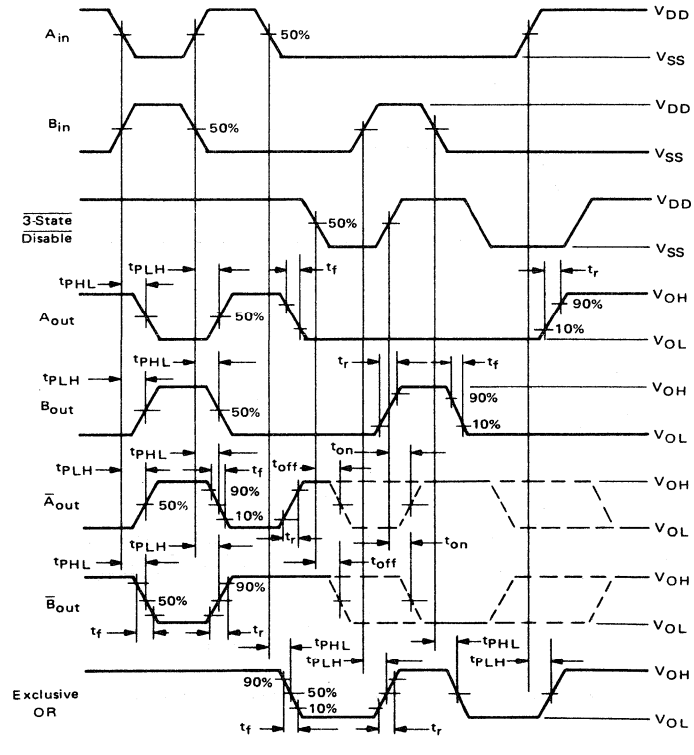


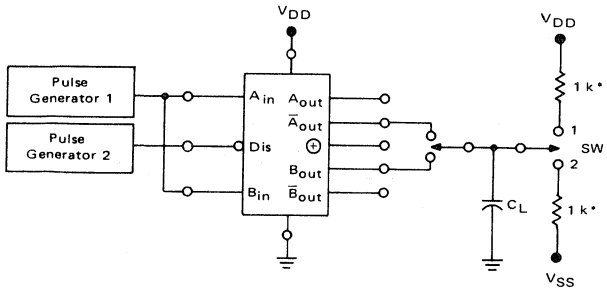
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





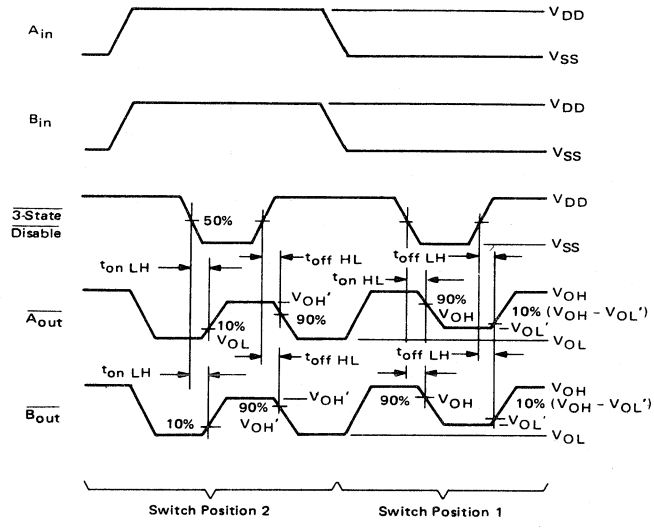
Note: Dashed lines indicate high output resistance.

FIGURE 5 – 3-STATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	SWITCH POSITION
$t_{on\ HL}$	1
$t_{on\ LH}$	2
$t_{off\ HL}$	2
$t_{off\ LH}$	1

*Metal film, ± 1%, 1/4 W or greater
C_L = 15 pF, which includes test circuit capacitance.



V_{OL}' and V_{OH}' refer to the levels present as a result of the 1 k ohm load resistors.

MOTOROLA

MC14597B
MC14598B

CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

8-BIT, BUS-COMPATIBLE
THREE-STATE LATCHES

Internal Counter – MC14597B
Binary Address – MC14598B

8-BIT BUS-COMPATIBLE LATCHES

The MC14597B and MC14598B are 8-bit latches, one addressed with an internal counter and the other addressed with an external binary address. The 8 latch-outputs are high drive, three-state and bus line compatible. The drive capability allows direct applications with MPU systems such as the Motorola 6800 family.

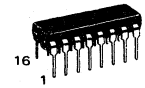
With MC14597B, a 3-bit address counter (clocked on the falling edge of Increment) selects the appropriate latch. The latches of the MC14598B are accessed via the Address pins, A0, A1, and A2. A $\overline{\text{Full}}$ Flag is provided on the MC14597B to indicate the position of the Address counter.

All 8 outputs from the latches are available in parallel when $\overline{\text{Enable}}$ is in the low state. Data is entered into a selected latch from the Data pin when the Strobe is high. Master reset is available on both parts.

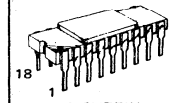
- Serial Data Input
- Three-State Bus Compatible Parallel Outputs
- Three-State Control Pin ($\overline{\text{Enable}}$) TTL Compatible Input
- Open Drain $\overline{\text{Full}}$ Flag (Multiple Latch Wire-O Ring)
- Master Reset
- Level Shifting Inputs on All Except $\overline{\text{Enable}}$
- Noise Immunity – 45% of V_{DD} Typical
- Diode Protection – All Inputs
- Supply Voltage Range – 3.0 Vdc to 18 Vdc
- Capable of Driving TTL Over Rated Temperature Range
  With Fanout as Follows:
  1 TTL Load
  4 LSTTL Loads
  9 LPTTL Loads



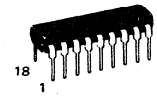
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 680



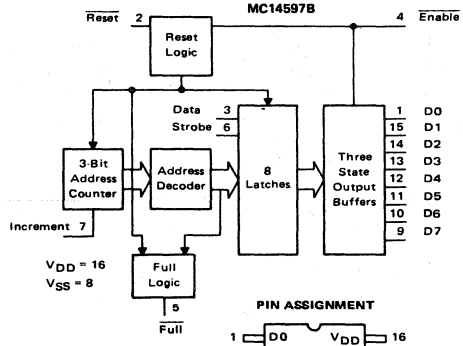
P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

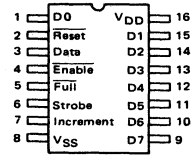
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAMS

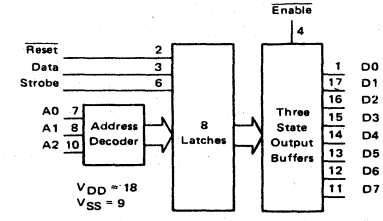
MC14597B



PIN ASSIGNMENT



MC14598B

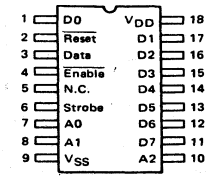


OUTPUT TRUTH TABLE

Enable	Outputs
1	High Impedence
0	D_n

D_n = State of nth latch

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltage referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, $\overline{\text{Enable}}$	V_{in}	-0.5 to V_{DD} +0.5	Vdc
Input Voltage, All Other Inputs	V_{in}	-0.5 to V_{DD} +12	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{out} be constrained to the range $V_{SS} \leq (V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# — $\overline{\text{Enable}}$ "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	0.8	–	1.1	0.8	–	0.8	
(V_O = 9.0 or 1.0 Vdc)		10	–	1.6	–	2.2	1.6	–	1.6	
(V_O = 13.5 or 1.5 Vdc)		15	–	2.4	–	3.4	2.4	–	2.4	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	2.0	–	2.0	1.9	–	2.0	–	
(V_O = 1.0 or 9.0 Vdc)		10	6.0	–	6.0	3.1	–	6.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	10	–	10	4.3	–	10	–	
Input Voltage# — "0" Level Other Inputs	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11	–	11	8.25	–	11	–	
Output Drive Current Source	I_{OH}									mAdc
($\overline{\text{Full}}$—Sink Only)										
(V_{OH} = 4.6 Vdc)		5.0	-1.0	–	-1.0	-2.0	–	-1.0	–	
(V_{OH} = 9.5 Vdc)		10	–	–	–	-6.0	–	–	–	
(V_{OH} = 13.5 Vdc)		15	–	–	–	-12	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.6	–	1.6	3.2	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	–	–	–	6.0	–	–	–	
(V_{OL} = 1.5 Vdc)		15	–	–	–	12	–	–	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Three-State Leakage Current	I_{TL}									μAdc
(AL Device)		15	–	±0.1	–	±0.00001	±0.1	–	±3.0	
(CL/CP Device)		15	–	±1.0	–	±0.00001	±1.0	–	±7.5	
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
†Total Supply Current at an External Load Capacitance (C_L) of 130 pF	I_T	5.0	I_T = (2.0 μA/kHz)f + I_{DD}							
		10	I_T = (4.0 μA/kHz)f + I_{DD}							
		15	I_T = (6.0 μA/kHz)f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

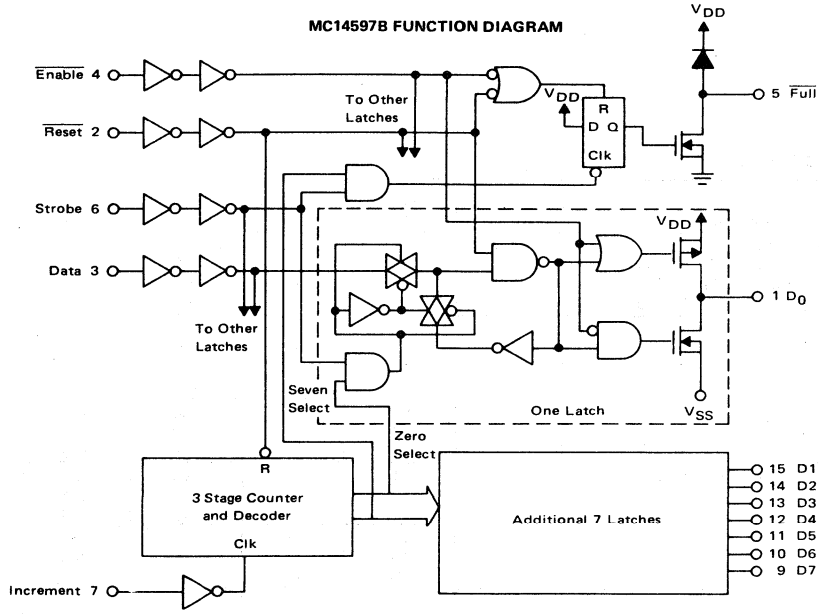
#Noise immunity specified for worst-case input combination. Noise Margin both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†The formulas given are for the typical characteristics only at 25°C.

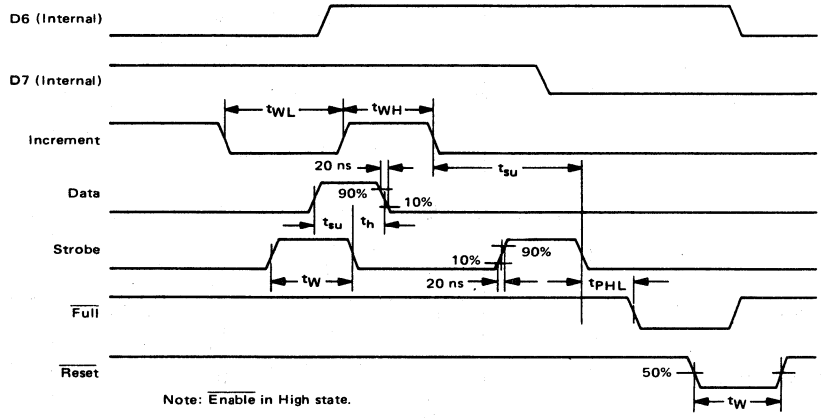
SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 130 pF + 1 TTL Load)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (0.5 ns/pF) C_L + 35 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.2 ns/pF) C_L + 25 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.16 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time						ns
$\overline{\text{Enable}}$ to Output	t_{PLH}, t_{PHL}	5.0	–	160	320	
		10	–	125	250	
		15	–	100	200	
Strobe to Output		5.0	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
Strobe to $\overline{\text{Full}}$ (MC14597B only)		5.0	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
Reset to Output		5.0	–	175	350	ns
		10	–	90	180	
		15	–	70	140	
Pulse Width						
$\overline{\text{Enable}}$	t_{WH}, t_{WL}	5.0	320	160	–	ns
		10	240	120	–	
		15	160	80	–	
Strobe		5.0	200	100	–	ns
		10	100	50	–	
		15	80	40	–	
Increment (MC14597B only)		5.0	200	100	–	ns
		10	100	50	–	
		15	80	40	–	
Reset		5.0	300	150	–	ns
		10	160	80	–	
		15	100	50	–	
Setup Time						
Data	t_{su}	5.0	100	50	–	ns
		10	50	25	–	
		15	35	20	–	
Address (MC14598B only)		5.0	200	100	–	ns
		10	100	50	–	
		15	70	35	–	
Increment (MC14597B only)		5.0	400	200	–	ns
		10	200	100	–	
		15	170	85	–	
Hold Time						
Data	t_h	5.0	100	50	–	ns
		10	50	25	–	
		15	35	20	–	
Address (MC14598B only)		5.0	100	50	–	ns
		10	50	25	–	
		15	35	20	–	

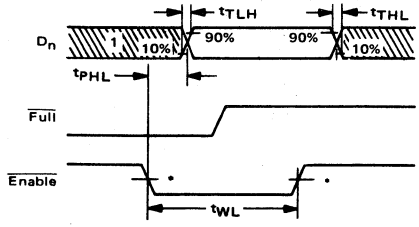
MC14597B FUNCTION DIAGRAM



MC14597B TIMING DIAGRAMS



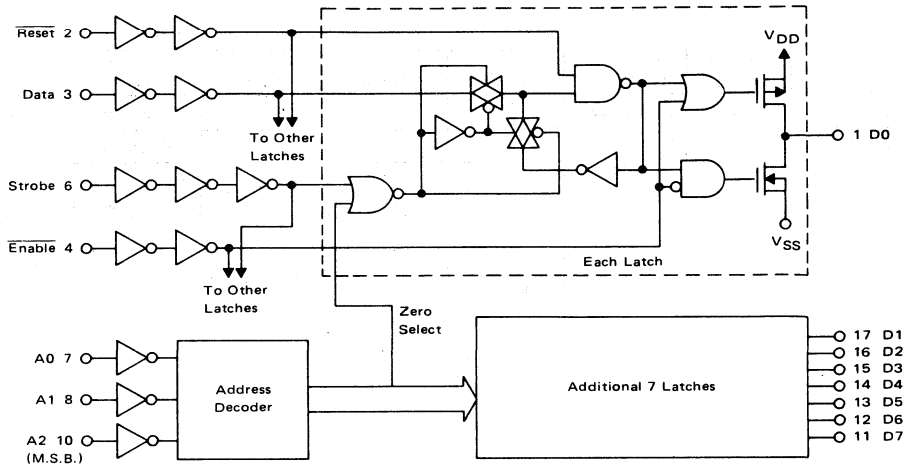
Note: $\overline{\text{Enable}}$ in High state.



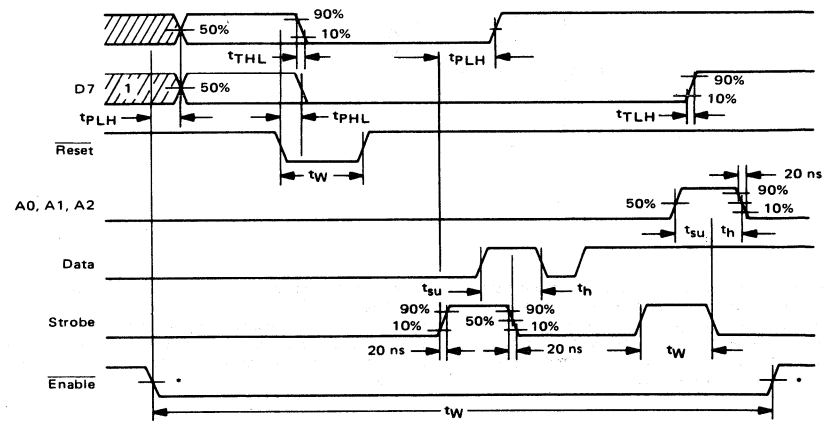
*1.4 V with V_{DD} = 5.0 V

NOTES: 1. High-impedance output state (another device controls bus).
2. $\overline{\text{Reset}}$ in High state.

MC14598B FUNCTION DIAGRAM



MC14598B TIMING DIAGRAM



* 1.4 V with V_{DD} = 5.0 V.

NOTES 1. High-impedance output state (another device controls bus).
2. Output Load as for MC14597B.

LATCH TRUTH TABLE

Strobe	$\overline{\text{Reset}}$	Addressed Latch	Other Latches
0	1	*	*
1	1	Data	*
X	0	0	0

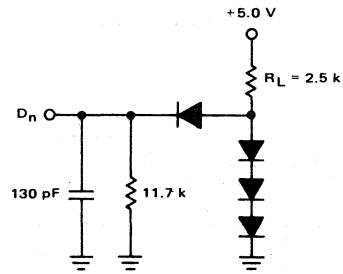
* = No change in state of latch
X = Don't care

TRUTH TABLE FOR MC14597B

Increment	$\overline{\text{Enable}}$	$\overline{\text{Reset}}$	Address Counter	$\overline{\text{Full}}$
⌐	X	1	Count Up	–
⌐	X	1	No Change	–
X	1	0	Reset to Zero	Set to One
X	0	1	No Change	Set to One
X	1	1	If at ADDRESS 7	To Zero on Falling Edge of STROBE

X = Don't care

Test Load
All Outputs



Circuit diagrams external to or containing Motorola products are included as a means of illustration only. Complete information sufficient for construction purposes may not be fully illustrated. Although the information herein has been carefully checked and is believed to be reliable, Motorola assumes no responsibility for inaccuracies. Information herein does not convey to the purchaser any license under the patent rights of Motorola or others.

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MOTOROLA

MC14599B

For Complete Data See
MC14099B

8-BIT ADDRESSABLE LATCHES

The MC14099B and MC14599B are 8-bit addressable latches. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. Chip enable must be high for writing into MC14599B. For the MC14599B the data pin is a bidirectional data port and for the MC14099B the input is a unidirectional write only port. The Write/$\overline{\text{Read}}$ line controls this port in the MC14599B.

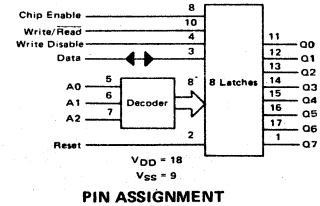
The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/$\overline{\text{Read}}$ or Chip Enable.

A Master Reset capability is available on both parts.

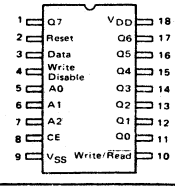
- Serial Data Input
- Parallel Output
- Low Input Capacitance — 5.0 pF typical
- Master Reset
- Noise Immunity — 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



PIN ASSIGNMENT

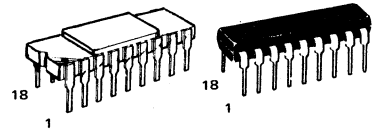


CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT ADDRESSABLE LATCH

WITH BIDIRECTIONAL PORT



L SUFFIX
CERAMIC PACKAGE
CASE 680

P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC141000
MC141200
MC141099

Advance Information

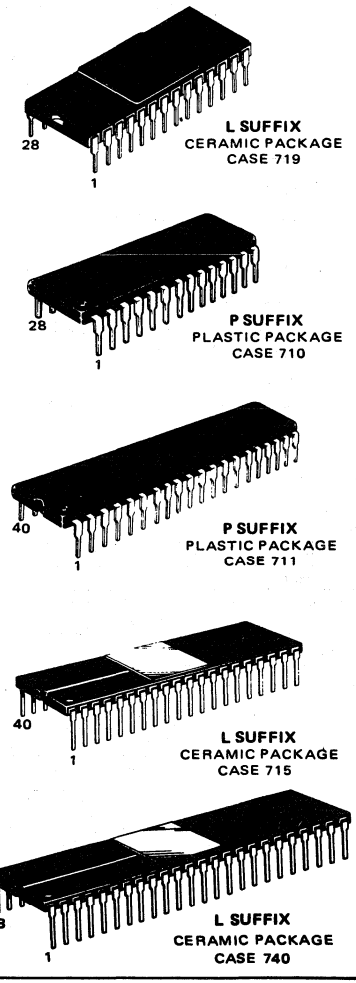
CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

ONE CHIP MICROCOMPUTERS

ONE CHIP MICROCOMPUTERS

The MC141000 family is a series of 4-bit CMOS Microcomputers designed for dedicated applications. The CMOS technology of the MC141000 family provides the flexibility of microcomputers, for battery-powered and battery-backed-up applications. The MC141000 and MC141200 include ROM, RAM, and I/O for self-contained configurations in 28 and 40-pin packages. The 48-pin MC141099 has RAM and I/O with provision for external program memory. The MC141099 serves lower-volume applications such as prototyping or pilot production of MC141000 and MC141200 systems.

FEATURES		MC141000	MC141200	MC141099
Package Pin Count		28 Pins	40 Pins	48 Pins
Instruction Read Only Memory		1024 X 8 (8,192 Bits)		None
Data Random Access Memory		64 X 4 (256 Bits)		
"R" Individually Addressed Outputs		11	16	16
"O" Parallel Latched Data Outputs		8 Bits		5 Bits
"R" and "O" Output Drive		Source 20 mA		
Maximum-Rated Voltage		6.5 V		
Working Registers		Static 2–4 Bits Each		
Instruction Set		See Table 2		
External Address Lines		None		10
On-Chip Oscillator		Yes		
Maximum Power Dissipation	5 V, 600 kHz	11.5 mW		
	5 V, 100 kHz	2.8 mW		
	3 V, 200 kHz	1.5 mW		
	3 V, 30 kHz	0.36 mW		



APPLICATIONS

- Appliance Controllers
- Calculators
- Toys
- Radio Controllers
- Communications Controllers
- Data Terminals
- Cash Registers
- Heating/Air-Conditioning Controllers
- Remote Sensing System
- Printing Controllers
- Security Systems
- Power Systems Control
- Automotive Control

The above applications of the MC141000 family demonstrate its wide potential. Motorola accepts customer programs or will contract complete program development given the specifications for the application. Customer hardware and software support is available for developing programs and debugging systems. This consists of one board and a software package using the M6800 EXORciser. Contact your local sales office for details.

ORDERING INFORMATION

MC14XXXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.5	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin, All Inputs	I	10	mAdc
DC Current Drain, V_{DD} Pin	I	250	mAdc
DC Current Drain, V_{SS} Pin	I	20	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Total Power Dissipation	P_D	See Figure 1	mW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0)

Parameter	Symbol	Value	Unit
DC Supply Voltage — High Speed Clock Full Range Operation	V_{DD}	+4.75 to +6.0 +3.0 to +6.0	Vdc
Clock Frequency — V_{DD} = 5.0 Vdc ± 5% V_{DD} = 3.0 Vdc Min.	f_{Clk}	DC to 600 DC to 200	kHz

ELECTRICAL CHARACTERISTICS (V_{DD} = +5.0 V, V_{SS} Gnd, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current — K Inputs and INIT	I_{in}				μAdc
(V_{in} = 5.0 V)		75	100	135	
(V_{in} = 0.0 V)		—	-0.00001	-0.3	
Input Current — I Inputs (MC141099 Only)	I_{in}				μAdc
(V_{in} = 5.0 V)		—	0.00001	0.3	
(V_{in} = 0.0 V)		—	-0.00001	-0.3	
Input Voltage — I Inputs (MC141099 Only)					Vdc
	V_{IL}	—	—	0.8	
	V_{IH}	2.0	—	—	
Input Voltage — Other Inputs					Vdc
	V_{IL}	—	—	1.5	
	V_{IH}	3.5	—	—	
Output Drive — R and O Outputs					mAdc
(V_{OH} = 2.4 V) — See Figure 2	I_{OH}	-20	—	—	
(V_{OL} = 0.4 V, T_A = 85°C, V_{DD} = 4.75 V)	I_{OL}	1.6	—	—	
Output Drive — PA and PC Outputs (MC141099 Only)					μAdc
(V_{OH} = 4.6 V) (T_A = 85°C, V_{DD} = 4.75 V)	I_{OH}	-100	—	—	
(V_{OL} = 0.4 V)	I_{OL}	100	—	—	
Average Supply Current	I_{DD}	—	—	See Figure 3	μAdc
Static Supply Current	I_{DD}	—	60	300	μAdc
(V_{DD} = 6.0 V)					
Oscillator Frequency	f_{Clk}	No Limit	—	600	kHz
(V_{DD} = 4.75 V)					
Internal Oscillator Frequency for R_{ext} = 30 kΩ	f_{Clk}	400	500	600	kHz
Input Capacitance — K Inputs and INIT	C_{in}	—	—	7.5	pF
Input Capacitance — Clock Input	C_{io}	—	—	30	pF

FIGURE 1 – TOTAL POWER DISSIPATION

Care must be taken to ensure that the maximum power dissipation of the package is not exceeded.

$$T_{stg} = T_A + (P_D)(\theta_{JA})$$

where T_{stg} is maximum storage temperature (150°C)

T_A is ambient operating temperature

P_D is total power dissipation:

$$P_D = (I_{DD})(V_{DD}) + (I_{OH})(V_{DD} - V_{OH}) + (I_{OL})(V_{OL} - V_{SS})$$

(I_{OH} and I_{OL} are the sum of all output pins)

	θ_{JA} Value	
	Ceramic	Plastic
28-Pin Package	58	98
40-Pin Package	50	95
48-Pin Package	50	–

FIGURE 2 – MINIMUM OUTPUT SOURCE CURRENT versus OUTPUT VOLTAGE (R and O Outputs)

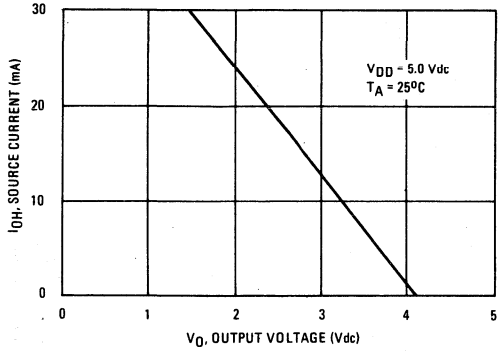
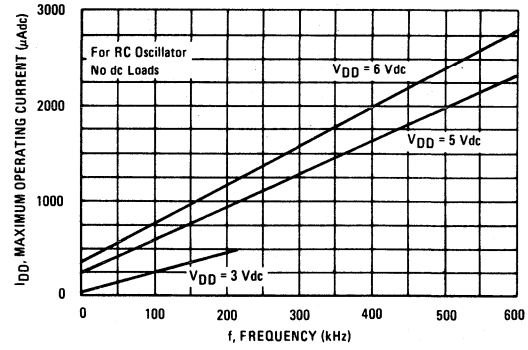
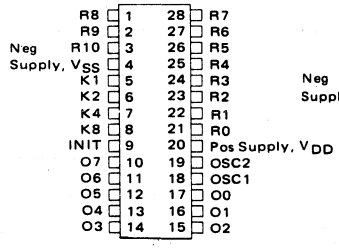


FIGURE 3 – MAXIMUM OPERATING CURRENT versus OSCILLATOR FREQUENCY

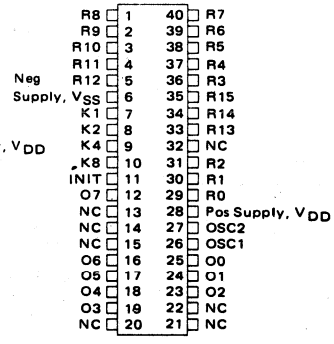


PIN ASSIGNMENTS

MC141000



MC14 1200



MC141099

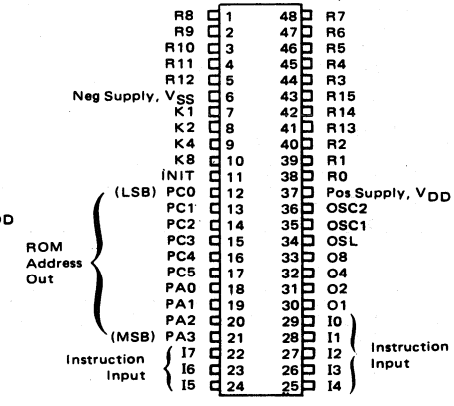
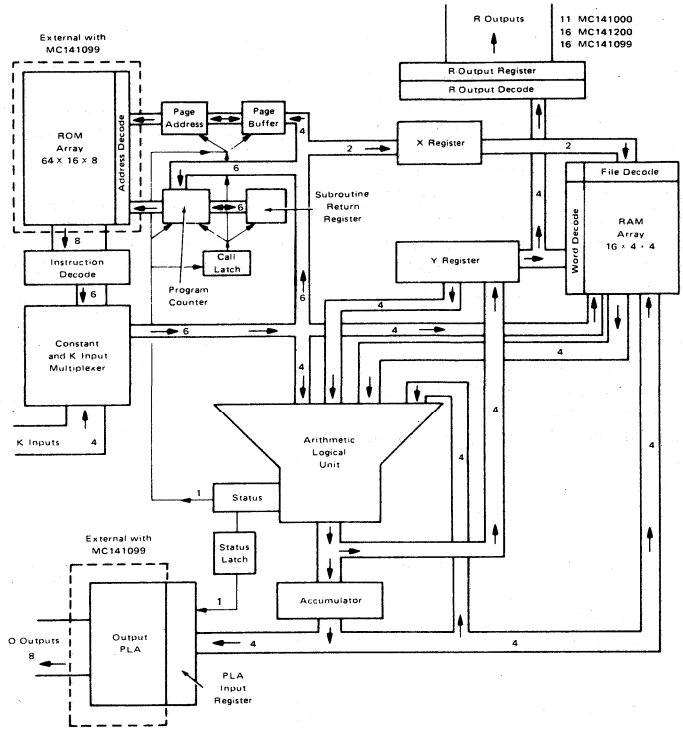


FIGURE 4 – FUNCTIONAL BLOCK DIAGRAM – MC141000/MC141200/MC141099



The block diagram above shows the resources available to the MC141000/1200/1099 programmer. They are:

A — The accumulator is used to store the result of an ALU operation for subsequent operations.

ALU — The arithmetic logical unit performs calculation and decision-making tasks.

K Inputs — The K lines are the data input port. Since there are only four input lines, they are usually multiplexed under control of the R lines. The inputs are diode protected and have a pull-down resistor of approximately 50 kΩ; therefore, open inputs are read as a logic low.

O Outputs — The eight outputs of the PLA are connected to output drivers which comprise the O outputs. These output drivers may be manufactured as open emitter, active sink, or push-pull at the user's option.

PLA — The output programmable logic array is user-defined to specify the state of each of the eight O outputs for each of the 32 possible PLAIR outputs.

PLAIR — The programmable logic array input register is a 5-bit latch which latches the four accumulator bits and the output of the status latch.

RAM — Variable data is stored in the 64-word, 4-bit per word Random Access Memory. Data is accessed by decoding a 2-bit file address (X register) and 4-bit word address (Y register).

ROM Array — The user's instructions are mask programmed into the Read Only Memory (ROM). Instructions are addressed by a page address register (PA) and program counter (PC). A single subroutine return register (SRR) and page buffer register (PB) permit a subroutine call to any location within the ROM.

R Outputs — The output of the Y register is decoded to select one of the R-output lines which can then be set or reset under program control. The R lines are used as control lines to scan keyboards and displays, perform handshakes, and interface external logic. The R outputs may be manufactured as open emitter, active sink, or push-pull at the user's option.

S — All branches and subroutine calls are dependent on the state of status logic. It may be set or reset on logical or arithmetic operations and is set by the remainder of the instructions.

SL — The status latch stores the state of the status logic in order to preserve it for subsequent O output operations.

NOTE: S and SL are NOT identical.

Y Register — The Y register is a multipurpose regiser used to address a word in a RAM file, to select an R output for manipulation by subsequent instructions, or as a general-purpose counting and storage register.

MICROCOMPUTER OPERATION

The MC141000/1200/1099 program controls data input, storage, processing, and output. The microcomputer internal organization is shown in Figure 4. The processing of data occurs in the arithmetic logic unit (ALU). K-input data enters the ALU and is stored in the 4-bit accumulator. The accumulator output accesses the output latches, RAM storage, or the ALU input. Data is stored in the 256-bit RAM, organized into 64 words, 4 bits per word. The 4-bit words are grouped into four 16-word files addressed by a 2-bit X register. The 4-bit Y register addresses one of the 16 words in a file.

The 43 basic instructions handle I/O, constant data from the ROM, bit control, internal data transfer, arithmetic processing, logic comparison, conditional and nonconditional branching and subroutines.

The system designer has access for mask programming the following functions:

1. ROM – 1024 Words of 8 Bits
2. Programmable Logic Array for O Outputs
3. Output Drivers

The MC141000 microcomputer consists of seven subsystems:

1. Read Only Memory (ROM)
2. Random Access Memory (RAM)
3. Output Ports
4. Input Port
5. Arithmetic Logical Unit (ALU)
6. The Instruction Decoder
7. Clock

The following paragraphs describe how each of these subsystems is controlled by the instruction set. Every instruction occupies a single memory byte and is executed in one instruction cycle (six clock cycles).

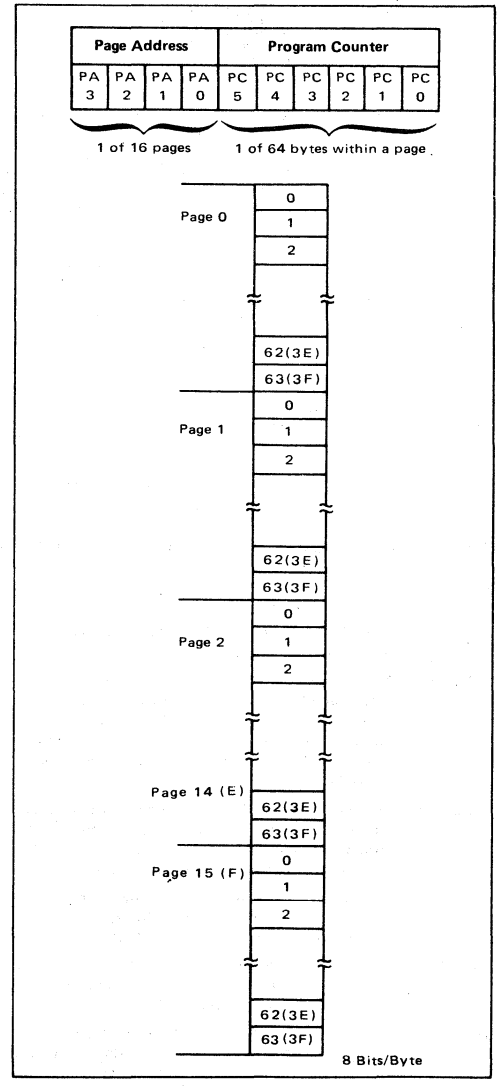
ROM ARRAY

The ROM in the MC141000/1200 consists of 8192 bits of mask-programmed memory organized as 1024 8-bit instructions. It is divided into 16 pages of 64 instructions per page. See Figure 5.

Instructions within ROM are addressed by the page address register (PA) which contains the page number, and the program counter (PC) which contains the location of the instruction relative to the beginning of the page. The PC is incremented prior to fetching the next instruction (unless diverted by a BRanch or CALL) so each instruction is accessed in the numerical order of its address. A carry from the PC is not added to the PA so the program "wraps around" within the page rather than executing the first instruction of the following page. Upon power up, the PC is set to zero and the PA and PB are set to 15.

The MC141099 addresses an external ROM program via ten address output lines. These are 6 bits from PC (PC0–PC5) and 4 bits from PA (PA0–PA3). The 8-bit instruction bytes are received by the MC141099 from an external ROM on 8 TTL compatible instruction input lines (I0–I7).

FIGURE 5 – ROM ORGANIZATION



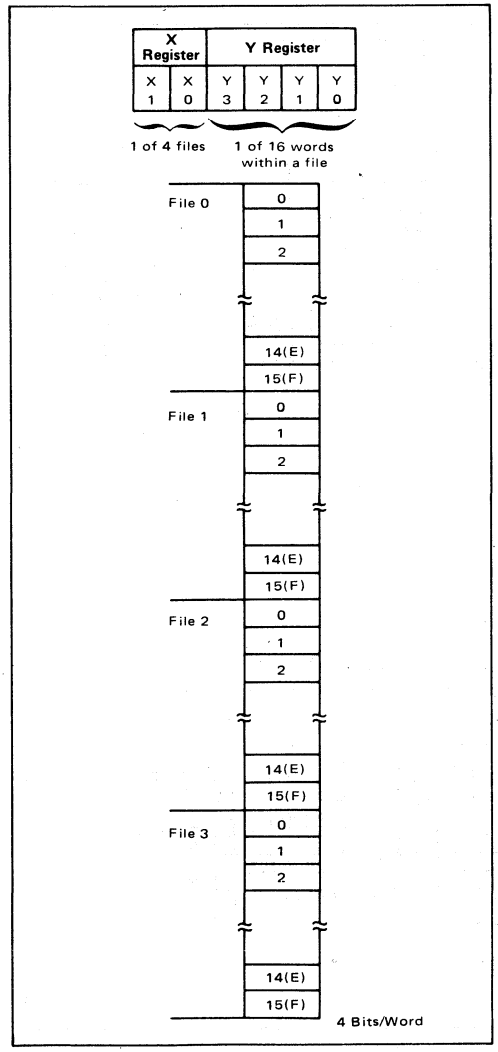
RANDOM ACCESS MEMORY – RAM

RAM consists of 256 bits organized into 64 4-bit words. For purposes of addressing, the 4-bit words are organized into four files of 16 4-bit words per file, Figure 6.

The X register is decoded to select 1 of the 4 RAM files; and the Y register is decided to address 1 of the 16 words in the selected file.

Individual bits within the RAM can be set, reset and tested under program control.

FIGURE 6 – RAM ORGANIZATION



OUTPUT PORTS

Two output ports (R and O) are included in the microcomputer. The MC141000 has eleven R outputs and the MC141200 and MC141099 each have sixteen R outputs. The MC141000 and MC141200 each have eight O outputs, while the MC141099 has five. The number of R outputs is the only difference between the MC141000 and the MC141200.

R-output lines are used primarily as control or "handshake" lines, and to multiplex external hardware. The R output which is to be operated on is selected by a binary decode of the contents of the Y register. Set R and reset R instructions change the state of one R output at a time.

The eight O-output lines on the MC141000 and MC141200 are the decoded outputs of the contents of the 5-bit PLAIR. Since the PLAIR is loaded from the A and the SL, these registers must be "set up" prior to an output operation. The status latch can only be loaded by the YNEA (Y register not equal to accumulator) instruction while the contents of the accumulator may be modified by numerous other instructions. The MC141099 brings out the 5-bit PLAIR to allow external decoding. An external PROM/EPROM could be used to simulate the PLA. Figure 7 shows how EPROMS may be used with MC141099 to emulate an MC14100 or an MC141200.

In a typical application, the first four R lines might be used as digit selects for outputting a four-digit decimal number using the PLA programmed as a seven-segment decode as shown in Figure 8.

The MC141000/1200 outputs may be mask programmed in any of three configurations. Figure 9 shows the open emitter circuit capable of sourcing 20 mA at V_O = 2.4 V and V_{DD} = 5.0 V, which will drive an LED. Figure 10 is the open drain circuit capable of sinking 1.6 mA over temperature, which will drive one TTL load or four LSTTL loads. The source and sink devices are combined in the active push-pull circuit of Figure 11. The MC141099 also has outputs as in Figure 11.

INPUTS

The input lines consist of the four K-input lines and the initialize (INIT) line. All inputs are static-protected CMOS inputs with pulldown of about 50 kΩ. Thus, an open input is equivalent to logic 0. The circuit is shown in Figure 12.

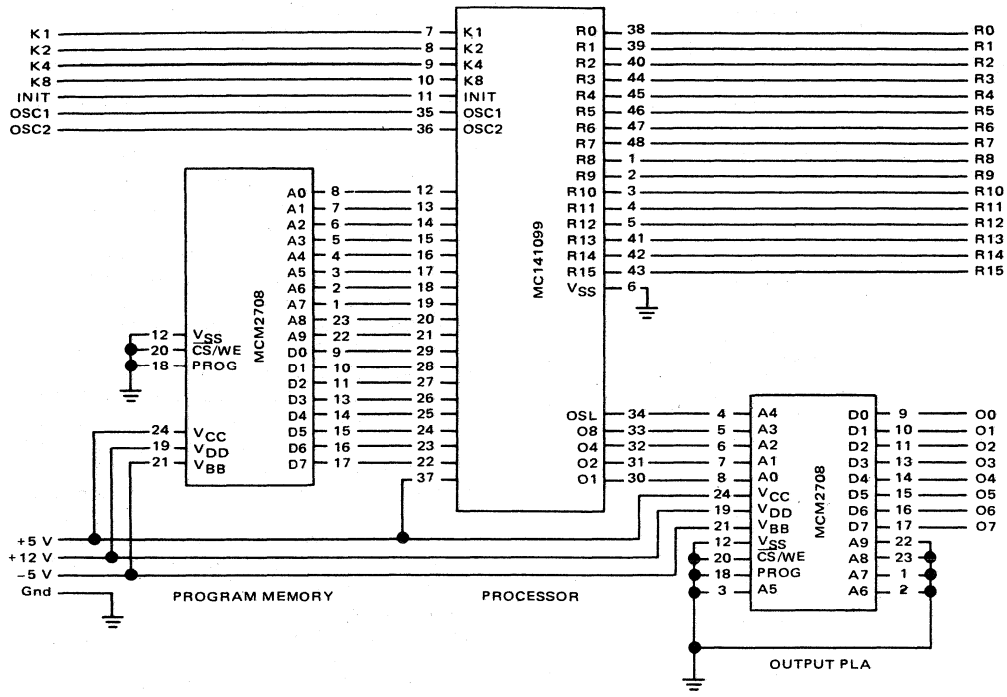
When power is applied, the registers shown in Table 1 are loaded as shown for power up. All other internal registers and RAM come up in an arbitrary state.

After power is applied, the initialize (INIT) input may be used to reinitialize the processor. Internally, INIT has

TABLE 1 – POWER UP AND INITIALIZE CONDITIONS

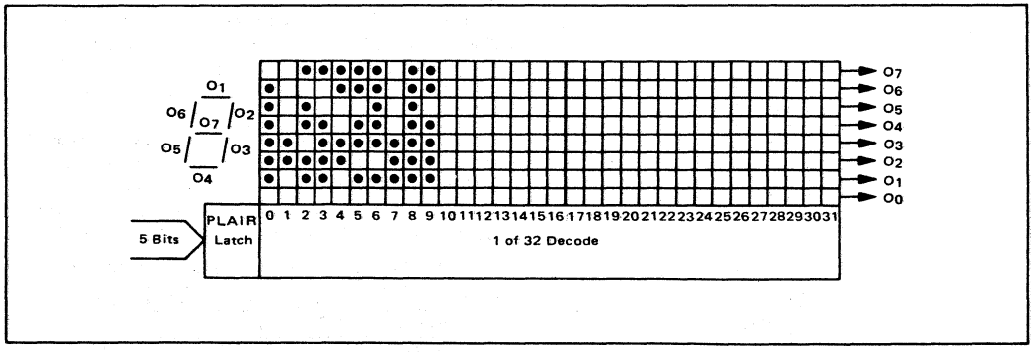
	PC	PA	PB	CL	PLAIR	R Outputs
Power Up	0	F_{16}	F_{16}	0	0	0
Initialize	0	$\overline{K}$ ·	$\overline{K}$	0	0	0

FIGURE 7 – USING THE MC141099 TO EMULATE MC141000/MC141200 IN REAL-TIME



NOTE: The OPLA EPROM outputs may require buffers depending on the requirements of the user's circuit. The EPROM outputs are TTL compatible.

FIGURE 8 – OUTPUT PLA EXAMPLE – 7-SEGMENT DISPLAY DECODE



a 50 kΩ pull-down resistor which holds the INIT line low. It must be held high for a minimum of 6 full clock cycles and then returned to the low state. If a mechanical switch or other mechanical device is used to control INIT, it may be necessary to include a method of contact debounce to ensure a valid INIT pulse.

A valid INIT pulse causes the registers to be initialized as shown in the table. The contents of registers other than those shown remain unchanged during initialize. Note that the PA and PB are loaded with the 1's complement of the K-input lines (K8 = MSB). This feature allows the MC141000 to be initialized to the first instruction on any page by controlling the K inputs. This is useful where the same circuit may be used for several applications. Since the K inputs have 50 kΩ pull-down resistors, open inputs are a 0 (unless driven from another device) and the 1's complement (F_{16}) is loaded into PA and PB.

ARITHMETIC LOGICAL UNIT (ALU)

The ALU is the calculating and decision-making portion of the MC141000/1200/1099 hardware and consists of a 4-bit adder/comparator and the status logic.

The adder/comparator can add, subtract, compare two numbers, add +1, −1, 6, 8, and 10.

The status logic is selectively set or reset by add, subtract, increment, decrement, compare and bit-test operations. Other instructions always set the status logic to a 1.

INSTRUCTION DECODE

The instruction decode logic latches every instruction fetched from ROM and configures the internal logic to execute the current instruction. The instruction set is listed in Table 2.

CLOCK

The internal oscillator cirucit operates with quartz crystals, ceramic resonators, an external resistor and from an external clock source. These oscillator circuit connections are shown in Figures 13, 14, and 15. Figure 16 shows the typical oscillation frequency with an external resistor. The discrete component values used with the quartz crystal and ceramic resonator oscillators may vary depending upon crystal/resonator manufacturer.

FIGURE 9 – OPEN EMITTER OUTPUT CIRCUIT

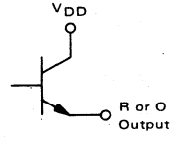


FIGURE 10 – OPEN DRAIN OUTPUT CIRCUIT

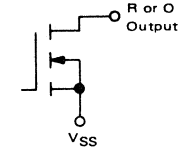


FIGURE 11 – ACTIVE PUSH-PULL OUTPUT CIRCUIT

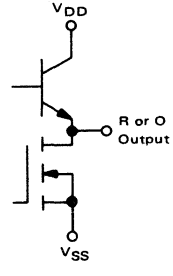


FIGURE 12 – INPUT CIRCUIT WITH PULLDOWN AND STATIC PROTECTION

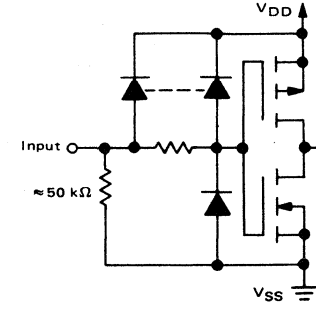
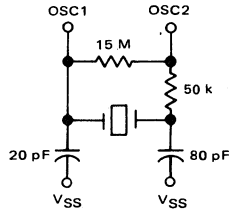


FIGURE 13 – EXTERNAL COMPONENTS FOR QUARTZ CRYSTAL OR CERAMIC RESONATOR OSCILLATOR



Component values typical for 500 kHz crystal.

FIGURE 14 – OSCILLATOR CIRCUIT WITH ONE EXTERNAL RESISTOR

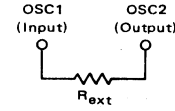


FIGURE 15 – EXTERNAL CLOCK SOURCE INPUT

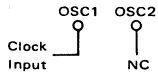


FIGURE 16 – TYPICAL OSCILLATOR FREQUENCY versus EXTERNAL RESISTANCE

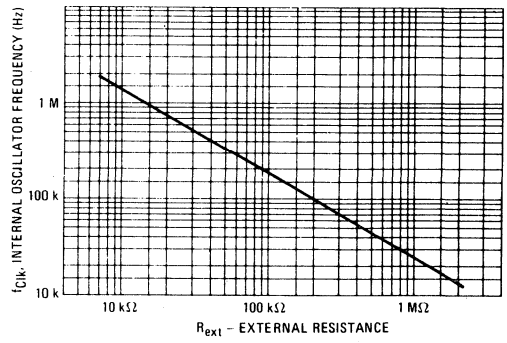


TABLE 2 – MC141000/1200/1099 INSTRUCTION SET

Opcode	Mnemonic	Description
0111 (C)	ALEC	If accumulator is less than or equal to I(C) field, status = 1.
00101001	ALEM	If accumulator is less than or equal to M(X,Y), status = 1.
00100101	AMAAC	Add memory to accumulator. Accumulator = result, status = carry.
00000110	A6AAC	Add 6 to accumulator. Accumulator = result, status = carry.
00000001	A8AAC	Add 8 to accumulator. Accumulator = result, status = carry.
00000101	A10AAC	Add 10 to accumulator. Accumulator = result, status = carry.
10 (W)	BR	Branch to label if status = 1.
11 (W)	CALL	Call subroutine if status = 1.
00101111	CLA	Clear contents of accumulator.
00001011	CLO	Clear PLA Input Register.
00000000	COMX	Complement X-Register.
00101101	CPAIZ	Complement accumulator, then add 1. If accumulator = 0, status = 1.
00000111	DAN	Decrement accumulator. If no borrow, status = 1.
00101010	DMAN	Load M(X, Y) into accumulator and decrement. If no borrow, status = 1.
00101100	DYN	Decrement Y-register. If no borrow, status = 1.
00001110	IA	Increment accumulator.
00101000	IMAC	Load M(X, Y) into accumulator and increment. Status = carry.
00101011	IYC	Increment Y-Register. Status = carry.
00001001	KNEZ	If K-inputs not equal to zero, status = 1.
0001 (C)	LDP	Load page buffer with I(C) field.
001111 (B)	LDX	Load X-register with I(B) field.
00100110	MNEZ	If M(X, Y) not equal to zero, status = 1.
001101 (B)	RBIT	Reset bit I(B) of M(X,Y).
00001111	RETN	Return from subroutine.
00001100	RSTR	Reset R-line specified by Y-register.
00100111	SAMAN	Subtract accumulator from memory. Accumulator = result. If no borrow, status = 1.
001100 (B)	SBIT	Set Bit I(B) of M(X,Y).
00001101	SETR	Set R-line specified by Y-register.
00000011	TAM	Transfer accumulator contents to M(X,Y).
00100000	TAMIY	Transfer accumulator contents to M(X,Y), increment Y-register.
00000100	TAMZA	Transfer accumulator contents to M(X,Y), zero accumulator.
00100100	TAY	Transfer accumulator contents to Y-register.
001110 (B)	TBIT1	If bit I(B) of M(X,Y) is one, status = 1.
0100 (C)	TCY	Transfer I(C) field to Y-register.
0110 (C)	TCMIY	Transfer I(C) field to M(X,Y), increment Y-register.
00001010	TDO	Transfer status latch and **accumulator to PLA input register.**
00001000	TKA	Tranfer K-inputs to accumulator.
00100001	TMA	Transfer M(X,Y) to accumulator.
00100010	TMY	Transfer M(X,Y) to Y-register.
00100011	TYA	Transfer Y-register contents to accumulator.
00101110	XMA	Exchange contents of M(X,Y) and accumulator.
00000010	YNEA	If Y-register is not equal to accumulator, status and status latch = 1.
0101 (C)	YNEC	If Y-register is not equal to I(C) field, status = 1.

MOTOROLA

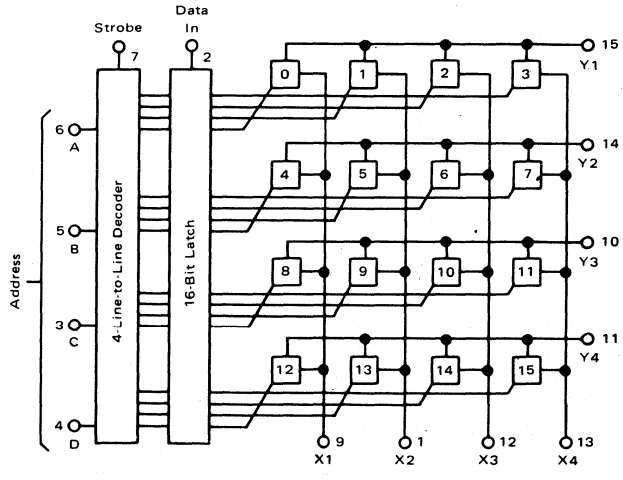
MC142100
MC145100

Product Preview

4 X 4 CROSSPOINT SWITCH WITH CONTROL MEMORY

The MC142100 and MC145100 consist of 16 crosspoint switches (analog transmission gates) organized in 4 rows and 4 columns. Both devices have 16 latches, each of which control the state of a particular switch. Any of the 16 switches can be selected by applying its address to the device and a pulse to the strobe input. The selected crosspoint will turn on if during strobe, Data In was a one and will turn off if during strobe, Data In was a zero. In addition the MC145100 will reset all non-selected switches in the same row as the selected switch. Other switches are unaffected. In both devices, an internal power-on reset disables all switches as power is applied.

- Internal Latches Control State of Switches
- Power-On Reset
- Low On Resistance – Typically on 100 Ω @ 10 Vdc
- Large Analog Range ± $V_{DD}/2$
- All Inputs Are Diode Protected
- Matched Switch Characteristics
- High CMOS Noise Immunity
- MC142100 Pin-for-Pin Replacement for CD22100

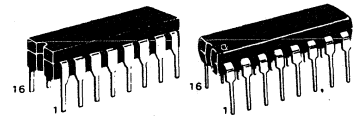


This is advance information and specifications are subject to change without notice.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4 X 4 CROSSPOINT SWITCH WITH CONTROL MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620

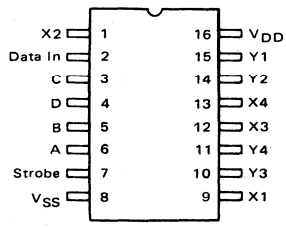
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXX

Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENTS



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range —	T_A		°C
AL Device		−55 to +125	
CL/CP Device		−40 to +85	
Storage Temperature Range	T_{stg}	−65 to +150	°C

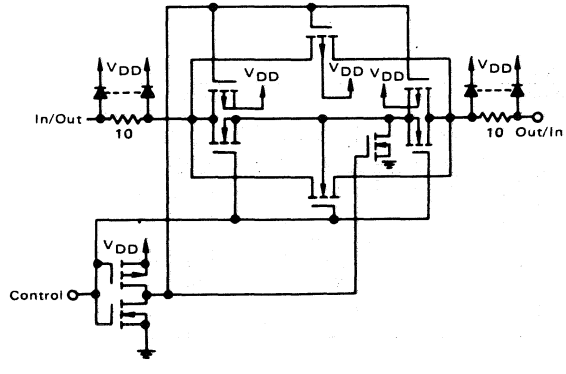
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

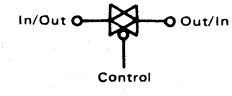
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Voltage (Logic) "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.9	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.75	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.25	–	11.25	8.25	–	11.25	–	
Input Current	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Input Capacitance (V_{in} = 0)	C_{in}									pF
Digital Inputs		–	–	–	–	5.0	–	–	–	
Switch Inputs		10	–	–	–	–	–	–	–	
Output Capacitance	C_{out}	10	–	–	–	–	–	–	–	pF
Feedthrough Capacitance	$C_{in/out}$	–	–	–	–	–	–	–	–	pF
Quiescent Current	I_Q	5.0	–	1.0	–	0.0005	1.0	–	7.5	Adc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
On-State Resistance	R_{on}	5.0	–	–	–	–	–	–	–	Ω
		10	–	–	–	–	–	–	–	
		15	–	–	–	–	–	–	–	
On-State Resistance Difference Between	ΔR_{on}	5.0	–	–	–	–	–	–	–	Ω
Any Two Switches		10	–	–	–	–	–	–	–	
		15	–	–	–	–	–	–	–	
Input/Output Leakage Current Switch Off	$I_{in/out}$	15	–	±300	–	±0.01	±300	–	±1000	nAdc

ANALOG TRANSMISSION GATE (CROSSPOINT) SCHEMATIC





SWITCHING CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Propagation Delay Times (V_{SS} = 0 Vdc) Input to Control (R_L = 10 kΩ)	t_{PLH}, t_{PHL}	5.0 10 15	– – –	– – –	– – –	ns
Strobe to Output Output "1" to High Impedance	t_{PHZ}	5.0 10 15	– – –	– – –	– – –	ns
Output "0" to High Impedance	t_{PLZ}	5.0 10 15	– – –	– – –	– – –	ns
High Impedance to Output "1"	t_{PZH}	5.0 10 15	– – –	– – –	– – –	ns
High Impedance to Output "0"	t_{PZL}	5.0 10 15	– – –	– – –	– – –	ns
Setup Time Address or Data In to Strobe	t_{su}	5.0 10 15	– –	– –	– –	ns
Hold Time Address or Data In to Strobe	t_h	5.0 10 15	This table lists all of the characteristics to be specified for this device. Final specifications were not available at the time of printing. For the latest data, contact CMOS Marketing, Motorola Semiconductor Products Inc., 3501 Ed Bluestein Blvd., Austin, Texas 78721.			ns
Strobe Pulse Width	t_{WH}	5.0 10 15				ns
Sine Wave Distortion (V_{SS} = –4.0 Vdc) (R_L = 10 kΩ, f = 1.0 kHz)	–	5.0 10 15				%
Frequency Response (Switch ON) V_{SS} = –5.0 Vdc (R_L = 1.0 kΩ, 20 $Log_{10} \frac{V_{out}}{V_{in}}$ = –3.0 dB)	–	5.0 10 15	– – –	– – –	– – –	MHz
Feedthrough Attenuation (Switch OFF) V_{SS} = –5.0 Vdc (R_L = 1.0 kΩ, 20 $Log_{10} \frac{V_{out}}{V_{in}}$ = –50 dB)	–	5.0 10 15	– – –	– – –	– – –	MHz
Crosstalk Between Any Two Switches V_{SS} = –5.0 Vdc (Switch A On, Switch B Off) (R_L = 1.0 kΩ, 20 $Log_{10} \frac{V_{out(B)}}{V_{in(A)}}$ = –50 dB	–	5.0 10 15	– – –	– – –	– – –	MHz

TRUTH TABLE

Address				Switch	MC145100 Only Switches			Address				Switch	MC145100 Only Switches		
A	B	C	D	Selected	Cleared			A	B	C	D	Selected	Cleared		
0	0	0	0	X1Y1	1	2	3	0	0	0	1	X1Y3	8	9	10	11
1	0	0	0	X2Y1	0	2	3	1	0	0	1	X2Y3	9	8	10	11
0	1	0	0	X3Y1	0	1	3	0	1	0	1	X3Y3	10	8	9	11
1	1	0	0	X4Y1	0	1	2	1	1	0	1	X4Y3	11	8	9	10
0	0	1	0	X1Y2	4	5	6	0	0	1	1	X1Y4	12	13	14	15
1	0	1	0	X2Y2	5	4	6	1	0	1	1	X2Y4	13	12	14	15
0	1	1	0	X3Y2	6	4	5	0	1	1	1	X3Y4	14	12	13	15
1	1	1	0	X4Y2	7	4	5	1	1	1	1	X4Y4	15	12	13	14

MOTOROLA

MCM145101

256 X 4 BIT STATIC RAM

The MCM145101 family of CMOS RAMs offers ultra low power and fully static operation with a single 5 volt supply. The CMOS 1024-bit devices are organized in 256 words by 4 bits. Separate data inputs and data outputs permit maximum flexibility in bus-oriented systems. Data retention at a power supply as low as 2.0 volts over temperature readily allows design into applications using battery backup for nonvolatility. The MCM145101 is fully static and does not require clocking in standby mode.

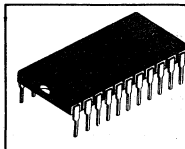
The MCM145101 is fabricated using the Motorola advanced ion-implanted, silicon-gate technology for high performance and high reliability.

- Low Standby Power
- Fast Access Time
- Single + 5.0 Volt Supply
- Fully TTL Compatible—All Inputs and Outputs
- Three-State Output
- Fully Static Operation
- Data Retention to 2.0 Volts
- Direct Replacement for:
  - Intel 5101 Series
  - AMI S5101 Series
  - Hitachi MH435101 Series
- Pin Replacement for Harris HM6501 Series

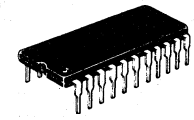
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

1024-BIT STATIC
RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 736



P SUFFIX
PLASTIC PACKAGE
CASE 708

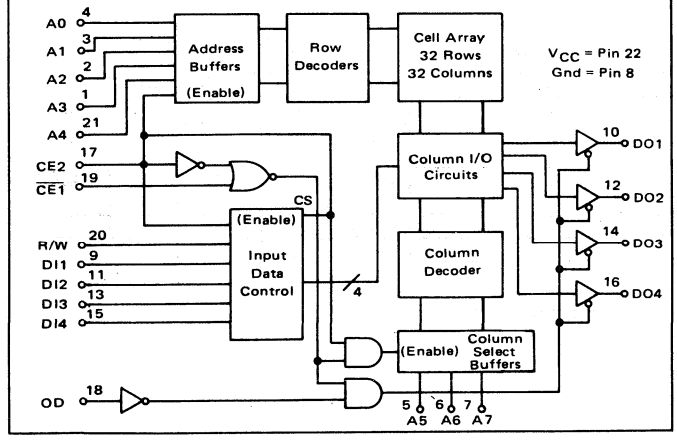
ORDERING INFORMATION

MCM14XXXX — Suffix Denotes
- L
- P
- -1
- -3
- -8
- (Not Used)

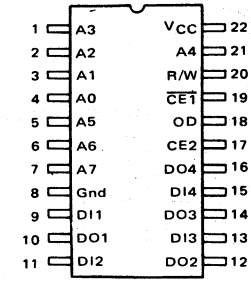
Selections for speed and power (see table)

Type Number	Typical Standby Current @ 2 Vdc (μA)	Typical Standby Current @ 5 Vdc (μA)	Max Access (ns)
MCM145101L, MCM145101P	0.14	0.2	650
MCM145101-1L, MCM145101-1P	0.14	0.2	450
MCM145101-3L, MCM145101-3P	0.70	1.0	650
MCM145101-8L, MCM145101-8P	—	10	800

BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

$\overline{CE1}$	CE2	OD	R/W	D_{In}	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D_{In}	Write
L	H	L	H	X	D_{Out}	Read

MAXIMUM RATINGS (Voltages referenced to V_{SS} Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Voltage on Any Pin	V_{in}	-0.3 to V_{CC} +0.3	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

DC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5 V ±5%)

Characteristic	Symbol	MCM145101,-1			MCM145101-3			MCM145101-8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Current	I_{in}(2)	–	5.0	–	–	5.0	–	–	5.0	–	nAdc
Input High Voltage	V_{IH}	2.2	–	V_{CC}	2.2	–	V_{CC}	2.2	–	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.65	-0.3	–	0.65	-0.3	–	0.65	Vdc
Output High Voltage (I_{OH} = -1.0 mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	Vdc
Output Leakage Current ($\overline{CE1}$ = 2.2 V, V_{OL} = 0 V to V_{CC})	I_{LO}(2)	–	–	±1.0	–	–	±1.0	–	–	±2.0	μAdc
Operating Current (V_{in} = V_{CC}, except $\overline{CE1}$ ≤ 0.65 V, outputs open)	I_{CC1}	–	9.0	22	–	9.0	22	–	11	25	mAdc
Operating Current (V_{in} = 2.2 V, except $\overline{CE1}$ ≤ 0.65 V, outputs open)	I_{CC2}	–	13	27	–	13	27	–	15	30	mAdc
Standby Current (CE2 ≤ 0.2 V)	I_{CCL}(2),(4)	–	–	10	–	–	200	–	–	500	μAdc

CAPACITANCE

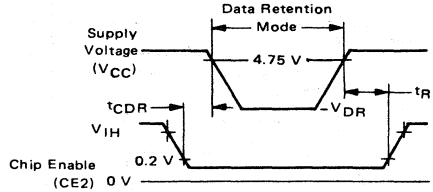
Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = O V)	C_{in}	4.0	8.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12.0	pF

LOW V_{CC} DATA RETENTION CHARACTERISTICS (Excluding MCM145101-8) T_A = 0°C to 70°C

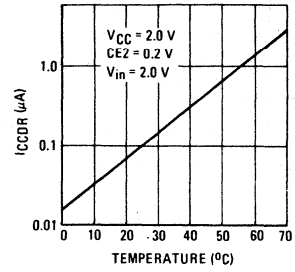
Parameter	Test Conditions		Symbol	Min	Typ.(1)	Max	Units
V_{CC} for Data Retention	CE2 ≤ 0.2 V		V_{DR}	2.0	–	–	Vdc
MCM145101 or MCM145101-1 Data Retention Current		V_{DR} = 2.0 V,	I_{CCDR1}	–	0.14	10	μAdc
MCM145101-3 Data Retention Current		V_{DR} = 2.0 V,	I_{CCDR2}	–	0.70	200	μAdc
Chip Deselect to Data Retention Time			t_{CDR}	0	–	–	ns
Operation Recovery Time			t_R	t_{RC}(3)	–	–	ns

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage.
2. Current through all inputs and outputs included in I_{CCL} measurement.
3. t_{RC} = Read Cycle Time.
4. Low current state is for CE2 = 0 only.

LOW V_{CC} DATA RETENTION WAVEFORM



TYPICAL I_{CCDR} versus TEMPERATURE



AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	+0.65 V to 2.2 V
Input Rise and Fall Times	20 ns
Output Load — 1 TTL Gate and C_L = 100 pF	
Timing Measurement Reference Level	1.5 Volt

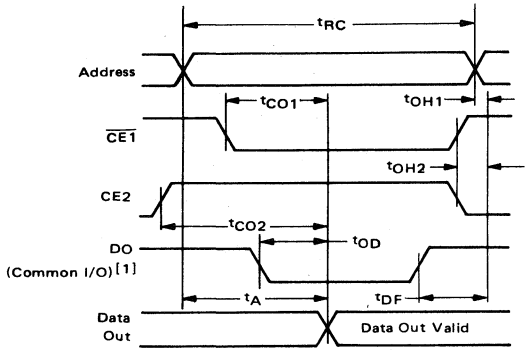
READ CYCLE

Parameter	Symbol	MCM145101-1		MCM145101,-3		MCM145101-8	
		Min	Max	Min	Max	Min	Max
Read Cycle	t_{RC}	450	–	650	–	800	–
Access Time	t_A	–	450	–	650	–	800
Chip Enable ($\overline{CE1}$) to Output	t_{CO1}	–	400	–	600	–	800
Chip Enable (CE2) to Output	t_{CO2}	–	500	–	700	–	850
Output Disable to Output	t_{OD}	–	250	–	350	–	450
Data Output to High Z State	t_{DF}	0	130	0	150	0	200
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0	–	0	–	0	0
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0	–	0	–	0	0

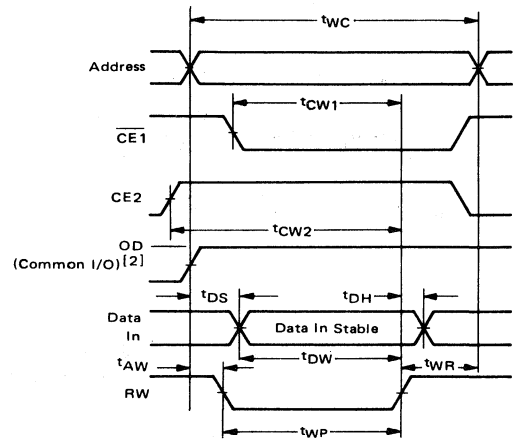
WRITE CYCLE

Write Cycle	t_{WC}	450	–	650	–	800	–
Write Delay	t_{AW}	130	–	150	–	200	–
Chip Enable ($\overline{CE1}$) to Write	t_{CW1}	350	–	550	–	650	–
Chip Enable (CE2) to Write	t_{CW2}	350	–	550	–	650	–
Data Setup	t_{DW}	250	–	400	–	450	–
Data Hold	t_{DH}	50	–	100	–	100	–
Write Pulse	t_{WP}	250	–	400	–	450	–
Write Recovery	t_{WR}	50	–	50	–	100	–
Output Disable Setup	t_{DS}	130	–	150	–	200	–

READ CYCLE TIMING



WRITE CYCLE TIMING



NOTES: 1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

MOTOROLA

MC145104
MC145106
MC145107
MC145109
MC145112

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PLL
FREQUENCY SYNTHESIZERS

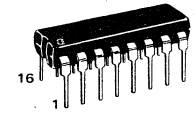
PLL FREQUENCY SYNTHESIZERS

The MC145104, MC145106, MC145107, MC145109, and MC145112 are phase locked loop (PLL) frequency synthesizer parts constructed with CMOS devices on a single monolithic structure. These synthesizers find applications in such areas as CB and FM transceivers. The device contains an oscillator/amplifier, a 2^{10} or 2^{11} divider chain for that oscillator signal, a programmable divider chain for the input signal and a phase detector. The MC145104/5106/5112 have circuitry for a 10.24 MHz oscillator or may operate with an external signal. The MC145107/5109 require the external reference signal. Several of the circuits provide a 5.12 MHz output signal, which can be used for frequency tripling. A 2^9 (MC145106/5109/5112) or 2^8 (MC145104/5107) programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground-to-supply binary signals. Pull-down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

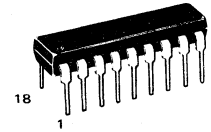
The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out of lock signal is provided from the on-chip lock detector with a "0" level for the out of lock condition.

The MC145106 is the full pinout version of this family of parts and has the capability of all parts in the family. The MC145104/5107/5109/5112 are limited pinout versions. See block diagrams for details.

- Single Power Supply
- Wide Supply Range: 4.5 to 12 Vdc
- 16 or 18 Pin Plastic Packages
- 10.24 MHz Oscillator on Chip
- 5.12 MHz Output
- Programmable Division Binary Input Selects up to 2^9
- On-Chip Pull Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 2^{10} or 2^{11}



P SUFFIX
PLASTIC PACKAGE
CASE 648



P SUFFIX
PLASTIC PACKAGE
CASE 707

Pin-for-Pin Replacements for:
MC145104 for SM5104, MM55104, MM55114
MC145106 for MM55106, MM55116
MC145107 for SM5107
MC145109 for SM5109
MC145112 for SM5106

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to + 12	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

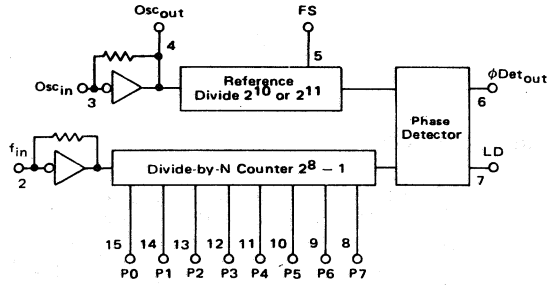
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out} \leq V_{DD}$.

RECOMMENDED OPERATION: DC Supply Voltage 4.5 to 12 Vdc

ELECTRICAL CHARACTERISTICS (T_A = 25° unless otherwise stated.)

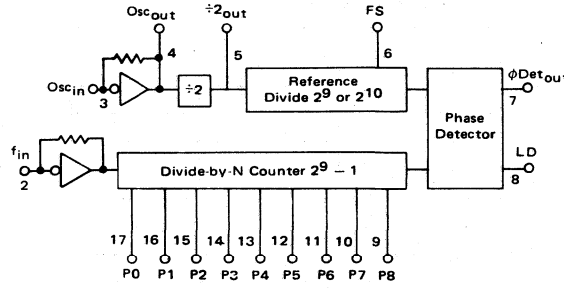
Characteristic		Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Supply Current		I_D	5.0	–	6	10	mAdc
			10	–	20	35	
			12	–	28	50	
Input Voltage	"0" Level	V_{IL}	5.0	–	–	1.5	Vdc
			10	–	–	3.0	
			12	–	–	3.6	
	"1" Level	V_{IH}	5.0	3.5	–	–	Vdc
			10	7.0	–	–	
			12	8.4	–	–	
Input Current (FS)	"0" Level	I_{in}	5.0	-5.0	-20	-50	μAdc
(Pull-up Resistor)			10	-15	-60	-150	
			12	-20	-80	-200	
(P0 to P8)			5.0	–	–	-0.3	
			10	–	–	-0.3	
			12	–	–	-0.3	
(FS)	"1" Level		5.0	–	–	0.3	μAdc
			10	–	–	0.3	
			12	–	–	0.3	
(P0 to P8)			5.0	7.5	30	75	
(Pull-down Resistor)			10	22.5	90	225	
			12	30	120	300	
(Osc_{in}, f_{in})	"0" Level		5.0	-2.0	-6.0	-15	μAdc
			10	-6.0	-25	-62	
			12	-9.0	-37	-92	
(Osc_{in}, f_{in})	"1" Level		5.0	2.0	6.0	15	
			10	6.0	25	62	
			12	9.0	37	92	
Output Drive Current		I_{OH}					mAdc
(V_O = 4.5 Vdc)	Source		5.0	-0.7	-1.4	–	
(V_O = 9.5 Vdc)			10	-1.1	-2.2	–	
(V_O = 11.5 Vdc)			12	-1.5	-3.0	–	
(V_O = 0.5 Vdc)	Sink	I_{OL}	5.0	0.9	1.8	–	mAdc
(V_O = 0.5 Vdc)			10	1.4	2.8	–	
(V_O = 0.5 Vdc)			12	2.0	4.0	–	
Input Amplitude		–					Vp-p
(f_{in} @ 4.0 MHz)			–	1.0	0.2	–	Sine
(Osc_{in} @ 10.24 MHz)			–	1.5	0.3		
Input Resistance		R_{in}					MΩ
(Osc_{in}, f_{in})			5.0	–	1.0	–	
			10	–	0.5	–	
			12	–	–	–	
Input Capacitance		C_{in}					pF
(Osc_{in}, f_{in})			–	–	6.0		
Three State Leakage Current		I_{TL}					μAdc
(ϕ Det_{out})			5.0	–	–	1.0	
			10	–	–	1.0	
			12	–	–	1.0	
Input Frequency		f_{in}	4.5	4.0	–	–	MHz
(-40°C to +85°C)			12	4.0	–	–	
Oscillator Frequency		Osc_{in}	4.5	10.24	–	–	MHz
(-40°C to +85°C)			12	10.24	–	–	

BLOCK DIAGRAMS



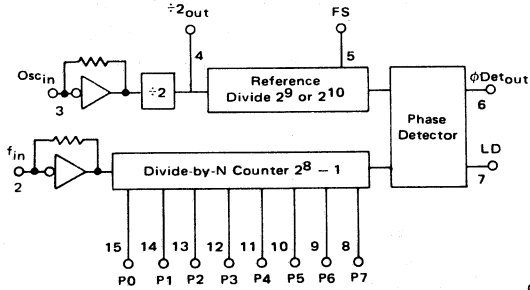
MC145104

V_{DD} = Pin 1
V_{SS} = Pin 16



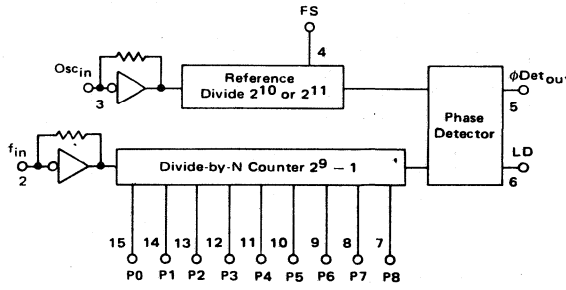
MC145106

V_{DD} = Pin 1
V_{SS} = Pin 18



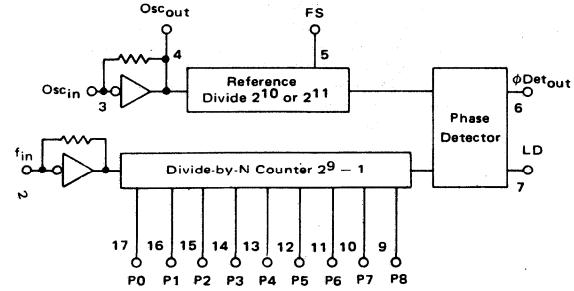
MC145107

V_{DD} = Pin 1
V_{SS} = Pin 16



MC145109

V_{DD} = Pin 1
V_{SS} = Pin 16



MC145112

N.C. = Pin 8
V_{DD} = Pin 1
V_{SS} = Pin 18

TYPICAL CHARACTERISTICS

FIGURE 1 – MAXIMUM DIVIDER INPUT FREQUENCY versus SUPPLY VOLTAGE

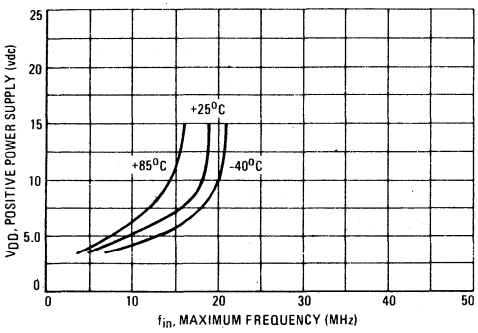
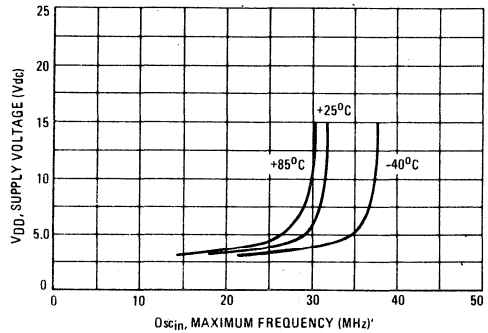


FIGURE 2 – MAXIMUM OSCILLATOR INPUT FREQUENCY versus SUPPLY VOLTAGE



TRUTH TABLE

Selection									
P8	P7	P6	P5	P4	P3	P2	P1	P0	Divide By N
0	0	0	0	0	0	0	0	0	2 } (Note 1)
0	0	0	0	0	0	0	0	1	3 } (Note 1)
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0	1	1	1	1	1	1	1	1	255
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	511

1: Voltage level = V_{DD}
0: Voltage level = 0 or open circuit input

Note 1: The binary setting of 00000000 and 00000001 on P8 to P0 results in a 2 and 3 division which is not in the 2^N-1 sequence. When pin is not connected (or is not listed as for the MC145104 and MC145107), the logic signal on that pin can be treated as a "0".

PIN DESCRIPTIONS

P0 – P8 – Programmable divider inputs (binary)
f_{in} – Frequency input to programmable divider (derived from VCO)
Osc_{in} – Oscillator/amplifier input terminal
Osc_{out} – Oscillator/amplifier output terminal
LD – Lock detector, low when out of lock
ϕ Det_{out} – Signal for control of external VCO, output high when f_{in}/N is less than the reference frequency; output low when f_{in}/N is greater than the reference frequency. Reference frequency is the divided down oscillator - input frequency typically 5.0 or 10 kHz.
FS – Reference Oscillator Frequency Division Select. When using 10.24 MHz Osc frequency, this control selects 10 kHz, a "0" selects 5.0 kHz.
$\div 2_{out}$ – Reference Osc frequency divided by 2 output; when using 10.24 MHz Osc frequency, this output is 5.12 MHz for frequency tripling applications.
V_{DD} – Positive power supply
V_{SS} – Ground

PLL SYNTHESIZER APPLICATIONS

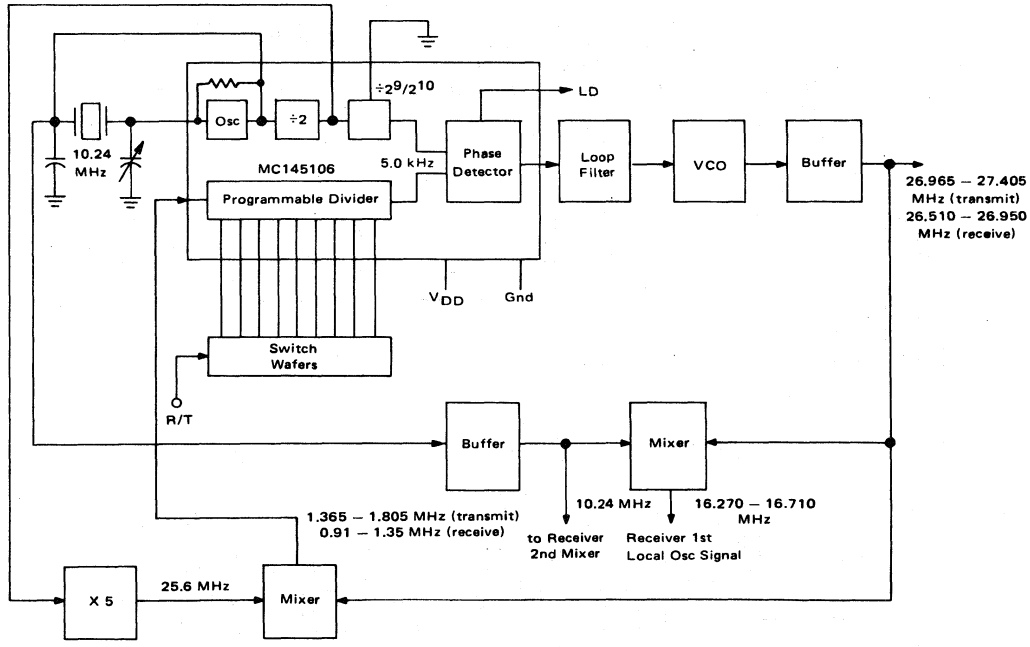
The MC145104, MC145106, MC145107, MC145109, MC145112 ICs are well suited for Applications in CB radios because of the channelized frequency requirements. A typical 40 channel CB transceiver synthesizer using a single crystal reference is shown in Figure 3 for receiver IF values of 10.695 MHz and 455 kHz.

In addition to applications in CB radios, the MC145104-12 ICs can be used as a synthesizer for several other systems. Various frequency spectrums can be achieved through the use of proper offset, prescaling and loop programming techniques. In general, 300-400 channels can be synthesized using a single loop, with many additional channels available when multiple loop approaches are employed. Figures 4 and 5 are examples of some possibilities.

In the aircraft syntheizer of Figure 5, the VHF loop (top) will provide a 50 kHz 360 channel system with 10.7 MHz R/T offset when only the 11.0500 MHz (transmit) and 12.1200 MHz (receive) frequencies are provided to mixer #1. When these signals are provided with crystal oscillators, the result is a three crystal, 360 channel, 50 kHz step synthesizer. When using the offset loop (bottom) in Figure 5 to provide the indicated injection frequencies for mixer #1 (two for transmit and two for receive) 360 additional channels are possible. This results in a 720 channel, 25 kHz step synthesizer which requires only two crystals and provides R/T offset capability. The receive offset value is determined by the 11.31 MHz crystal frequency and is 10.7 MHz for the example.

The VHF marine synthesizer in Figure 4 depicts a single loop approach for FM transceivers. The VCO operates on-frequency during transmit and is offset downward during receive. The offset corresponds to the receiver I F (10.7 MHz) for channels having identical receive/transmit frequencies (simplex), and is (10.7 – 4.6 = 6.1) MHz for duplex channels. Carrier modulation is introduced in the loop during transmit.

FIGURE 3 – SINGLE CRYSTAL CB SYNTHESIZER FEATURING ON-FREQUENCY VCO DURING TRANSMIT



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

FIGURE 4 – VHF MARINE TRANSCEIVER SYNTHESIZER

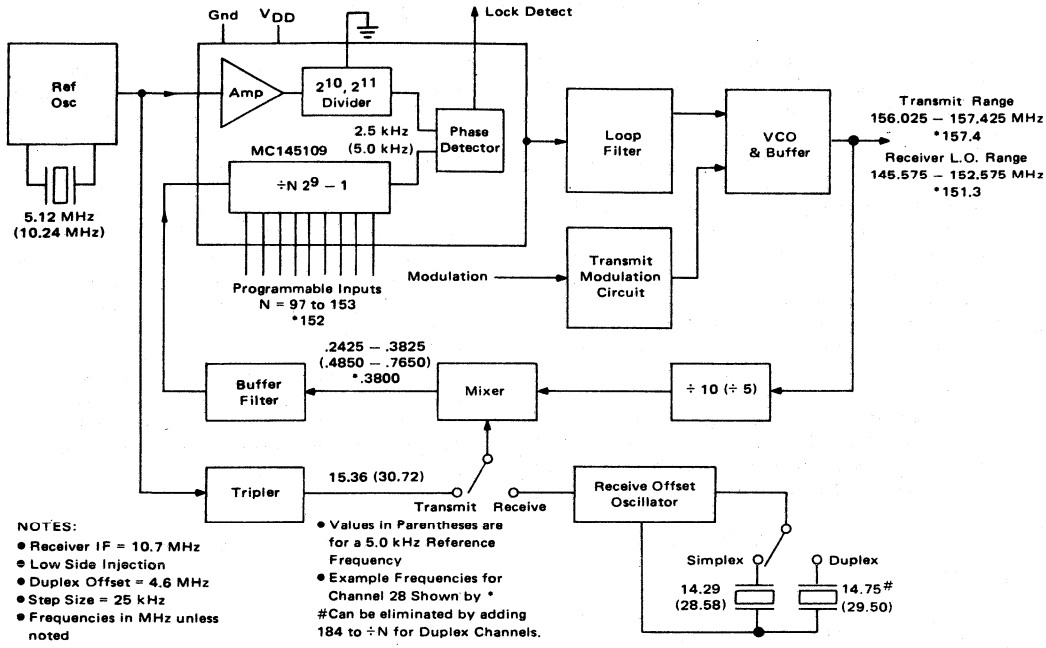
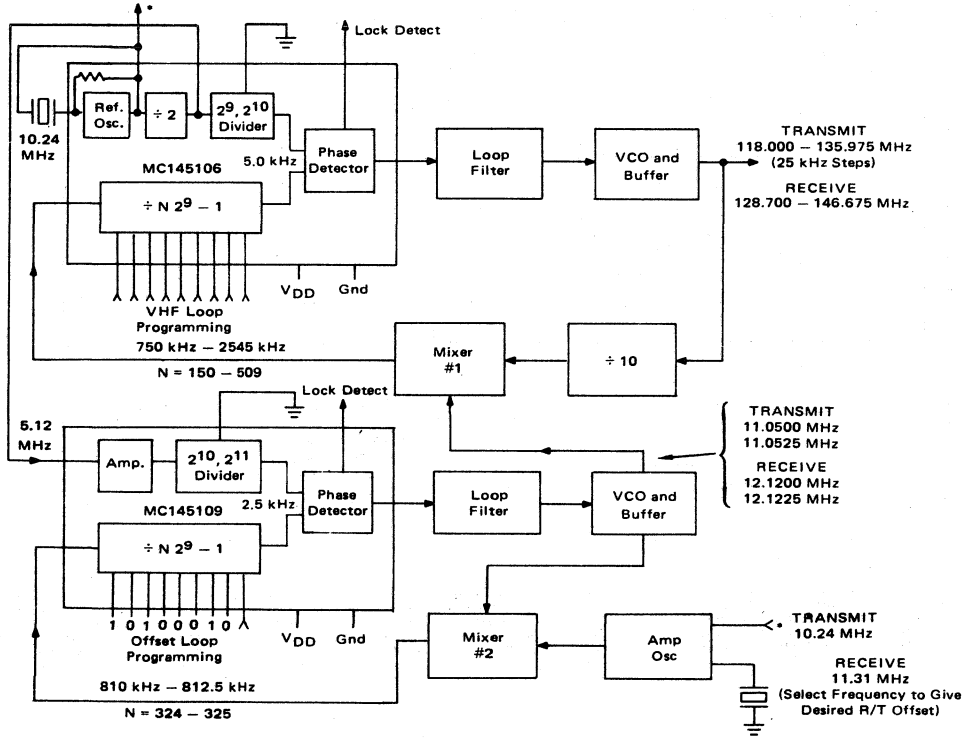


FIGURE 5 – VHF AIRCRAFT 720 CHANNEL TWO CRYSTAL FREQUENCY SYNTHESIZER



MOTOROLA

MCM146504

Product Preview

4096X1-BIT STATIC RANDOM ACCESS MEMORIES

The MCM146504 is a 4096X1-bit static random access memory, fabricated with high density, high reliability CMOS silicon-gate technology. The device has TTL compatible inputs and outputs. It is designed to retain data at low supply voltages, to further reduce supply current requirements.

The MCM146504 is useful in memory applications where low-power and non-volatility is required. It is assembled in 18 pin dual in-line package with the industry standard pin-outs.

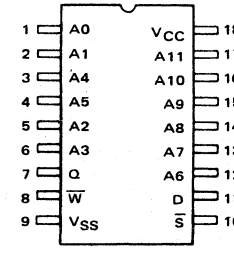
- Single Low Voltage Power Supply
- Static Operation
- Industry Standard 18-Pin Configuration
- Fully TTL Compatible
- Common Data Input and Output Capability
- Three-State Outputs
- Low Power Dissipation – Standby 10 mW (Typical)
- Ideal for Battery Backup Operation
- Access Time – 450 ns (Maximum)
- Pinout and Functional Replacement for
  Harris – HM6504
  Intersil – IM6504

CMOS LSI

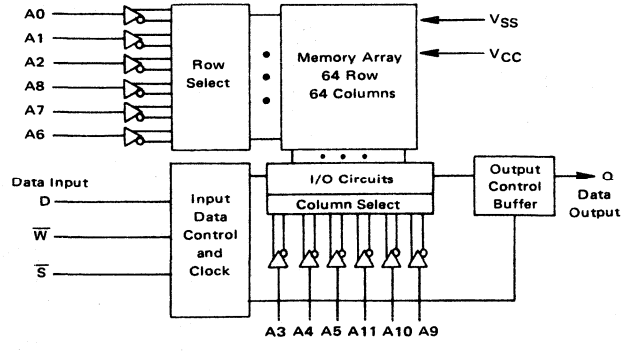
(LOW-POWER COMPLEMENTARY MOS)

4096X1-BIT STATIC RANDOM ACCESS MEMORIES

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0–A11	Address Input
D	Data Input
Q	Data Output
$\overline{S}$	Chip Select
V_{CC}	Power Supply (+5 V)
V_{SS}	Ground
$\overline{W}$	Write Enable

TRUTH TABLE

$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	HI-Z	Not Selected
L	L	L	HI-Z	Write "0"
L	L	H	HI-Z	Write "1"
L	H	X	Output data	Read

This is advance information and specifications are subject to change without notice.

MOTOROLA

MCM146508
MCM146518

Advance Information

1024 X 1 BIT STATIC RANDOM ADDRESS MEMORY

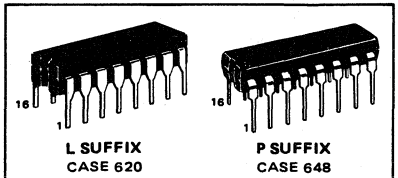
The MCM146508 and MCM146518 are fully static 1024 X 1 RAMS fabricated using high performance silicon gate CMOS technology. They offer low-power operation from a single 5.0 V supply with data retention to 2.0 V. The MCM146508 has the two select lines and the enable line brought out as a single enable line.

- Low Standby and Operating Power
- Single 5.0 V Supply
- Data Retention to 2.0 V
- Fast Access Time
- Address Latches
- Three-State Outputs
- Fully TTL Compatible Inputs/Outputs
- Fully Static Operation
- Direct Replacement for
  Harris HM6508/HM6518
  Intersil IM6508/IM6518

CMOS LSI

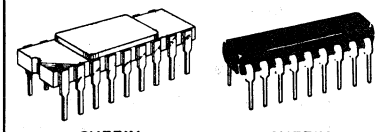
(LOW-POWER COMPLEMENTARY MOS)

1024 X 1 BIT STATIC RANDOM ACCESS MEMORY



L SUFFIX
CASE 620

P SUFFIX
CASE 648



L SUFFIX
CASE 680

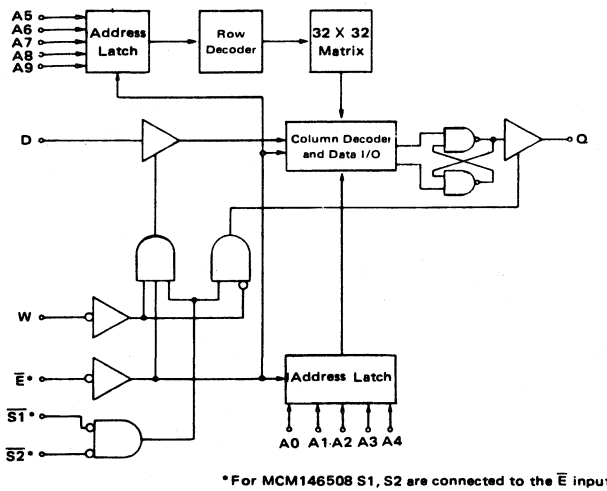
P SUFFIX
CASE 707

MCM14XXXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- See Table 1

TABLE 1

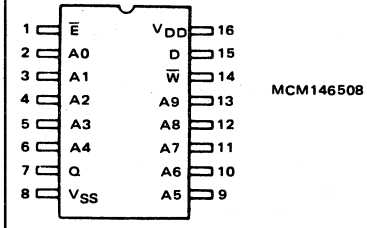
Type Number	Package Suffixes	Typical Current 2 Vdc	Typical Current 5 Vdc	Maximum Access Time	Operating Temperature Range
MCM146508/MCM146518	L/P	0.1 μA	5.0 μA	460 ns	-40 to +85°C
MCM146508-1/MCM146518-1	L/P	0.01 μA	1.0 μA	300 ns	-40 to +85°C
MCM146508-2/MCM146518-2	L	0.01 μA	1.0 μA	300 ns	-55 to +125°C

BLOCK DIAGRAM

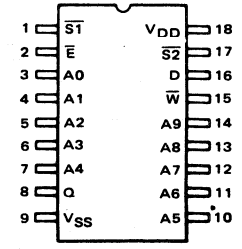


*For MCM146508 S1, S2 are connected to the $\overline{E}$ input.

PIN ASSIGNMENT



MCM146508



MCM146518

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +7.0	Vdc
Input Voltage, All Inputs	V_{in}	−0.3 to V_{DD} + 0.3	Vdc
Operating Temperature Range MCM146508/MCM146518 MCM146508-1/MCM146518-1 MCM146508-2/MCM146518-2	T_A	 −40 to +85 −40 to +85 −55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

DC CHARACTERISTICS (V_{DD} = 5.0 V ±10%, T_A = 25°C)

Characteristic	Symbol	MCM146508-1 MCM146518-1			MCM146508 MCM146518			MCM146508-2 MCM146518-2			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Current	I_{in}	–	5.0	–	–	5.0	–	–	5.0	–	nAdc
Input High Voltage	V_{IH}	V_{DD} − 2.0	–	V_{DD}	V_{DD} − 2.0	–	V_{DD}	–	–	V_{DD}	Vdc
Input Low Voltage	V_{IL}	−0.3	–	0.8	−0.3	–	0.8	−0.3	–	0.8	Vdc
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	Vdc
Output Leakage Current (V_{OL} = 0 V to V_{DD})	I_{OL}	–	–	±1.0	–	–	±1.0	–	–	±1.0	μAdc
Standby Current (V_{IH} = $\overline{E}$ = $\overline{S1}$ = $\overline{S2}$ = V_{DD})	I_{DDSB}	–	0.1	10	–	1.0	100	–	1.0	100	nAdc
Data Retention Current (V_{DD} = 2.2 V = V_{IH} = $\overline{E}$ = $\overline{S1}$ = $\overline{S2}$)	I_{DDDR}	–	0.1	1.0	–	0.1	10	–	0.1	10	μAdc
Operating Current (t_{ELEH} = 1.0 μs)	I_{DDOP}	–	–	–	–	–	–	–	–	–	mAdc

CAPACITANCE

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	8.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

AC OPERATING CONDITIONS

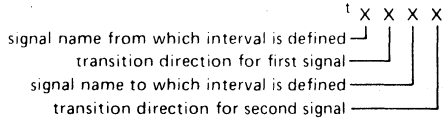
Condition	Value
Input Pulse Levels	+0.8 V to V_{DD} − 2.0 V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and C_L = 50 pF
Timing Measurement Reference Level	1.5 V
Supply Voltage	5.0 V ±10%
Temperature Range MCM146508/MCM146518 MCM146508-1/MCM146518-1 MCM146508-2/MCM146518-2	 −40°C to +85°C −40°C to +85°C −55°C to +125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

AC CHARACTERISTICS

Parameter	Symbol	MCM146508-1 MCM146518-1		MCM146508-2 MCM146518-2		MCM146508 MCM146518		Unit
		Min	Max	Min	Max	Min	Max	
Read or Write Cycle Time	t_{ELEL}	500	–	500	–	760	–	ns
Enable Pulse Width, Low	t_{ELEH}	300	–	300	–	460	–	ns
Enable Pulse Width, High	t_{EHEL}	200	–	200	–	300	–	ns
Enable Access Time	t_{ELQV}	–	300	–	300	–	460	ns
Address Setup	t_{AVEL}	7.0	–	7.0	–	15	–	ns
Address Hold	t_{ELAX}	90	–	90	–	150	–	ns
Data Setup	t_{DVWH}	200	–	200	–	300	–	ns
Data Hold	t_{WHDX}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WLWH}	200	–	200	–	300	–	ns
Write Enable to Output Disable	t_{WLQZ}	–	180	–	180	–	285	ns
Output Disable (MC146508 Only)	t_{EHQZ}	–	180	–	180	–	285	ns
Output Disable (MC146518 Only)	t_{SHQZ}	–	180	–	180	–	285	ns
Write Disable to Output Enable	t_{WHQX}	–	180	–	180	–	285	ns
Output Enable (MC146508 Only)	t_{ELQX}	–	180	–	180	–	285	ns
Output Enable (MC146518 Only)	t_{SLQX}	–	180	–	180	–	285	ns
Select to Write Pulse Setup	t_{WLSH}	200	–	200	–	300	–	ns
Select to Write Pulse Hold	t_{SLWH}	200	–	200	–	300	–	ns
Enable to Write Pulse Setup	t_{WLEH}	200	–	200	–	300	–	ns
Enable to Write Pulse Hold	t_{ELWH}	200	–	200	–	300	–	ns

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:

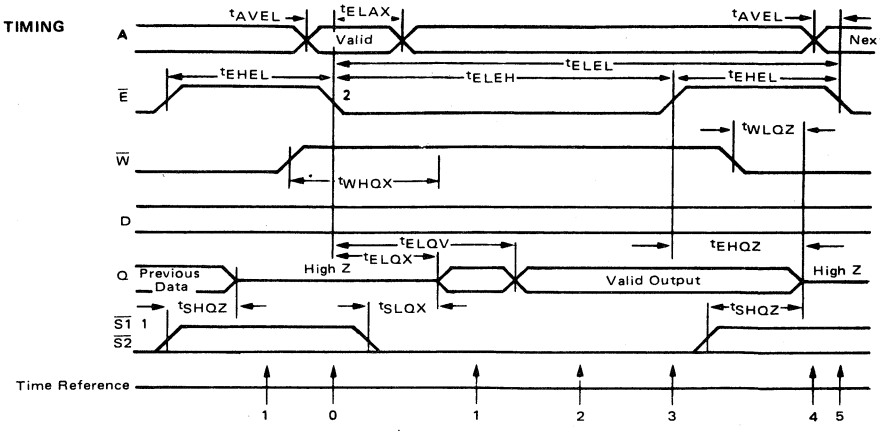
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

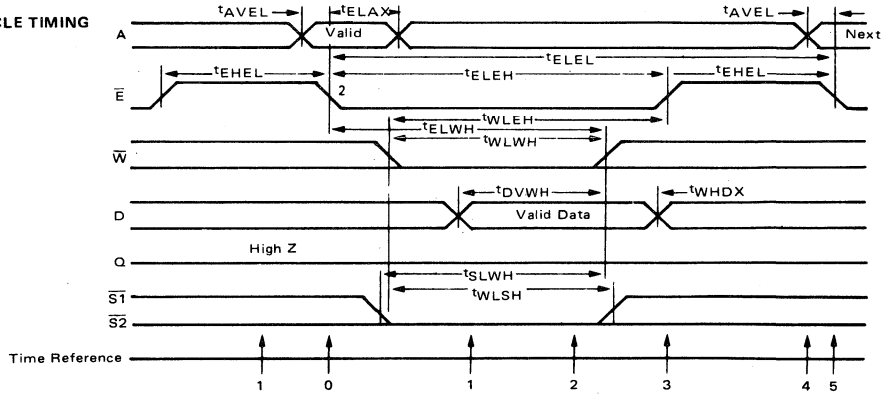
READ CYCLE TIMING



TRUTH TABLE

Time Reference	Inputs $\overline{E}$	$\overline{S}$	$\overline{W}$	A	D	Output Q	Function
-1	H	H	X	X	X	Z	Disabled
0	↓	X	H	V	X	Z	Address Latched
1	L	L	H	X	X	X	Output Enabled
2	L	L	H	X	X	V	Output Valid
3	↑	L	H	X	X	V	Output Latched
4	H	H	X	X	X	Z	Disabled (Same as -1)
5	↓	X	H	V	X	Z	Next Cycle (Same as 0)

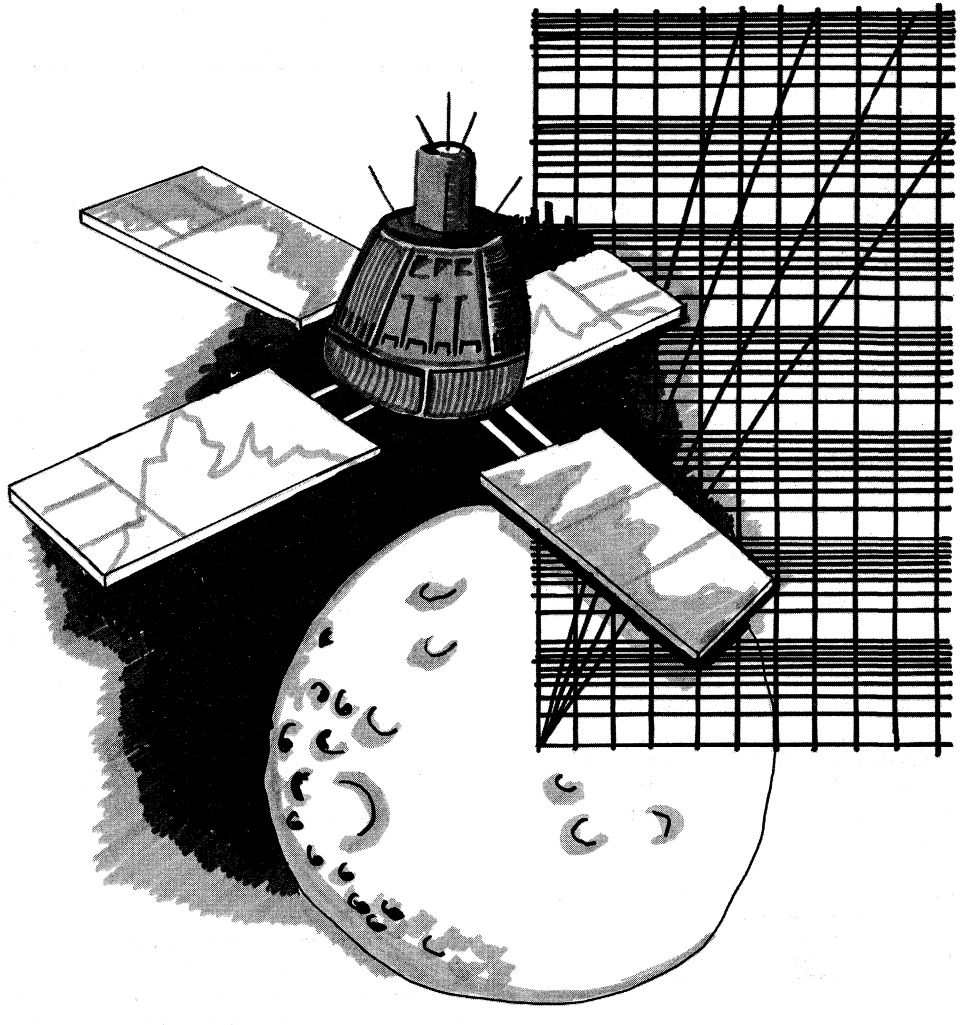
WRITE CYCLE TIMING



TRUTH TABLE

Time Reference	Inputs $\overline{E}$	$\overline{S}$	$\overline{W}$	A	D	Output Q	Function
-1	H	X	X	X	X	Z	Disabled
0	↓	X	X	V	X	Z	Address Latched
1	L	L	L	X	V	Z	Write Mode
2	L	↑	L	X	V	Z	Data Written
3	↑	X	X	X	X	Z	Write Completed
4	H	X	X	X	X	Z	Disabled (Same as -1)
5	↓	X	X	V	X	Z	Next Cycle (Same as 0)

NOTES:
1. MCM146518 selected only if both $\overline{S1}$ and $\overline{S2}$ are low and deselected if either $\overline{S1}$ or $\overline{S2}$ is high. $\overline{S1}$ and $\overline{S2}$ are connected to $\overline{E}$ on the MCM146508.
2. The address within the memory will change only on falling $\overline{E}$.



CMOS reliability 10

CHAPTER 8 – CMOS RELIABILITY AND QUALITY CONTROL

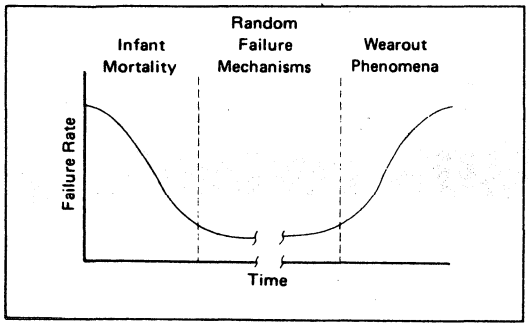
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Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of trouble-free service it can offer. The reliability of a device is exactly that – an expression of how well it will serve the customer.

BASIC CONCEPTS

It is essential to begin with an explanation of the various parameters of reliability. These are probably summarized best in the Bathtub Curve (Figure 1). The reliability of a device is characterized by three phases: infant mortality, random failure and wearout. When a device is produced there is often a small distribution of failure mechanisms which will exhibit themselves under relatively moderate stress levels and therefore appear early. This period of early failures, termed infant mortality, can often be reduced significantly through proper manufacturing controls and screening techniques. The most effective period is that in which only occasional random failure mechanisms appear. This typically spans a long period of time with a very low failure rate. The final period is that in which the devices literally wear out due to continuous phenomena which existed at the time of manufacture. Using reasonable design techniques and selectivity in applications this period can easily be extended beyond the lifetime required by the user.

FIGURE 1 – THE BATHTUB CURVE



Random Failure

During this time the probability of having no failures to a specific point in time can be expressed by the equation:

$$P(t) = e - \lambda t$$

where λ is the failure rate and t is time. Since λ is changing rapidly during infant mortality, the expression does not become useful until the random period, where λ is relatively constant. In this equation λ is failures per unit of time. It is usually expressed in percent failures per thousand hours. Other forms include FIT (Failures in Time = [(%/10^3 hrs] x 10^{-4} = 10^{-9} failures per hour) and MTTF (Mean Time To Failure) or MTBF (Mean Time Between Failures), both being equal to $1/\lambda$ and having units of hours.

Since reliability evaluations usually involve only samples of an entire population of devices, a point estimation for λ is calculated using the χ^2 distribution through the equation:

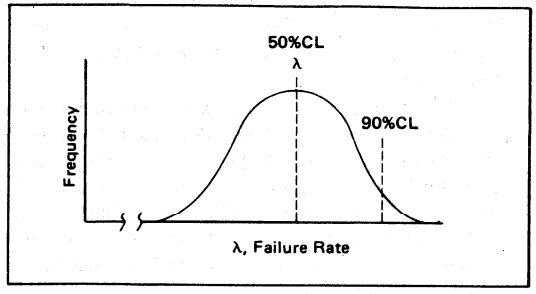
$$\lambda \leq \frac{\chi^2\ (\alpha,\ 2r + 2)}{2nt}$$

$$\text{Where } \alpha = \frac{100 - CL}{100}$$

CL = Confidence Limit in percent
r = Number of rejects
n = Number of devices
t = Duration of test

The confidence limit is the degree of conservatism desired in the calculation. The Central Limit Theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 2). The term (2r + 2) is called the degrees of freedom and is an expression of the number of rejects in a form suitable to χ^2 tables.

FIGURE 2 – CONFIDENCE LIMITS AND THE DISTRIBUTION OF SAMPLE FAILURE RATES



The number of rejects is a critical factor since the definition of rejects often differs between manufacturers. While Motorola uses data sheet limits to determine failures, sometimes rejects are counted only if they are catastrophic. Due to the increasing chance of a test not being representative of the entire population as sample size and test time are decreased, the X^2 calculation produces surprisingly high values of λ for short test durations even though the true long-term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long-term failure rate. Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing has shown that temperature will accelerate failures and that this behaviour fits the form of the Arrhenius equation:

$$R(t,T) = R_0(t)e^{-\theta/kT}$$

where $R(t,T)$ = Reaction rate as a function of time and temperature

R_0 = A constant with respect to temperature

t = Time

θ = Activation energy in electron volts

k = Boltzman's constant

T = Temperature in degrees Kelvin

To provide time-temperature equivalents this equation is applied to failure rate calculations in the form

$$t = t_0 e^{\theta/kT}$$

where

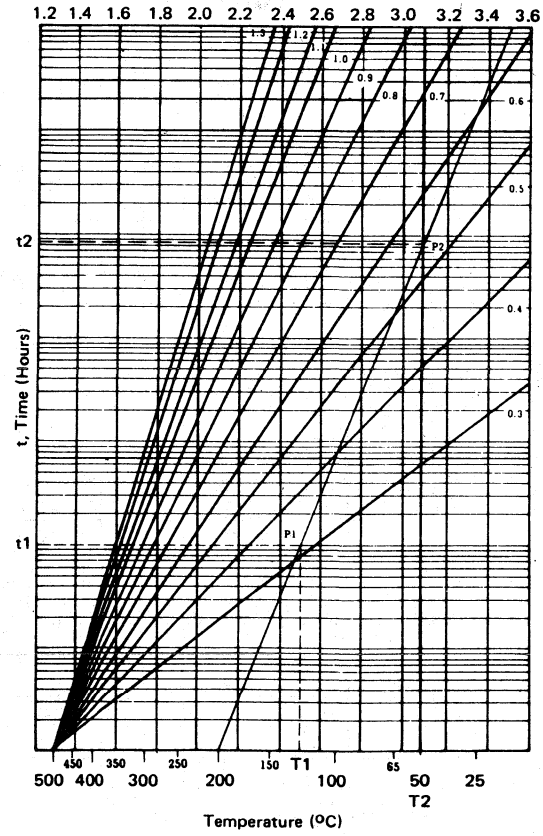
t = Time

t_0 = A constant.

The Arrhenius equation states that reaction rate increases with temperature. This produces a straight line when plotted on log-linear paper with a slope expressed by θ. θ may be physically interpreted as the energy threshold of a particular reaction or failure mechanism.

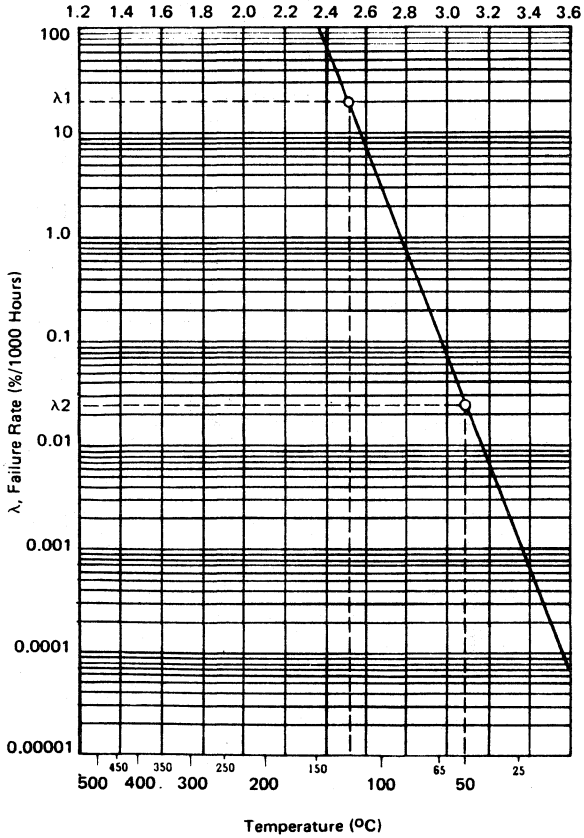
The activation energy exhibited by CMOS integrated circuits varies from about 0.7 eV for serious contamination problems to about 1.3 eV. Although the relationships do not prohibit devices from having poor failure rates and high activation energies, good performance often implies a high θ. Studies by Bell Telephone Laboratories have indicated that an overall θ for semiconductors is 1.0 eV. This value has been accepted by the Rome Air Development Command for time-temperature acceleration in life testing specified in Method 1005.1 of MIL-STD-883A. Data taken by McDonnell Douglas and Motorola on CMOS devices has verified this number and it is therefore applied as our standard time-temperature regression for extrapolation of high temperature failure rates to temperatures at which the devices will be used.

FIGURE 3 – NORMALIZED TIME-TEMPERATURE REGRESSIONS FOR VARIOUS ACTIVATION ENERGY VALUES



The Arrhenius relationship can be used to determine the failure rate at temperatures other than the test temperature of the device. (Figure 3 is a log-normal plot generated by the Arrhenius equation.) To accomplish this, the time in device hours (t1) and temperature (T1) of the test are plotted as point P1. A vertical line is drawn at the temperature of interest (T2) and a line with a 1.0 eV slope is drawn through point P1. Its intersection with the vertical line defines point P2, and determines the number of equivalent device hours (t2). This number may then be used with the χ^2 formula to determine the failure rate at the temperature of interest. Assuming T1 of 125°C at t1 of 10,000 hours, a t2 of 8.8 million hours results in a T2 of 50°C. If one failure occurs in the 10,000 device hours of testing at 125°C, the failure rate at that temperature will be 20%/1000 hours using a 60% confidence level. One failure in the equivalent 8.8 million device hours at 50°C will result in a 0.023%/1000 hour failure rate, as illustrated by Figure 4.

FIGURE 4 – FAILURE RATE



For increased flexibility in working with a broad range o device hours, the time-temperature regression lines hav been normalized to 500°C and the time scale omitte permitting the user to define the scale based on his ow requirements.

Three parameters determine the failure rate quoted b the manufacturer: the failure rate at the test temperatur the activation energy employed, and the differenc between the test temperature and the temperature of the quoted λ. A term often used in this manipulation is the "acceleration factor" which is simply the equivalent device hours at the lower temperature divided by the actual test device hours.

Wearout

Every device will eventually fail, but with reasonable care in design and application the wearout phase can be extended well beyond the lifetime required. During wearout, as in infant mortality, the failure rate is changing rapidly. The parameter used to describe performance in this area is "Median Life" and is the point at which 50% of the devices have failed. There are currently only two significant wearout mechanisms: electromigration of circuit metallization and electrolytic corrosion in plastic devices.

Electromigration is the current induced mass transport of metallization due to high temperature and current density. It is strongly affected by the type of metallization as well as the grain structure and surface sealing. It is therefore important that the designer predict the maximum junction temperature of the device, the current on all space limited lines and the process characteristics such as thickness variation, grain size, and step coverage. With these parameters fixed, a median life goal can be selected and the metal width chosen accordingly. Reasonable consideration in the design phase, coupled with careful die inspection, can therefore eliminate this phenomena as one of practical concern. Extended life time testing to thousands of hours at 125 °C and 15 V has verified this.

A more pertinent mechanism is the electrolytic corrosion of die metallization by moisture and applied voltage. Although it can occur in hermetic packages which are not properly sealed, hermeticity testing can easily prevent it. Adequate control of the plastic process will also provide a device which performs well under a wide range of normal environments.

Sampling Procedures

There are primarily three methods of measuring how well a lot of product meets the quality and reliability requirements of the customer; 100% testing using a Percent Defective Allowable (PDA), sampling based on an Acceptable Quality Level (AQL), and sampling based on a Lot Tolerance Percent Defective (LTPD). Since 100% testing is time consuming and expensive, sampling procedures are typically employed to assure acceptably low defect

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levels.

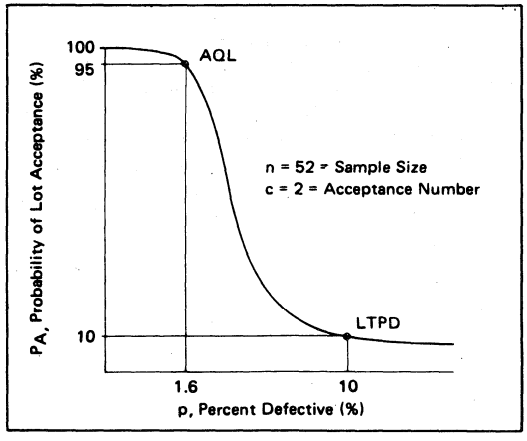
A PDA is simply a reject percentage above which the lot will be rejected. Depending on how the PDA was derived, it may or may not be statistically sound. The availability of theoretically accurate sampling plans in the various military specifications has led to wide use of AQL and LTPD plans. Depending on lot size and sample size, three different probability distributions may be used to derive the sampling plan: the Binomial, the Hypergeometric and the Poisson. The assumptions of a particular sample size (n) and acceptance number (c) and the use of these distributions will generate an Operating Characteristic (OC) Curve as shown in Figure 5. The AQL is defined at the 95% probability of lot acceptance level while the LTPD is defined at the 10% level. The AQL point describes the Producer's Risk of rejecting a good lot (5%) while the LTPD point describes the Consumer's Risk of accepting a bad lot (10%) given that the incoming product contains the percent defective p.

It is important to remember that although the concepts of Producer's and Consumer's Risk are utilized to describe AQLs and LTPDs, both are merely indicators of the performance of the original population. Both plans are widely used by manufacturers and users alike. By definition, LTPDs employ fixed sample sizes while AQL plans adjust the sample size according to the lot size. As in the case of failure rate determination, the criteria established to determine rejects and their interpretation are key factors in determining the performance of lots during inspection.

THE SOURCE OF RELIABILITY

One of the most popular sayings about reliability is that it must be "built in," not "tested in." Every manufacturing process exhibits a distribution of quality and reliability. The intent of the saying is that this distribution must be controlled to assure a high mean value, a narrow range and a consistent shape. Through proper design and process control this can be accomplished, thereby reducing the task of screening programs which attempt to eliminate the lower tail of the distribution.

FIGURE 5 – OPERATING CHARACTERISTIC CURVE



Design

A close interface must be maintained between reliability and design. For this reason a large part of the reliability effort is dedicated to a day by day interface with the device design and processing groups. Through this mutual effort new techniques are evaluated and proven before they are committed to production. Special test vehicles are generated and experiments performed to verify that the performance of new approaches meets or exceeds the standards of the product line. This effort is not only a beneficial application of reliability principles but an absolute necessity to provide the rapid product development demanded by the dynamic integrated circuit marketplace.

Processing

In addition to the design interface, reliability engineers work closely with process engineers in both the wafer and assembly areas. As each new process is developed, it is also tested to assure that it presents no hazards to the reliability of the ultimate product. This testing is an extensive qualification program which is performed independently on processes, packages and designs.

New wafer processes are qualified using prototypes of production devices. Each new package is tested using methods based on MIL-STD-883. Assembly process changes are qualified by employing them in the construction and testing of well-characterized products. After these primary level qualifications, wafer processes are generically qualified in new packaging systems to assure process-package compatibility. While assembly-oriented qualifications center around the thermal-mechanical sequences of MIL-STD-883, wafer process qualifications emphasize high temperature and voltage stress testing (See Figures 6 and 7).

After testing has proven the performance of the process, it is specified and documented to provide a baseline for process control. Beyond the detailed process control efforts of the process engineering groups, an In-Process Quality Control (IPQC) group exists to assure that process control is meeting its objectives. IPQC accomplishes this through surveillance of both the wafer and assembly areas (see Figure 8). There are two major inspection points in the wafer processing areas: CV Plotting and Final Visual. Samples from each wafer lot are stringently tested for voltage shift and inspected for gold backing and visual defects. The three major inspection points in the Assembly Area are Die High Power, Die Bond-Wire Bond and Pre-Cap.

FIGURE 6 – TYPICAL PACKAGE TESTS PER PACKAGE QUALIFICATION PROGRAM PLAN-REPORT 7639-2A

Test	MIL-STD-883 Test Method	Test Condition
Operating Life	1005	N/A
High Temperature Storage	N/A	150°C
Temperature Cycle	1010	C
Thermal Shock	1011	C
Thermal Resistance	N/A	N/A
Mechanical Shock	2002	B
Constant Acceleration	2001	E
Vibration, Variable Frequency	2007	A
Wire Pull (Hermetic)	2011	D
Temperature-Humidity-Bias (Plastic)	N/A	85°C/85% RH/10V
Moisture Resistance	1004	Unbiased
Salt Atmosphere	1009	A
Solderability	2003	260°C
Lead Fatigue	2004	B2
Marking Permanency	2015	N/A
Physical Dimensions	2016	N/A

All of these inspection points are known as "Gate Inspections" and are performed on lots of material. Wafers are grouped into lots which generally consist of thirty to fifty wafers while individual devices are grouped into assembly orders consisting of 500 to 2000 devices. Each lot or assembly order is submitted to In-Process Quality Assurance Gate Inspection. If accepted, they are passed to the next operation, while failed material is returned to Production for 100% screening. Only the wafers or devices that meet all established standards are accepted for continued processing.

"Monitor" inspections are performed in the assembly area on each individual machine and operator. The monitors are designed to control the operation, and provide feedback of quality problems to the responsible production supervision. Periodic line audits are used to check for:

1. Documented procedures on each operation
2. Proper usage of specifications
3. Up-to-date calibration of equipment
4. Proper settings on equipment
5. Housekeeping
6. Safety precautions.

In addition to product-oriented surveillance, all incoming materials, including wafers, mask, chemicals, piece parts and molding compounds, are inspected prior to use. Each supplier is qualified through the joint efforts of Incoming Quality Control and Reliability Engineering, and continuously rated to assure consistency.

Comprehensive training programs are provided for all domestic and off-shore personnel, new plant start-ups, changes in specifications, or process changes. The primary objective is to evaluate the material in process and assure that CMOS products meet the levels of reliability and quality which are consistent with the requirements of our customers.

SCREENING

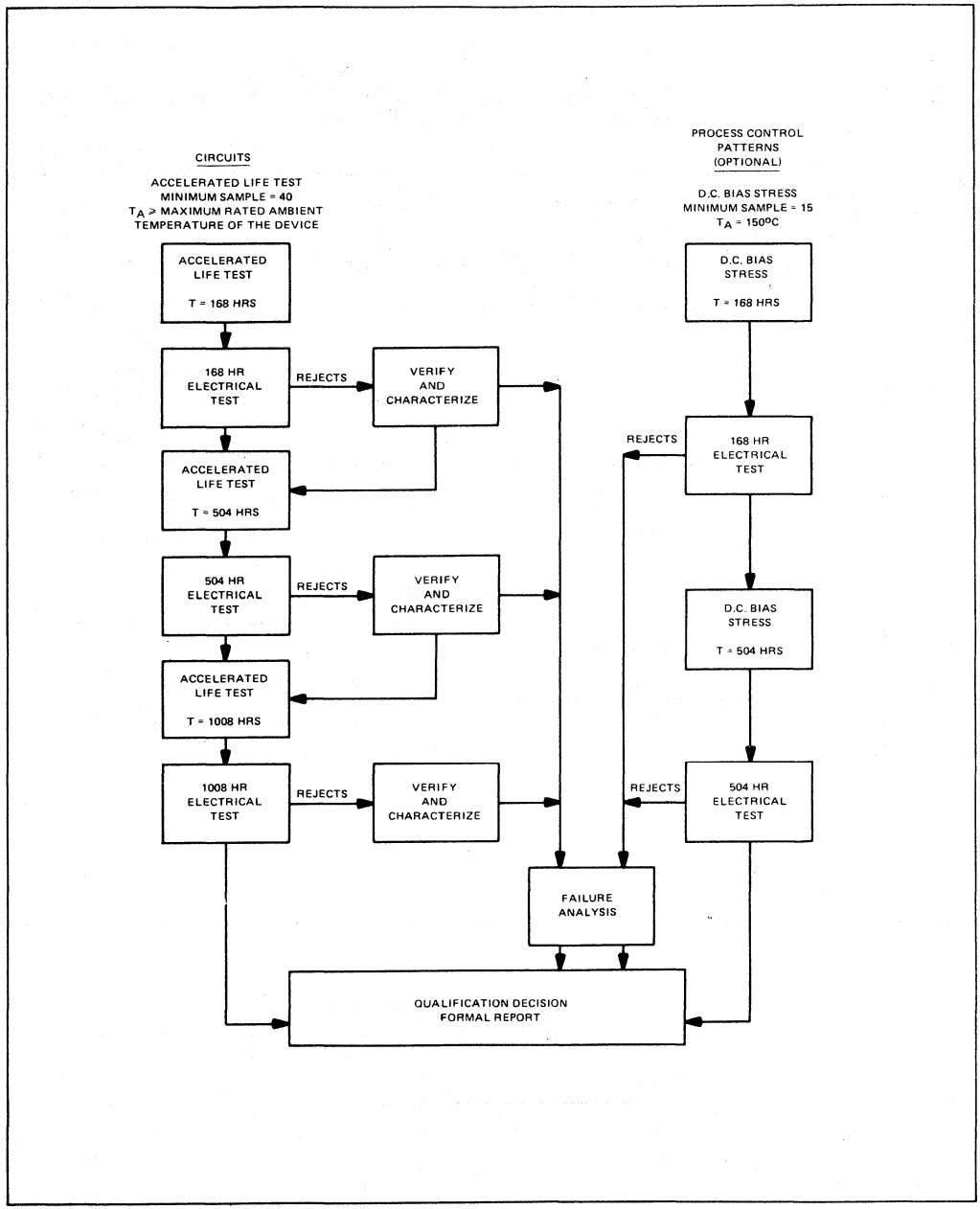
During the lifetime of the semiconductor industry, a wide variety of screening techniques have evolved to eliminate the lower tail of the process distribution discussed previously. These techniques may be categorized in two ways, as illustrated by the two axes of the matrix in Figure 9. The performing agency varies, depending on the type and purpose of the test. Most screens utilized by the industry today are based on MIL-STD-883 and are employed by Motorola in the various categories of Figure 9.

Several 100% visual screens are performed during assembly using both stereozoom and metallurgical microscopes. Subsequent sampling is performed by In-Process Quality Control as described above. The assembly mechanical tests for hermetic product consist of:

1. Gross leak sampling
2. Temperature cycling
3. Krypton-85 fine testing.

At the end of the assembly process, production final test screens the product with a comprehensive series of DC, functional, and speed-oriented electrical tests. These tests are normally more stringent than data sheet requirements and are sampled by Outgoing Quality Control per the flow chart of Figure 10.

FIGURE 7 – RELIABILITY EVALUATION TEST FLOW



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FIGURE 8 – HERMETIC PACKAGE QUALITY CONTROL FLOW CHART (SIMPLIFIED)

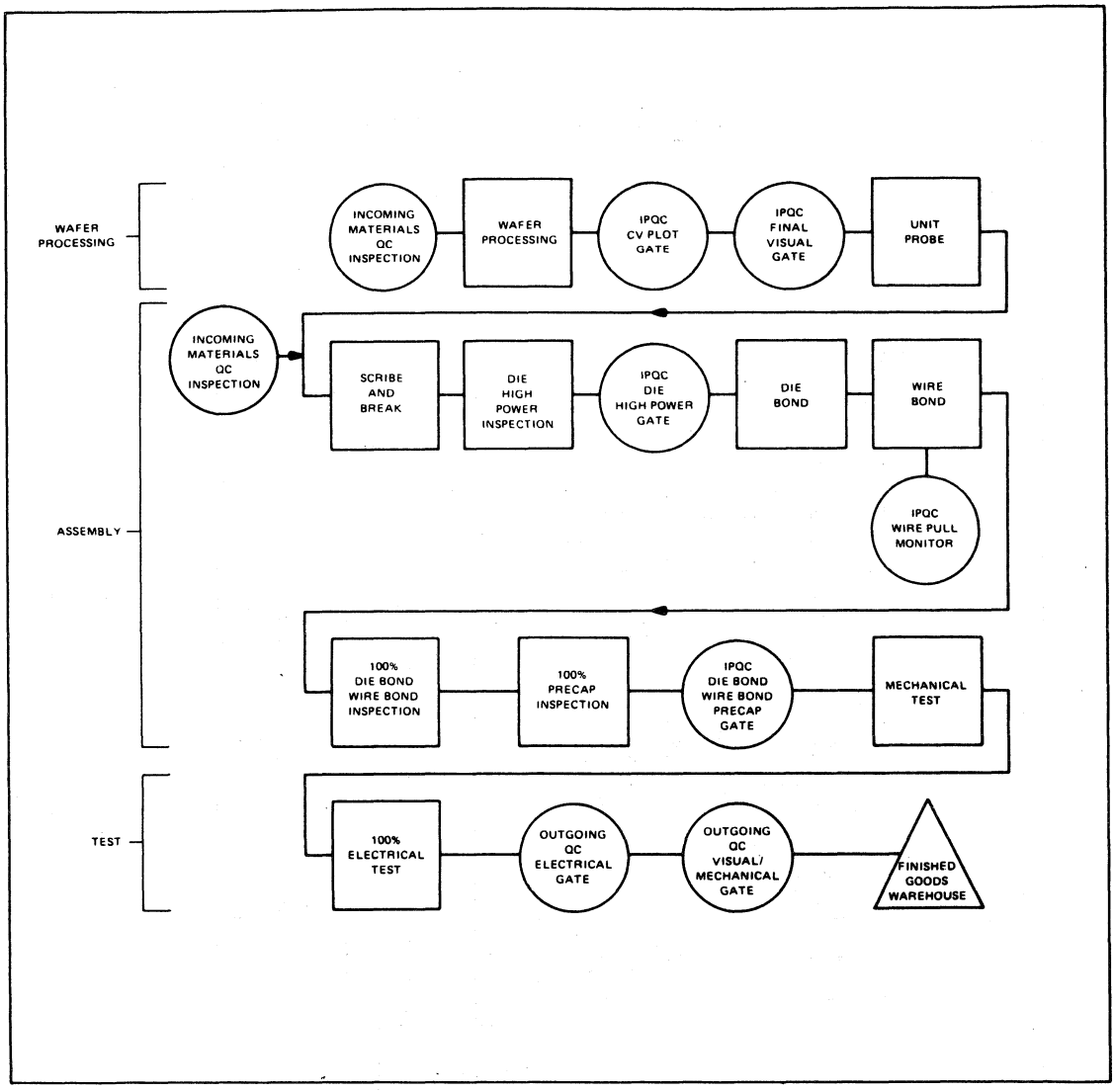


FIGURE 9 – TESTING CATEGORIES

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Category	Visual Inspection	Thermal/ Mechanical Testing	Electrical Testing	Environmental Stress
100%	Assembly	Assembly	Final Test	Production Burn-in
Sampling	In-Process QC Outgoing QC	In-Process QC	Outgoing QC	Lot Processing Quality Assurance
Qualification Testing	Reliability Engineering			

FIGURE 10 – CMOS OUTGOING QUALITY CONTROL FINAL TEST FLOW

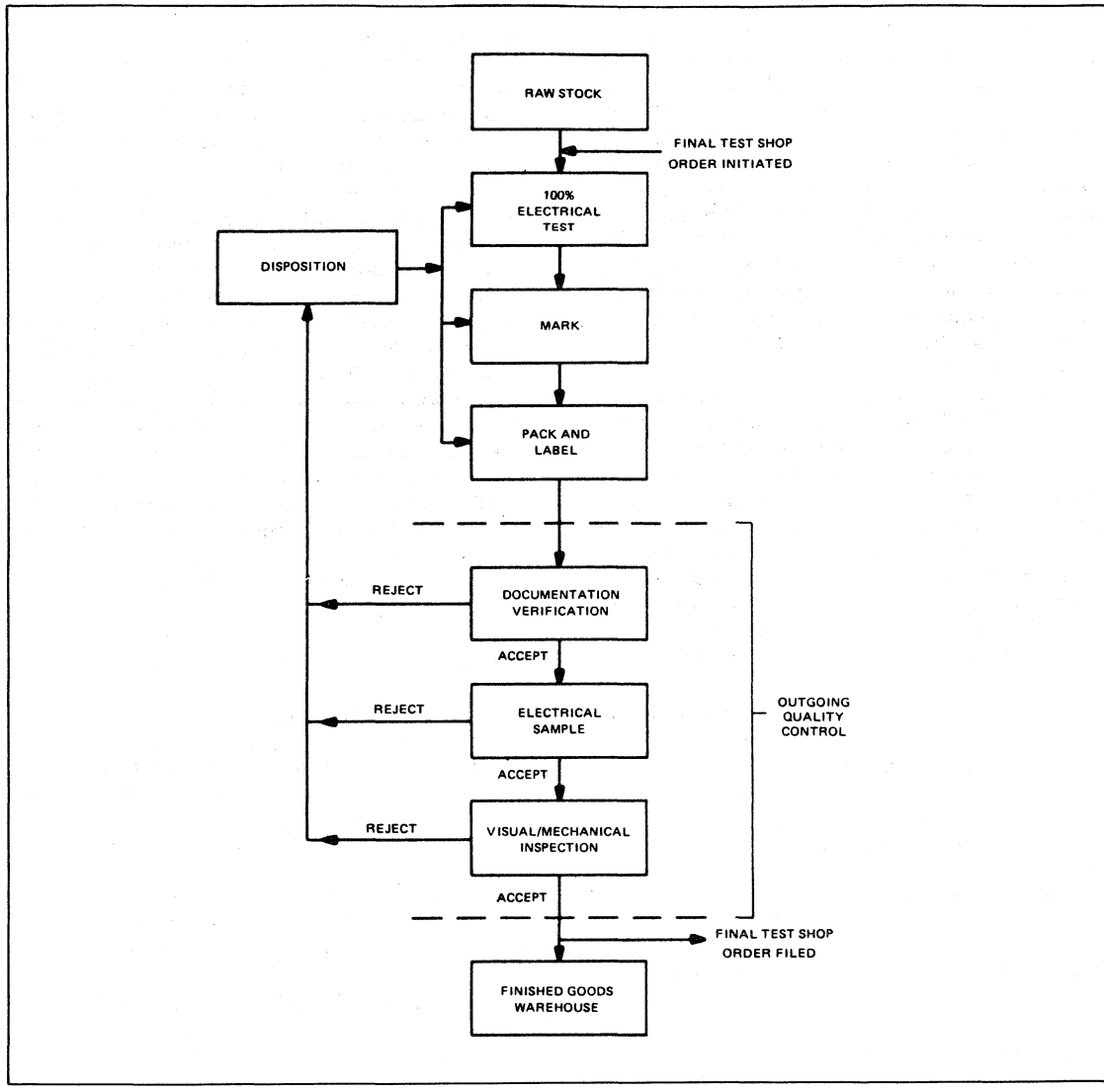


FIGURE 10a – CMOS OUTGOING QUALITY CONTROL SAMPLING PLAN

Characteristic	LTPD	ACC #	EQUIVALENT AQL
Vis/Mech/Clerical	5	0	0.11
Functional	5	0	0.11
Parametric	5	0	0.11
Cumulative	5	0	0.11

Outgoing QC performs electrical inspections as outlined below. These consist of DC and functional tests and are performed to an LTPD of 5 with a 0 accept number. For January 1979 LTPD values and equivalent AQL values See Figure 10 a. Quality control is on a programme of constant improvement. For the latest LTPD and equivalent AQL values contact the local sales office.

Visual inspections are also performed using the same LTPD and in both cases the lots are returned for 100% rescreen if failed. The production final test philosophy is described and compared to the Outgoing Quality Control tests in Figure 11. In addition to the techniques described here, a Quality Assurance organization exists to approve final test programs and conduct periodic monitors of all products for a wide variety of environmental life and electrical tests.

Various methods are touted for reducing the infant mortality of CMOS including temperature cycle, thermal shock, high temperature testing, stabilization bake and burn-in. Temperature cycle is a standard part of the ceramic assembly process where it is useful for detecting hermeticity problems, but as a screen, it is usually directed toward wire bond failures in plastic. The data included in the System Implementation section adequately demonstrates that several hundred cycles at extreme temperature ranges are required to produce failures in Motorola plastic CMOS and that thermal shock is even less effective. There is obviously no benefit in thermal cycling for eliminating infant mortality in Motorola Plastic CMOS, and the high temperature continuity data support the same conclusion. Stabilization bake was introduced for unpassivated discrete products and did have a significant effect. With properly passivated integrated circuits and Motorola product in particular, the effect of a bake is insignificant since no bias is present to drive mobile ions or stress junction defects. Cost adders for bakes are particularly misleading since the sealing temperature of ceramic packges performs this function and a cure cycle is always part of the plastic process.

Constant acceleration is occasionally required for hermetic product testing. The intent of this centrifuge test is to exert a force on the wire bonds which would detect latent failures. Calculations have shown that even at 30,000 Gs, a higher than normal military requirement, the force on a wire is in the order of 100 mg. This is insignificant compared to a wire pull average of at least 7000 mg. Since each wire bonder is sampled continuously to provide constant control, centrifuge becomes a needless screen. Occasionally die bonds can fail in a centrifuge test, but Motorola controls this factor by employing stringent wetting criteria in a 100% visual screen enforced by In-Process QC.

Burn-in remains the only screening technique which is effective, in eliminating infant mortality. To characterize

FIGURE 11 – MOTOROLA CMOS FINAL TEST OF STANDARD PRODUCT

TESTS PERFORMED ON 100% OF PRODUCT	TESTS PERFORMED ON Q.C. SAMPLE GATES[1]
1. Functional, V_{DD} = 3 Volts V_{DD} = 18 Volts	1. Functional, V_{DD} = 3 Volts V_{DD} = 18 Volts
2. Leakage Current (I_{DD}), V_{DD} = 5 Volts V_{DD} = 15 Volts	2. Leakage Current (I_{DD}), V_{DD} = 5 Volts V_{DD} = 10 Volts V_{DD} = 15 Volts
3. Output Voltage (V_{OH}/V_{OL}), V_{DD} = 15 Volts	3. Output Voltage (V_{OH}/V_{OL}), V_{DD} = 5 Volts V_{DD} = 10 Volts V_{DD} = 15 Volts
4. Output Current (I_{OH}/I_{OL}), V_{DD} = 5 Volts V_{DD} = 10 Volts	4. Output Current (I_{OH}/I_{OL}), V_{DD} = 5 Volts V_{DD} = 10 Volts V_{DD} = 15 Volts
5. Input Voltage (V_{IL}/V_{IH}), V_{DD} = 5 Volts (Noise Immunity) V_{DD} = 15 Volts	5. Input Voltage (V_{IL}/V_{IH}), V_{DD} = 5 Volts (Noise Immunity) V_{DD} = 10 Volts V_{DD} = 15 Volts
6. Input Current (I_{in}), V_{DD} = 15 Volts	6. Input Current (I_{in}), V_{DD} = 15 Volts
7. Output Saturation Current[2] (I_{sat}), V_{DD} = 5 Volts (Unbuffered Gates Only)	

NOTES 1. Data Sheet Limits (No Guardband)
2. Guarantees t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}, V_{DD} = 5 Volts

its effect, a large group of devices consisting of seven lots of three device types were burned-in and electrical readouts taken at frequent intervals. Of 873 devices tested, only nine failed over a 1000-hour test at 125 °C and 15 volts. These failures all occurred within the first 216 hours as indicated in the upper curve of Figure 12. The lower scale indicates the burn-in time at 125 °C while the upper scale gives the equivalent system time at 50 °C. The lower curve plots the resultant failure rate after the period of burn-in on the lower scale. A 48-hour burn-in has a dramatic effect and 168 hours eliminates nearly all the failures. For this reason 48, 96 and 168-hour burn-ins are offered as standard screens and the only technique considered effective for Motorola CMOS.

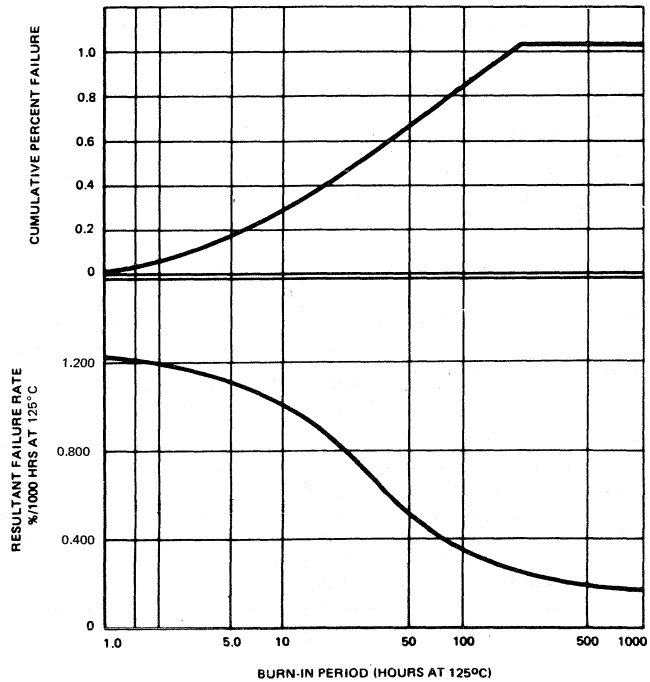
SYSTEM IMPLEMENTATION

Assessing System Requirements

The reliability needs of each system and application differ significantly, so the various aspects of component performance must be analyzed separately. The two parameters which should be addressed initially are infant mortality and long-term random failure rate. Systems with large numbers of components require greater component reliability. Infant mortality should be estimated and used to calculate service costs. This data should be balanced against the cost of a burn-in and possibly a board or system burn-in. Long-term reliability goals should be established for the system and used to calculate the necessary long-term failure rate for the components. Long-term failure rates cannot be effectively improved by short burn-ins unless they include infant mortality failures. (Infant failures are included in Motorola data.) Infant mortality can be effectively screened by short-term accelerated stress testing such as a 48-hour high temperature burn-in. The concepts defined earlier can be used to relate the burn-in to equivalent system hours. Often, customers who are experiencing problems fail to distinguish between infant mortality, long-term reliability and wear-out. It is imperative that failure patterns be sufficiently investigated and recorded to accomplish this. Buying a Hi Rel device will not solve a problem caused by poor handling or an unforeseen overstress in the application.

The system environment should be given careful consideration when choosing between plastic and hermetic packages. Sustained high temperature and humidity will accelerate the corrosion wearout mechanism in plastic. Office environments, however, will rarely produce a detectable difference in plastic and hermetic packages. Since the die and wire bonding systems are totally encapsulated in plastic, these packages can often outperform hermetics

FIGURE 12 – CUMULATIVE PERCENT FAILURE AND RESULTANT FAILURE RATE VS. BURN-IN PERIOD



for mechanical shock and vibration resistance. The potential for moisture condensation should be evaluated in light of the lead material and finish, whether the package is hermetic or plastic. Unusually moist or contaminated atmospheres can rapidly corrode ferrous metals under bias, regardless of the finish material.

Cost-effectiveness is also influenced by the number of defective units received by the customer. For various reasons, a small percentage of product is defective as received. This may be due to handling, correlation, shipping damage or a host of minor difficulties. The percentage of these defects should be less than one percent and any significant levels should be discussed with the vendor immediately.

Comparing Competitors' Data

Every manufacturer has a slightly different method of generating his reliability data. It is therefore difficult for a user inexperienced in reliability calculations to make a valid comparison. Toward this end the concepts introduced earlier will be of great value. The following parameters should be verified before any conclusions of vendor superiority are drawn.

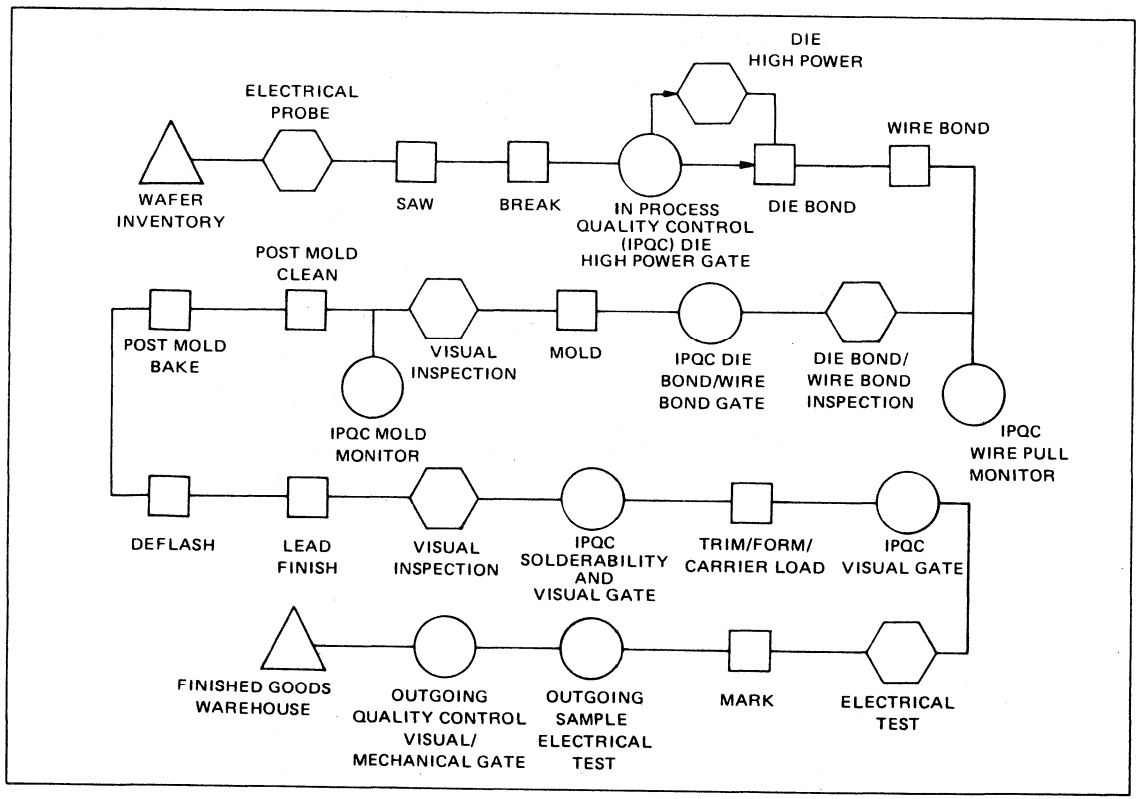
1. Confidence limit
2. Reject criteria (degradation, data sheet, functional, catastrophic, specific mechanisms)
3. Temperature of test
4. Activation energy
5. Distortion of failure rate due to a low number of device hours and failures
6. Biasing configuration
7. Test monitoring (system failures can produce impressive results due to less stringent stress being applied to the device).

Only if all these factors are considered can a truly objective comparison be made.

MOTOROLA DATA FOR PLASTIC PACKAGE DEVICES

The following data presents all the significant performance characteristics of CP-suffixed plastic-packaged devices. Of particular interest in the verification of a 0.04%/1000-hour failure rate; an impressive reduction from the 0.12%/1000-hour value reported previously. Other parameters continue at levels similar to those previously published.

PROCESS FLOW



PACKAGE DESCRIPTION

Die	Glassivated
Lead Frame	Alloy 42
Die Bond	Eutectic
Wire	Gold
Wire Bond	Thermocompression
Molding Compound	Epoxy Novalac
Mold Method	Transfer
Lead Finish	Tin Plate or Solder Dip

Life Test Data

Extensive life testing has generated a large and impressive data base which totally replaces that of earlier reports. All testing was performed at a temperature of 125°C with a 15 volt bias. Failures were verified and are included whether they are catastrophic or merely slight parametric drifts.

Moisture-Related Performance

One of the primary considerations in choosing a plastic package is its susceptibility to moisture ingression and corrosion. Since no plastic material forms an impervious barrier to moisture and its adhesion to the leadframe material is not perfect, moisture can enter the package by diffusing through the bulk material or wicking along the interface between the plastic and the metal leadframe. When moisture reaches the surface of the die, the applied potential forms an electrolytic cell which corrodes the aluminum, affecting DC parameters through its conduction and eventually causing catastrophic failure by opening the metal. The presence of contaminants greatly accelerates the reaction as does excessive phosphorous in the glassivation. Thus, careful controls are maintained on phosphorous concentration, cleaning techniques and molding processes.

Three popular techniques exist for determining the performance of components in the presence of moisture; Pressure Temperature Humidity (Autoclave), Pressure Temperature Humidity Bias (PTHB) and Temperature Humidity Bias (THB). Each test is used to achieve different objectives based on their sensitivity, length and difficulty. Autoclave is the quickest and simplest but the least effective since no bias is applied. It will detect only the most extreme contamination problems and provide little basis for distinguishing between groups of material since the lack of bias creates a condition which is atypical of actual use. PTHB is an excellent indicator of performance which distinguishes well and is quick, but which is difficult to perform. The presence of bias under these extreme conditions causes rapid corrosion of all metal surfaces including the device leads, sockets and PC board traces. The board often warps and this, in conjunction with corrosion, leads to open circuits during the test which produce either a relatively benign Autoclave condition or an electrical overstress. THB is the most reliable test method, but it requires much more time to develop failures. Board and socket problems are much less severe. Unlike PTHB, THB boards can be reused. In each of these tests, it is imperative that the chambers be kept clean and water purity be controlled.

Listed below is data generated from each of the three methods which is representative of current CMOS production.

AUTOCLAVE

Conditions — 15 psig, 121°C, 100% RH, 24 hrs.

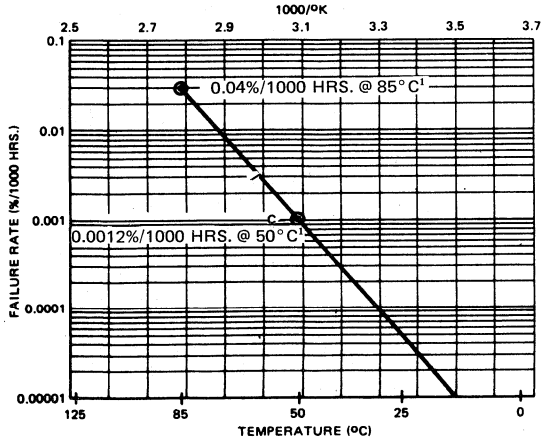
Lots	Devices	Failures	Percent Failure
10	220	0	0

PRESSURE TEMPERATURE HUMIDITY BIAS

Conditions — 15 psig, 121°C, 100% RH, 10 V, 12 hrs.

Lots	Devices	Failures	Percent Failure
70	683	10	1.46

FIGURE 13 — FAILURE RATE versus TEMPERATURE



Number of Wafer Lots	79
Number of Devices	6724
Failures	68
Equivalent Device Hours @ 85°C	1.77×10^8
V_{DD}	15V
Activation Energy	1.0 eV
Confidence Limit	60%

[1] Figures extrapolated from 125 °C testing and slope corresponding to 1.0 eV activation energy.

Temperature Humidity Bias

Data of this type is often useful in comparing vendors if all the conditions are identical. Unfortunately, very little work has been done to generate acceleration factors for these tests, and even small differences in parameters may produce dramatic changes in the results. The best effort to date was a study of various THB conditions which resulted in an empirical model for THB life versus vapor pressure. The model takes the form and is plotted in Figure 15. A vapor pressure chart is also provided in Figure 16 to simplify the estimation of median life.

It must be emphasized that this is an estimation since the plot extrapolates to values beyond the age of CMOS technology and beyond the test conditions normally used by Motorola. Wide negative variations from this plot can be expected if devices are exposed to contaminants or positive variation can be achieved through the proper use of conformal coatings or potting compounds.

Thermal Cycling Performance

The plastic package, unlike the ceramic package, has no cavity so the wires are in contact with the encapsulant. The difference in the thermal coefficient of expansion between the wires, encapsulant and leadframe, therefore,

FIGURE 14 – CUMULATIVE PERCENT FAILURES versus TIME
(Conditions, 85°C, 85% RH, 10 V)

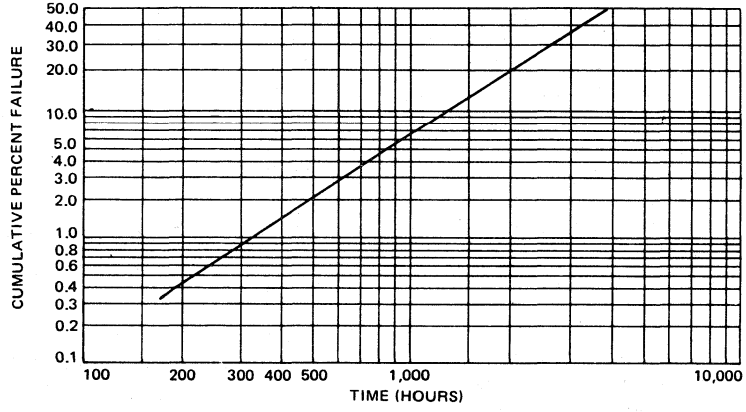


FIGURE 15 – MEDIAN LIFE versus VAPOR PRESSURE

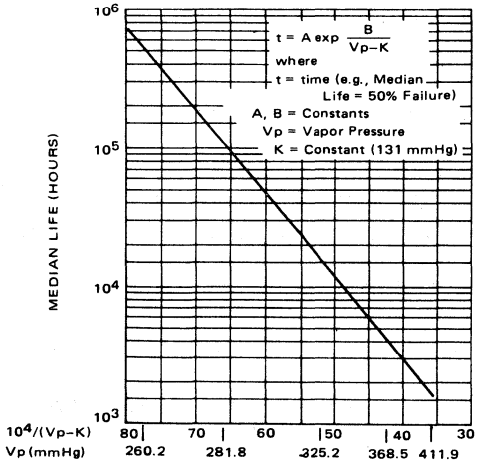
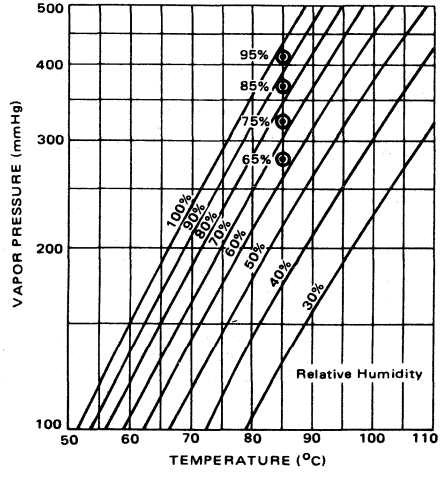


FIGURE 16 – VAPOR PRESSURE versus TEMPERATURE AND RELATIVE HUMDIITY



cause stress to develop as the device is cycled over a range of temperature. Since most leadframes are Alloy 42, differences in the ability to withstand this stress are dependent on the wirebonding and molding processes. The degree to which these processes are engineered and controlled determines the thermal cycling performance of the device. One particular occurrence which has improved this performance is the increasing shift to automatic wirebonding. This technique provides an extremely consistent bond which has been unattainable with manual systems and dramatically reduces lot to lot variations in the testing described below. Three tests characterize thermal cycling performance; High Temperature Continuity, Thermal Shock and Temperature Cycle. High Temperature Continuity is employed as a routine production monitor as well as a readout test for Thermal Shock and Temperature Cycle. A complete electrical test is also done at each readout of the shock and cycling sequences so the data provided includes parametric and functional failures in addition to opens and intermittents. The following data displays the performance of current plastic integrated circuits under each of these conditions:

HIGH TEMPERATURE CONTINUITY

Conditions – 125°C, Forward Bias Current
No prescreening or stressing

Lots	Units	Rejects
406	26,897	0

THERMAL SHOCK

Conditions – MIL-STD-883A
Method 1011.1, Condition C
–65°C to +150°C

Lots	Units
12	688

Cycles	Cumulative % Failures
150	0.45
300	0.45
450	0.45
600	0.75

TEMPERATURE CYCLE

Conditions – MIL-STD-883A
Method 1010.1, Condition C
–65°C to +150°C

Lots	Units
34	1883

Cycles	Cumulative % Failures
100	0
150	0.29
300	0.61
500	1.10
750	1.84
1000	2.72

The unstressed High Temperature Continuity data is excellent, reflecting the engineering behind Motorola's plastic packaging system. The Thermal Shock data is also good and exhibits a more shallow slope than the Temperature Cycle data. This is consistent with previous data and demonstrates an apparent effect of the longer dwell time used for cycling. Although more time-consuming, temperature cycle puts a greater stress on the device than thermal shock. The most significant attribute of the data is that hundreds of cycles are required to produce failures even at the extreme conditions employed here. The use of temperature cycle as a screen is therefore not cost-effective since no significant early failures are detected.

CERAMIC PACKAGE DEVICES

This section describes the package, processing and life test performance of all ceramic packaged CMOS devices. These families bear a CL or AL suffix designating the commercial (–40°C to 85°C) or military (–55°C to 125°C) temperature range. The AL device also receives a more stringent internal visual inspection, ten temperature cycles instead of five and tighter electrical testing.

PACKAGE DESCRIPTION

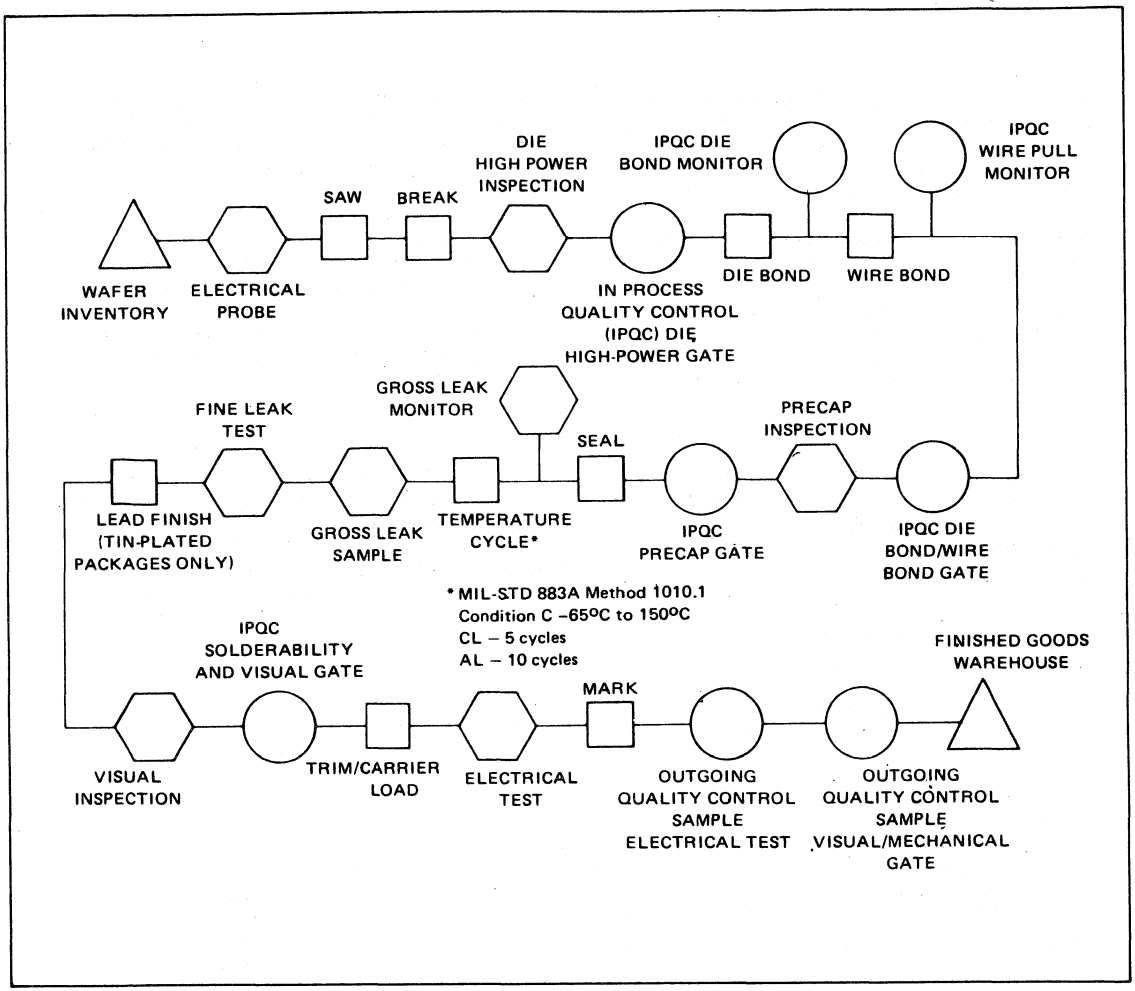
CERDIP – Frit Seal Ceramic Dual Inline Package

Die	Glassivated
Leadframe	Alloy 42
Die Bond	Eutectic
Wire	Aluminum
Wire Bond	Ultrasonic
Package Body	Alumina
Lead Finish	Tin Plate

Side Braze – Laminated Ceramic Package

Die	Glassivated
Die Bond	Eutectic
Wire	Aluminum
Wire Bond	Ultrasonic
Seal	Solder with gold plated Kovar lid or Glass frit with alumina lid
Package Body	Glass laminated alumina
Metallization	Gold plated tungsten
Leads	Gold or tin plated Kovar

PROCESS FLOW



LIFE TEST DATA

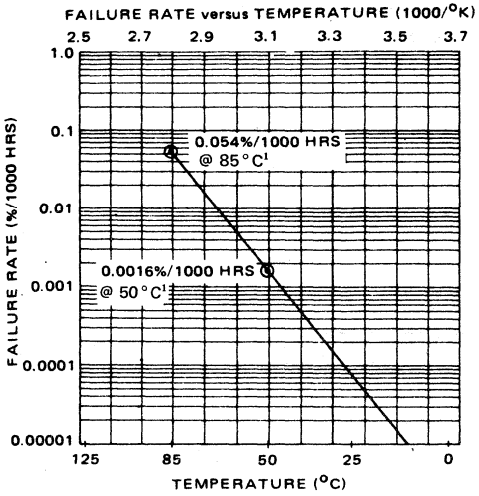
Life testing of CL devices is performed at 125°C and 15 volts while the AL series is stressed at 200°C and 15 volts. The resultant CL data is similar to the CP data, as can be expected since the plastic process has no significant effect on the die and the electrical test screens for both products are identical. Although the larger plastic data base results in a better failure rate, the choice between these families should be made on the basis of environmental constraints on the package rather than a significant difference in life test performance. The AL series does provide an increased temperature range and tighter electrical limits and is more suitable where higher reliability is required. This performance is limited mainly by the size of the data base and would appear significantly better than the CP and CL families if a similar sample size were used.

Life Test Techniques

The usual temperature for burn-in is 125 °C. Fifteen volts is applied to V_{DD} in all cases and is significant due to the inability of many competitors to perform sucessfully at 125 °C in excess of 10 volts. Various independent studies have indicated that the voltage acceleration factor for comparing 15 volt data to 10 volt data ranges from 2 to 10.

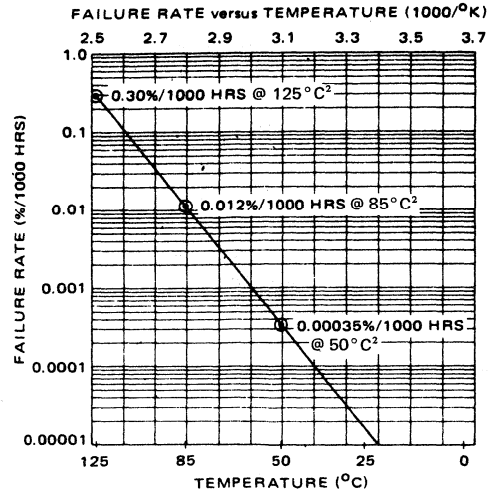
Biasing patterns can also determine the amount of stress

FIGURE 17 – COMMERCIAL TEMPERATURE RANGE



[1] Figures extrapolated from 125 °C testing and slope corresponding to 1.0 eV activation energy.

FIGURE 18 – MILITARY TEMPERATURE RANGE



[2] Figures extrapolated from 200 °C testing and slope corresponding to 1.0 eV activation energy.

TEST DATA

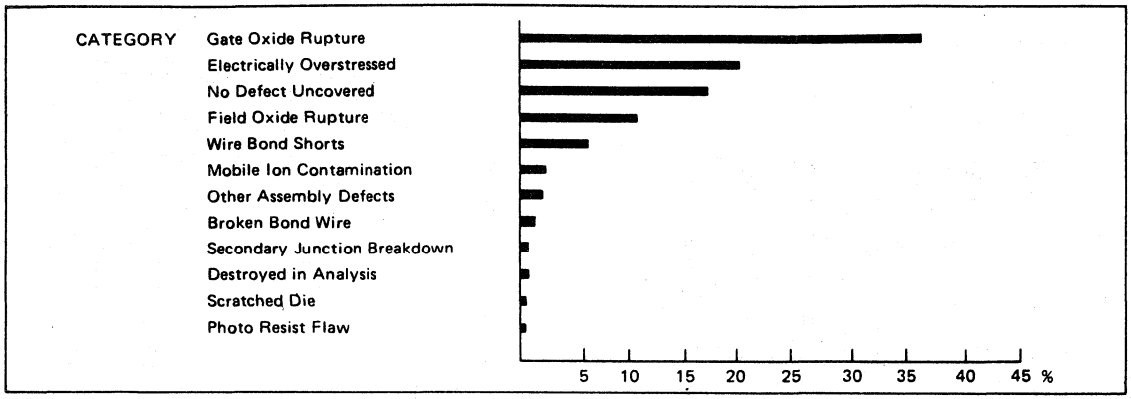
	Commercial MC14XXXCL	Military MC14XXXAL
Temp. Range	-40 to +85°C	-55 to +125°C
Number of Wafer Lots	10	70
Number of Devices	1175	697
Equivalent Device Hours	3.01×10^7 @ 85°C	3.40×10^6 @ 125°C
Number of Failures	15	9
V_{DD}	15V	15V
Activation Energy	1.0 eV	1.0 eV
Confidence Limit	60%	60%

on the circuit. Since the electric field created by the circuit biasing determines the level of stress, a worst case condition is achieved by maximizing the number of internal components to which a potential difference is applied. In most SSI and MSI devices, this can be achieved through the careful choice of a static pattern while more complex circuits require dynamic biasing to access internal nodes. Static bias provides a greater stress on an individual transistor while dynamic bias maximizes the number of devices biased at a lower duty cycle.

System failures in the field may occur upon catastrophic device failure or merely with parametric degradation if the circuit is more sensitive. It is, therefore, important that electrical readouts test parametrics as well as functionality in the same manner as the production final test program.

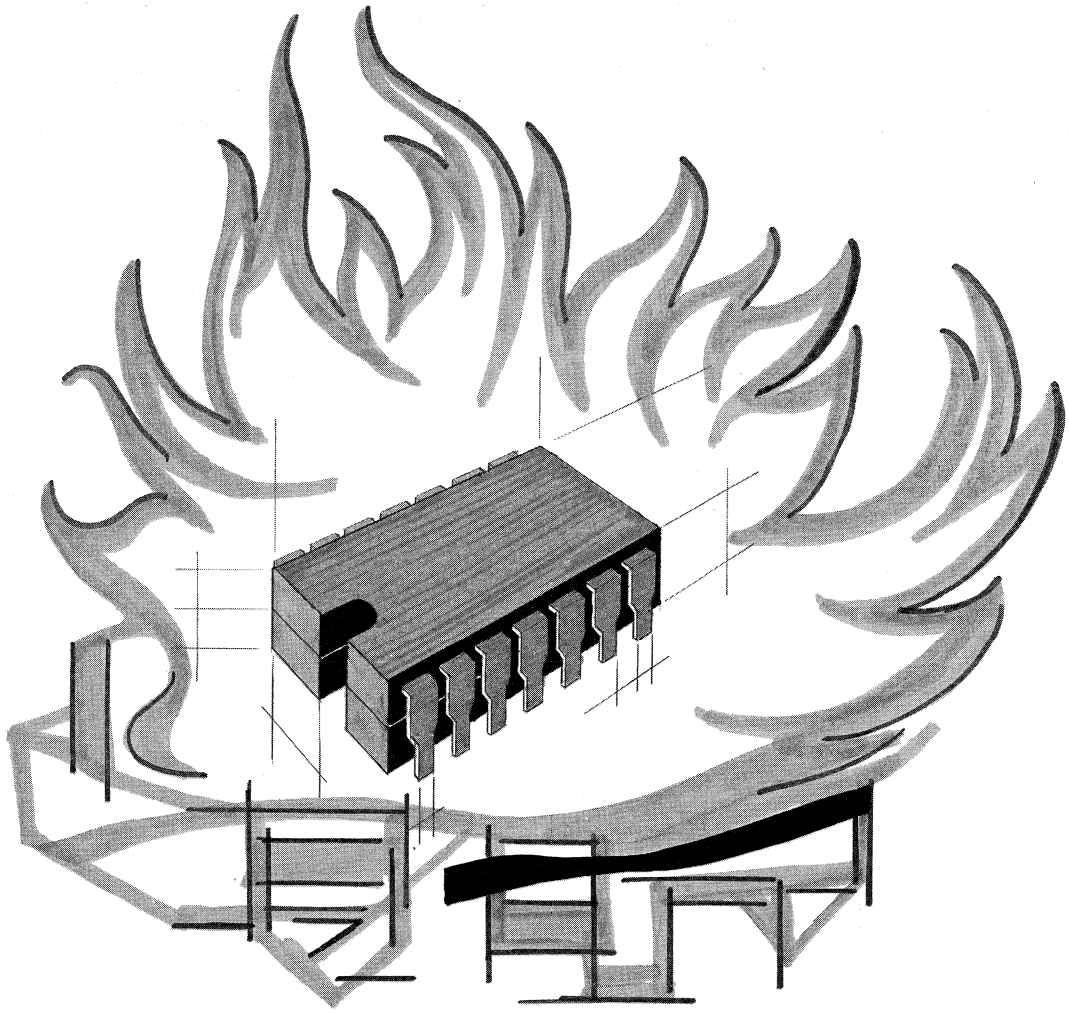
Proper evaluation of rejects and feedback to processing can occur only through intensive failure analysis. To support the processing areas, product groups and R & QA, a Product Analysis Laboratory exists. "State-of-the-art" analytical tools are at its disposal including wet chemical techniques, Auger, electron microprobe and scanning electron microscopy with stroboscopic voltage contrast. This capability is complemented by computer tracking systems to evaluate failure patterns and distributions. A simplified example is illustrated in the bar chart of Figure 19.

FIGURE 19 – FAILURE CAUSE



CONCLUSION

This chapter has attempted to explain some of the concepts of reliability and quality control testing used for CMOS product. Motorola's reputation for reliability and customer support has been established by the philosophy of its leadership and is being perpetuated through the efforts of CMOS Reliability and Quality Assurance. Customer assistance is always available through sales offices, marketing or R & QA personnel directly.



Mechanical and thermal data

11

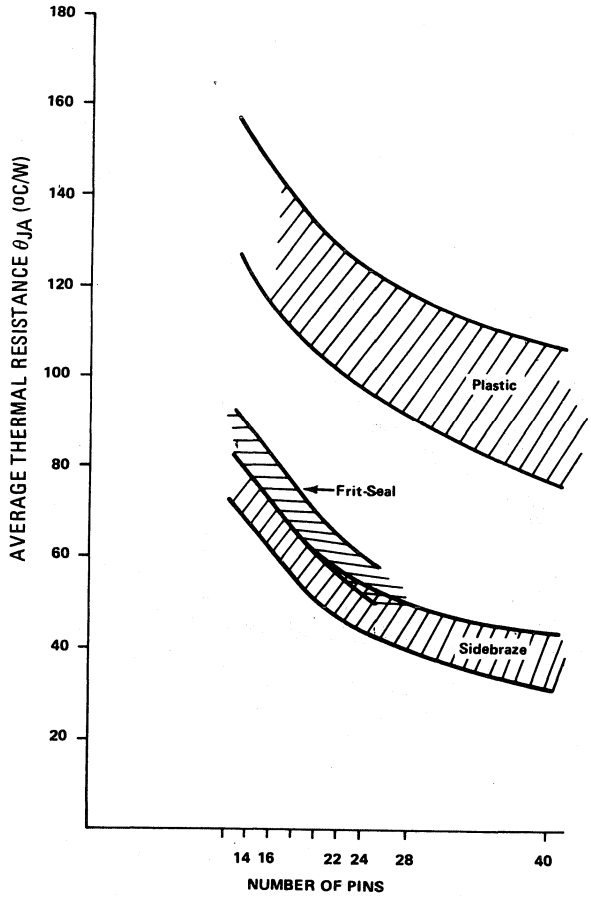
THERMAL RESISTANCE θ_{JA}

The junction-to-ambient thermal resistance values of dual in-line packaging systems used in Motorola CMOS integrated circuits are graphically illustrated in Figure 1. Each envelope represents the typical range of values for plastic, frit-seal or ceramic sidebraze package types as a function of size. The values were obtained while operating in a "still-air" environment and inserted into low-cost sockets mounted on printed circuit cards.

Thermal resistance is influenced by a number of factors including die size, cavity size and die bonding. In order to present a comprehensive characterization of these variables, a range of values is provided rather than a single point.

Since most CMOS devices dissipate insignificant power, it is not likely that thermal resistance will be a critical design factor. In those situations where high dc currents or high-speed operation is required, the junction temperatures should be estimated through the use of this data and by knowing the actual power being dissipated by the device.

FIGURE 1 – THERMAL RESISTANCE OF DIP PACKAGES

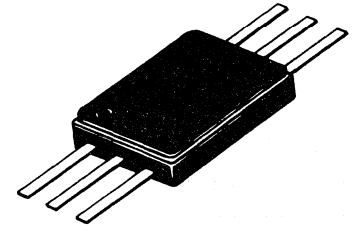


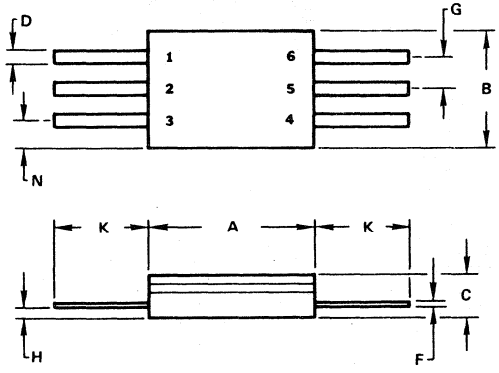
MECHANICAL DATA

The packaging availiability for each device is indicated on the individual data sheets. Dimensions for the packages are given in this section.

6-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 688



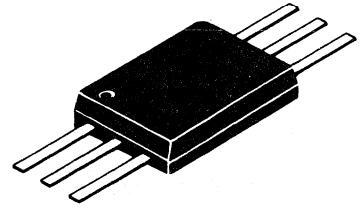


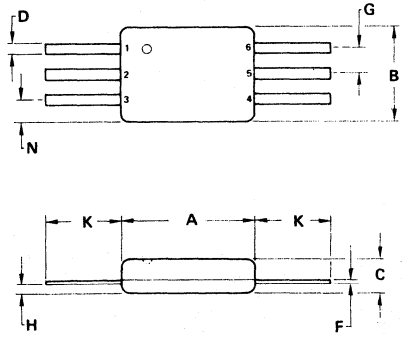
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	7.11	0.235	0.280
B	4.32	5.72	0.170	0.225
C	1.17	1.91	0.046	0.075
D	0.25	0.51	0.010	0.020
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.13	0.89	0.005	0.035
K	1.90	3.05	0.075	0.120
N	0.89	1.52	0.035	0.060

CASE 688-05

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.13 mm (0.005) RADIUS TO DIM "A" & "B" AT MAXIMUM MATERIAL CONDITION.

P SUFFIX
PLASTIC PACKAGE
CASE 704



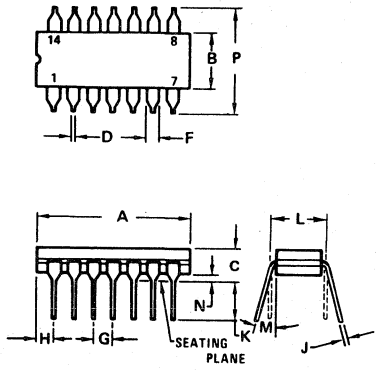


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.69	6.35	0.224	0.250
B	4.06	5.08	0.160	0.200
C	1.17	1.90	0.046	0.075
D	0.38	0.51	0.015	0.020
F	0.20	0.30	0.008	0.012
G	1.22	1.32	0.048	0.052
H	0.13	0.89	0.005	0.035
K	2.34	2.84	0.092	0.112
N	0.89	1.14	0.035	0.045

CASE 704-02

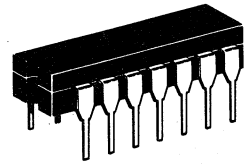
14-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 632



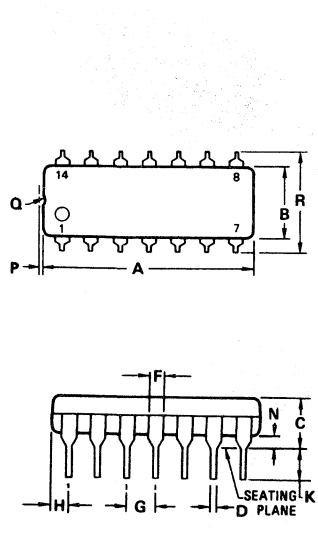
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

CASE 632-06



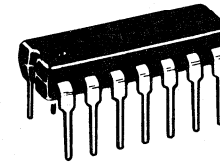
NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "A" AND "B" (632-06) DO NOT INCLUDE GLASS RUN-OUT.
4. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

P SUFFIX
PLASTIC PACKAGE
CASE 646



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

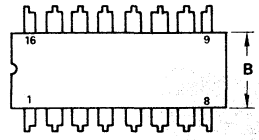
CASE 646-05

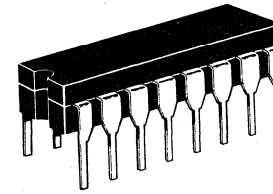


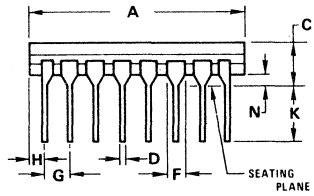
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

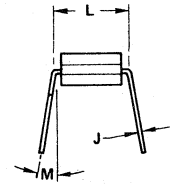
16-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 620







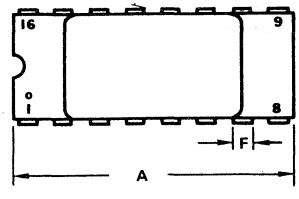


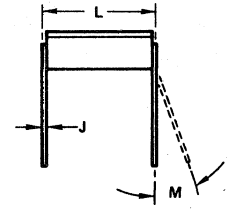
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

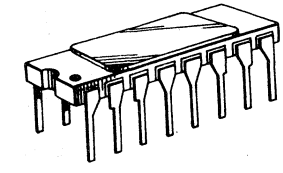
CASE 620-06

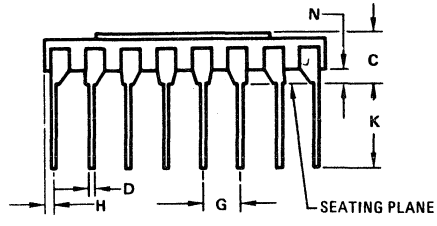
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM "A" AND "B" (620-06) DO NOT INCLUDE GLASS RUN-OUT.

L SUFFIX
CERAMIC PACKAGE
CASE 690









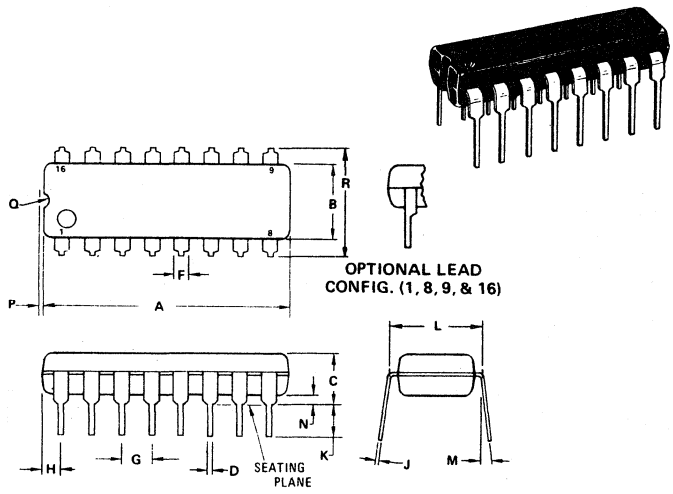
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.07	20.57	0.790	0.810
B	7.11	7.62	0.280	0.300
C	2.67	3.94	0.105	0.155
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.38	1.40	0.015	0.055

CASE 690-12

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION, AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

16-PIN PACKAGES (Continued)

P SUFFIX
PLASTIC PACKAGE
CASE 648



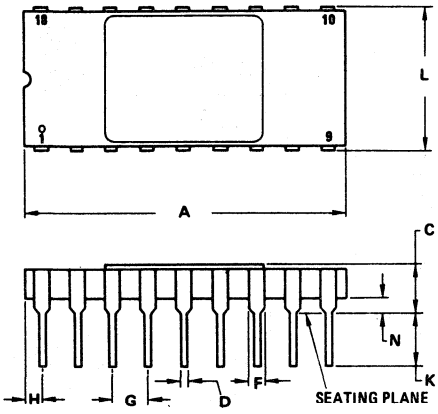
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

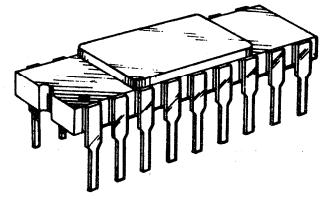
CASE 648-05

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9 AND 16.
5. ROUNDED CORNERS OPTIONAL.
6. 648-04 OBSOLETE, NEW STD 648-05.

18-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 680



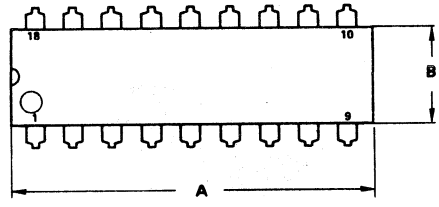


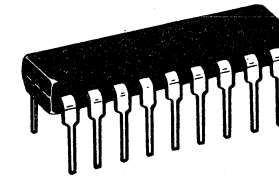
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.48	23.24	0.885	0.915
B	7.16	7.57	0.282	0.298
C	3.18	4.27	0.125	0.168
D	0.38	0.58	0.015	0.023
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.68	4.44	0.105	0.175
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.38	1.40	0.015	0.055

CASE 680-06

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

P SUFFIX
PLASTIC PACKAGE
CASE 707

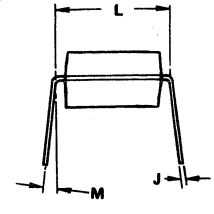




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 707-02

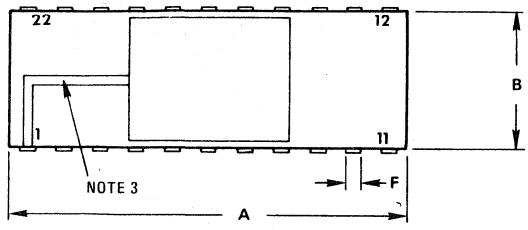
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



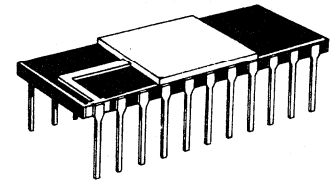
11

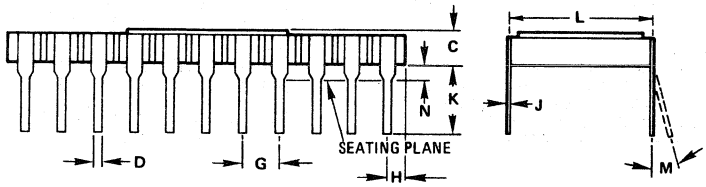
22-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 677



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. EXPOSED CONTACT TO LEAD 1, OPTIONAL.

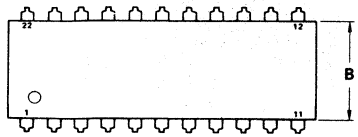


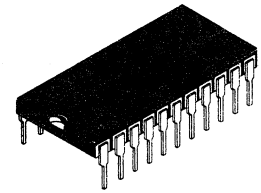


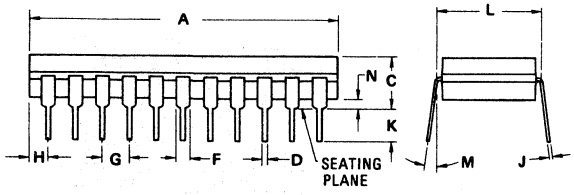
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.15	27.71	1.069	1.091
B	9.65	10.06	0.380	0.396
C	2.79	3.56	0.110	0.140
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.51	1.52	0.020	0.060
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	9.91	10.41	0.390	0.410
M	–	10°	–	10°
N	0.64	1.27	0.025	0.050

CASE 677-05

L SUFFIX
CERAMIC PACKAGE
CASE 736







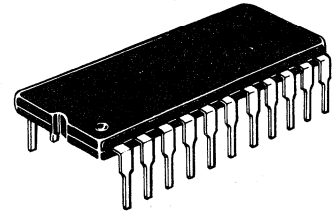
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	26.80	27.81	1.055	1.095
B	9.14	9.91	0.360	0.390
C	3.81	5.46	0.150	0.215
D	0.38	0.53	0.015	0.021
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	2.54	4.32	0.100	0.170
L	9.91	10.41	0.390	0.410
M	–	15°	–	15°
N	0.25	0.89	0.010	0.035

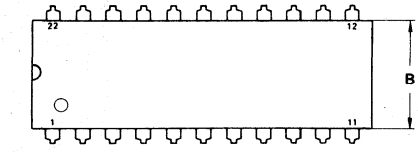
CASE 736-01

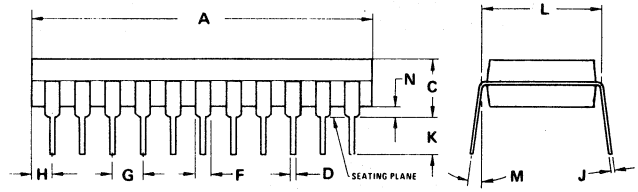
NOTES:
1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "D").
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

22-PIN PACKAGES (Continued)

P SUFFIX
PLASTIC PACKAGE
CASE 708







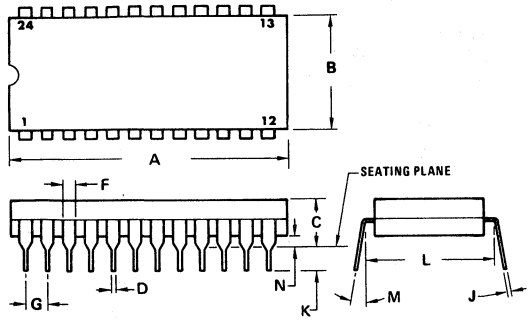
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

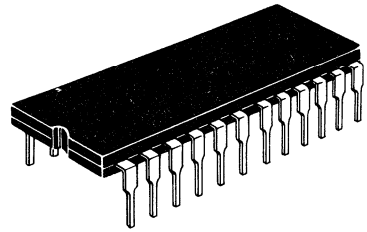
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	4.39	0.155	0.173
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 708-03

24-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 623



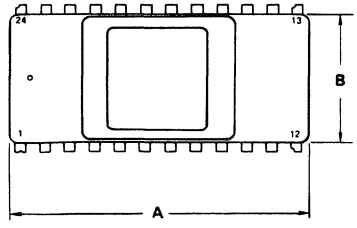


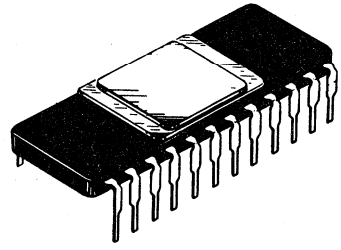
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.27	0.020	0.050

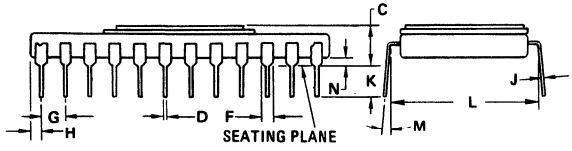
NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

CASE 623-03

L SUFFIX
CERAMIC PACKAGE
CASE 684







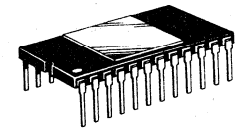
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	29.34	30.86	1.155	1.215
B	12.70	14.22	0.500	0.560
C	3.05	3.94	0.120	0.155
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.92	3.68	0.115	0.145
L	14.86	15.87	0.585	0.625
M	–	15^0	–	15^0
N	0.51	1.14	0.020	0.045

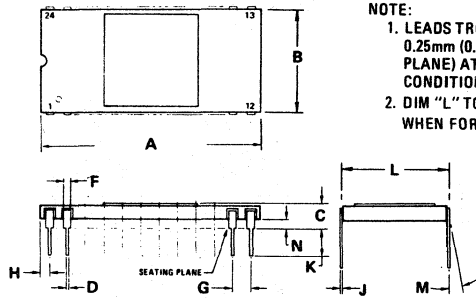
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. LEAD NO. 1 CUT FOR IDENTIFICATION, OR BUMP ON TOP.
3. DIM "L" TO INSIDE OF LEADS. (MEASURED 0.51 mm (0.020) BELOW PKG BASE)

CASE 684-04

24-PIN PACKAGES (Continued)

L SUFFIX
CERAMIC PACKAGE
CASE 716



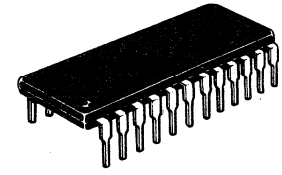


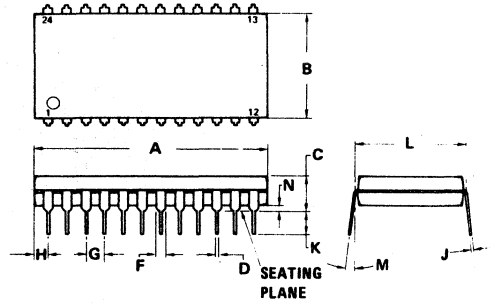
NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.64	30.78	1.088	1.212
B	14.94	15.34	0.588	0.604
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	–	10^0	–	10^0
N	1.02	1.52	0.040	0.060

716-04

P SUFFIX
PLASTIC PACKAGE
CASE 709





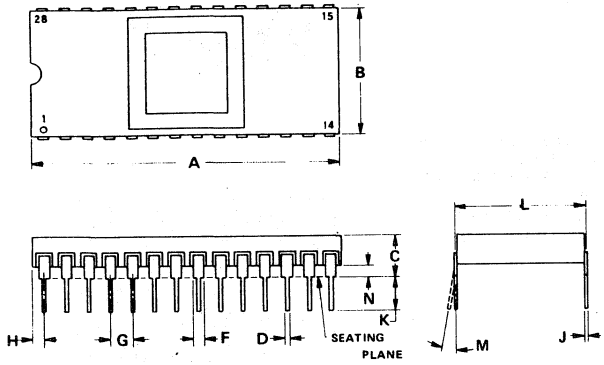
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

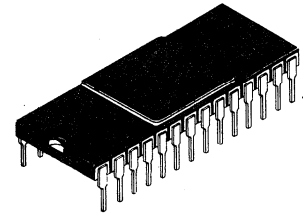
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.78	2.03	0.070	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.02	0.020	0.040

CASE 709-02

28-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 719



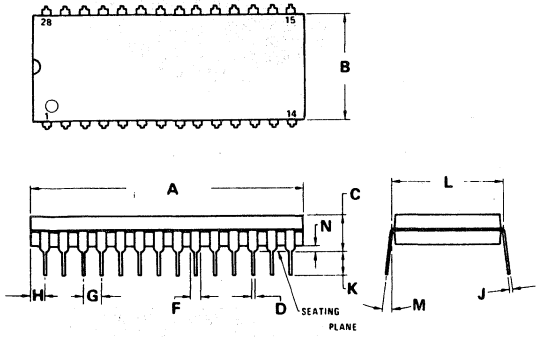


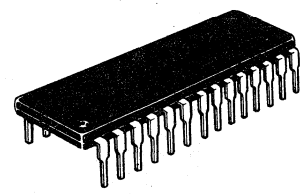
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	35.20	35.92	1.386	1.414
B	14.94	15.34	0.588	0.604
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

CASE 719-03

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIAMETER (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

P SUFFIX
PLASTIC PACKAGE
CASE 710





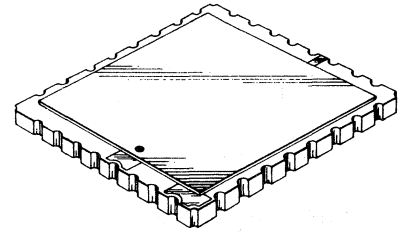
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

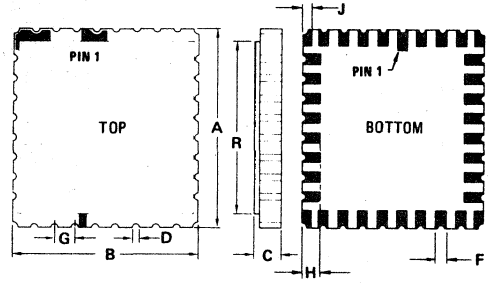
CASE 710-02

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

36-PAD PACKAGE

Z SUFFIX
LEADLESS CERAMIC PACKAGE
CASE 703





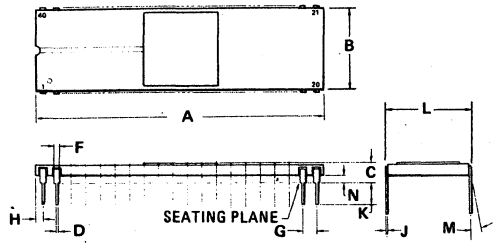
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.29	10.67	0.405	0.420
B	9.27	9.65	0.365	0.380
C	1.02	1.65	0.040	0.065
D	0.10	0.61	0.004	0.024
F	0.38	0.63	0.015	0.025
G	1.02 BSC		0.040 BSC	
H	0.76	1.14	0.030	0.045
J	0.25	0.51	0.010	0.020
R	8.76	9.02	0.345	0.355

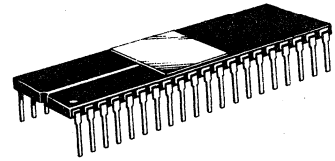
NOTE:
1. SLOTS, TRUE POSITIONED WITHIN 0.25 mm (0.010) TOTAL TO DIM. A and B AT MAXIMUM MATERIAL CONDITION.

CASE 703-01

40-PIN PACKAGE

L SUFFIX
CERAMIC PACKAGE
CASE 715



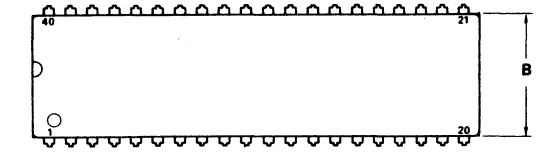


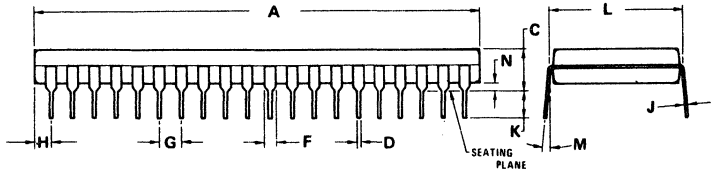
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.94	15.34	0.588	0.604
C	3.05	4.06	0.120	0.160
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

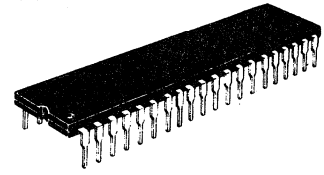
CASE 715-03

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX MAT'L CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

P SUFFIX
PLASTIC PACKAGE
CASE 711







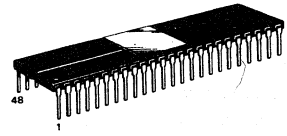
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

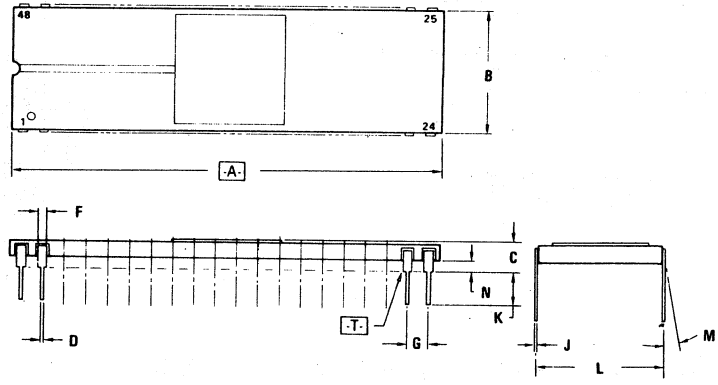
CASE 711-03

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

48-PIN PACKAGE

L SUFFIX
CERAMIC PACKAGE
CASE 740





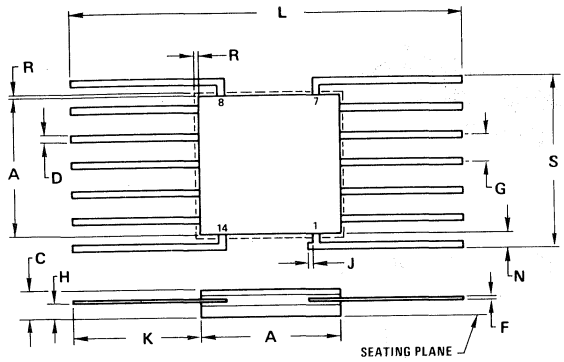
NOTES:
1. DIMENSION -A- IS DATUM.
2. POSTIONAL TOLERANCE FOR LEADS:
   ⌖ Ø 0.25 (0.010)Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

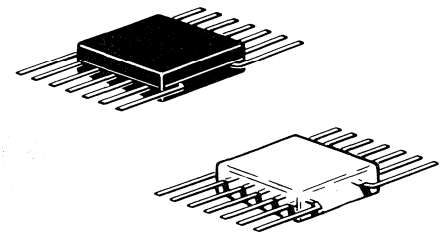
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	60.35	61.57	2.376	2.424
B	14.94	15.34	0.589	0.604
C	3.05	4.06	0.120	0.160
D	0.381	0.533	0.015	0.021
F	0.762	1.397	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.203	0.330	0.008	0.013
K	2.54	4.19	0.100	0.165
L	15.24 BSC		0.600 BSC	
M	0°	10°	0°	10°
N	1.016	1.524	0.040	0.060

CASE 740-01

14-PIN FLAT PACKAGE

F SUFFIX
CERAMIC PACKAGE
CASE 607





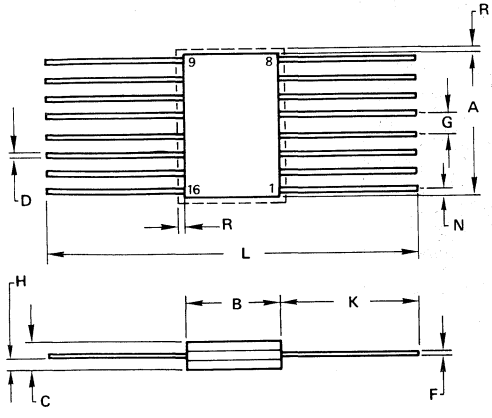
NOTE:
LEADS WITHIN 0.13 mm(0.005) TOTAL OF TRUE POSITION RELATED TO "A" AT MAXIMUM MATERIAL CONDITION.

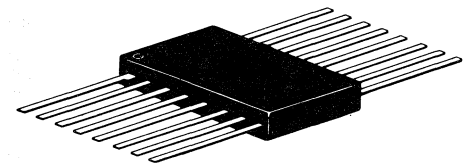
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
C	0.76	1.78	0.030	0.070
D	0.33	0.48	0.013	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.30	0.89	0.012	0.035
J	–	0.38	–	0.015
K	6.35	9.40	0.250	0.370
L	18.80	–	0.740	–
N	0.25	–	0.010	–
R	–	0.38	–	0.015
S	7.62	8.38	0.300	0.330

CASE 607-05

16-PIN FLAT PACKAGE

F SUFFIX
CERAMIC PACKAGE
CASE 650

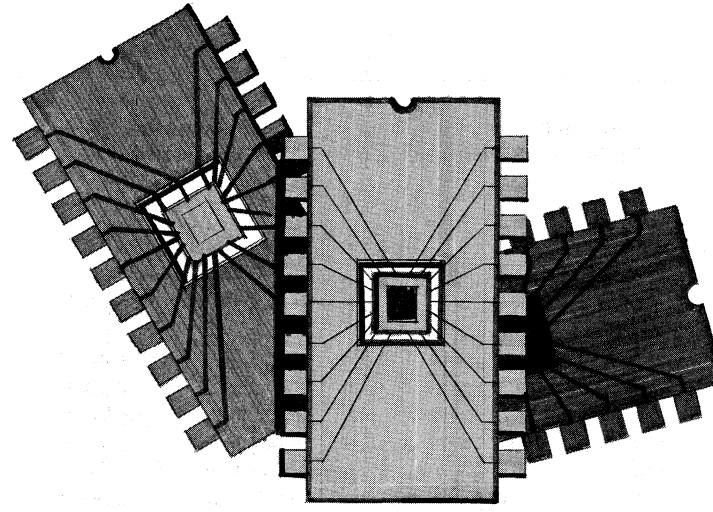




NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	6.60	0.245	0.260
C	1.52	2.03	0.060	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
N	–	0.51	–	0.020
R	–	0.38	–	0.015

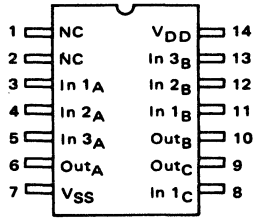
CASE 650-02



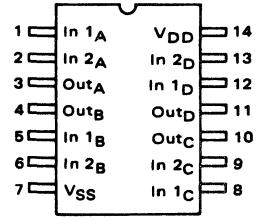
Device pin assignments 12

PIN ASSIGNMENTS (continued)

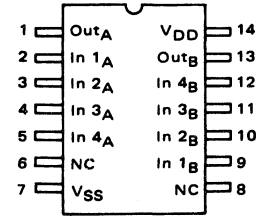
MC14000UB
Dual 3-Input NOR Gate Plus Inverter



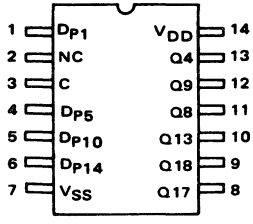
MC14001UB, MC14001B
Quad 2-Input NOR Gate



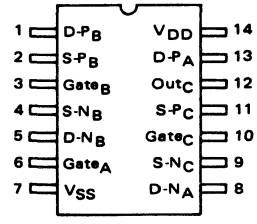
MC14002UB, MC14002B
Dual 4-Input NOR Gate



MC14006B
18-Bit Static Shift Register

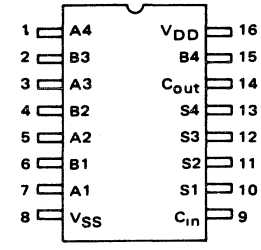


MC14007UB
Dual Complementary Pair Plus Inverter

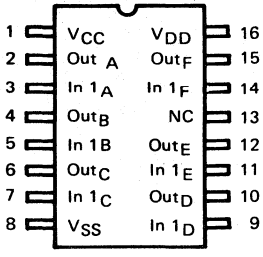


D = Drain
S = Source

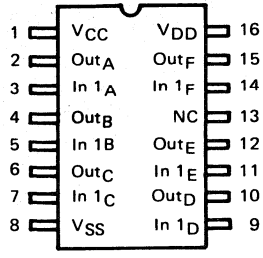
MC14008B
4-Bit Full Adder



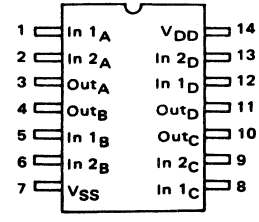
MC14009UB
Hex Inverter Buffer



MC14010B
Hex Buffer



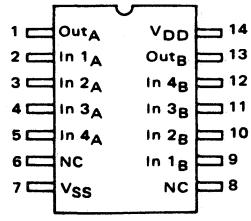
MC14011UB, MC14011B
Quad 2-Input NAND Gate



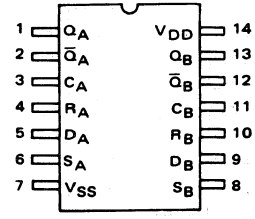
12

NC = No Connection

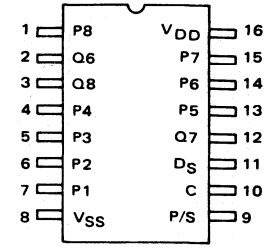
MC14012UB, MC14012B
Dual 4-Input NAND Gate



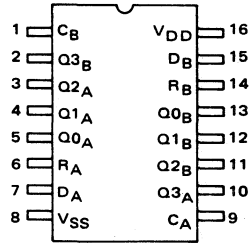
MC14013B
Dual Type D Flip-Flop



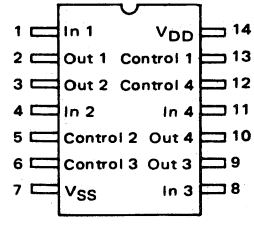
MC14014B
8-Bit Static Shift Register



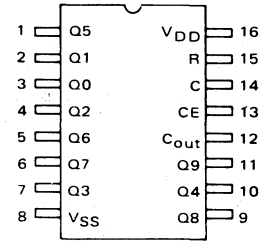
MC14015B
Dual 4-Bit Static Shift Register



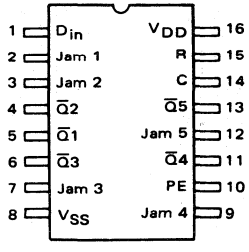
MC14016B
Quad Analog Switch/Quad Multiplexer



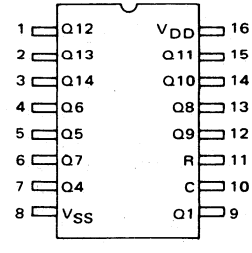
MC14017B
Decade Counter/Divider



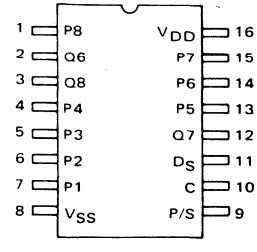
MC14018B
Presettable Divide-by-N Counter



MC14020B
14-Bit Binary Counter



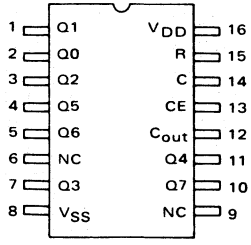
MC14021B
8-Bit Static Shift Register



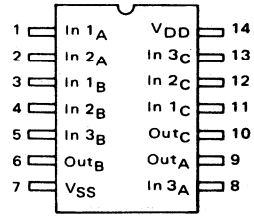
NC = No Connection

PIN ASSIGNMENTS (continued)

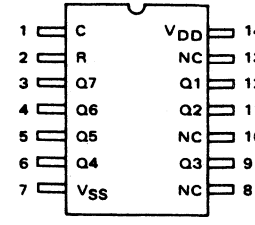
MC14022B
Octal Counter/Divider



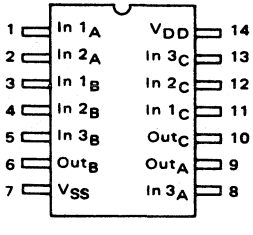
MC14023UB, MC14023B
Triple 3-Input NAND Gate



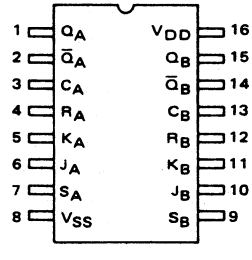
MC14024B
Seven-Stage Ripple Counter



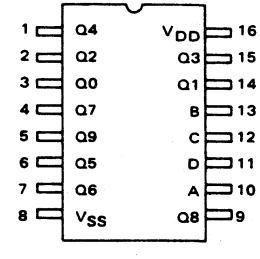
MC14025UB, MC14025B
Triple 3-Input NOR Gate



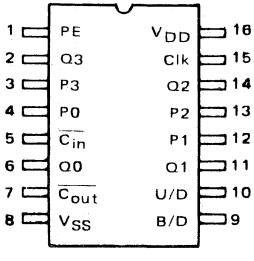
MC14027B
Dual J-K Flip-Flop



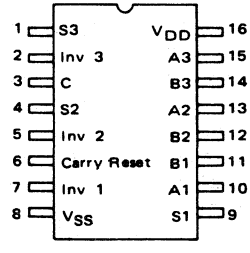
MC14028B
BCD-To-Decimal Decoder/
Binary-To-Octal/ Decoder



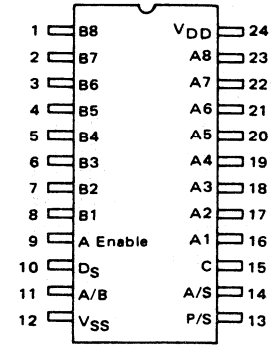
MC14029B
Binary BCD
Up/Down Counter



MC14032B
Triple Serial Adder
(Positive Logic)



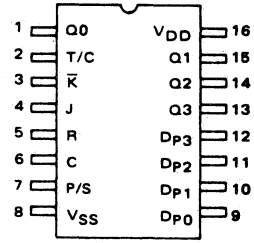
MC14034B
8-Bit Universal Bus Register



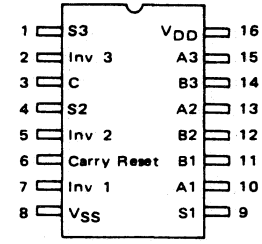
12

NC = No Connection

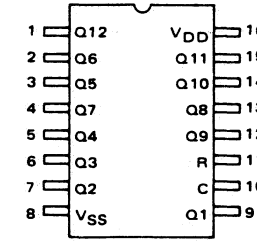
MC14035B
4-Bit Parallel-In/Parallel Out Shift Register



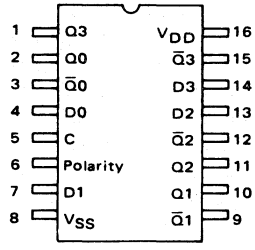
MC14038B
Triple Serial Adder (Negative Logic)



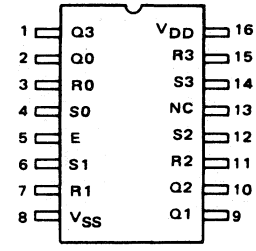
MC14040B
12-Bit Binary Counter



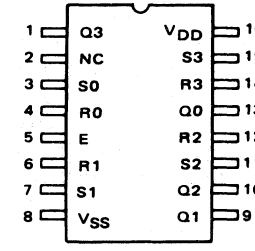
MC14042B
Quad Latch



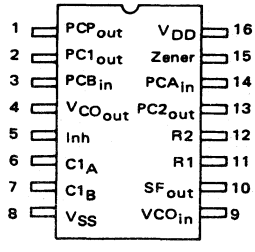
MC14043B
Quad NOR R-S Latch



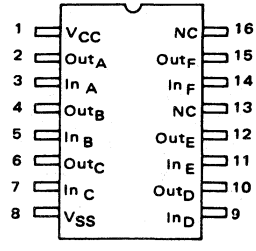
MC14044B
Quad NAND R-S Latch



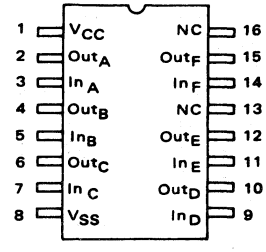
MC14046B
Phase-Locked Loop



MC14049UB
Hex Inverter/Buffer



MC14050B
Hex Buffer

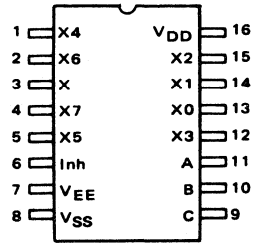


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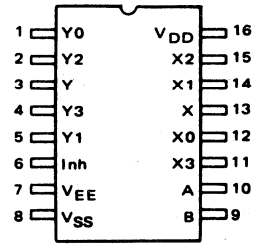
NC = No Connection

PIN ASSIGNMENTS (continued)

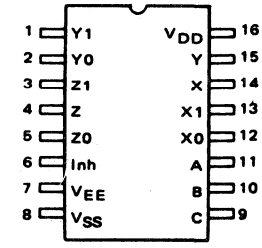
MC14051B
8-Channel Analog Multiplexer/Demultiplexer



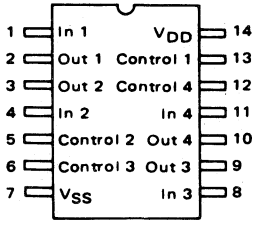
MC14052B
Dual 4-Channel Analog Multiplexer/Demultiplexer



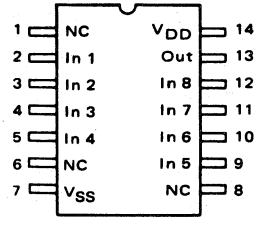
MC14053B
Triple 2-Channel Analog Multiplexer/Demultiplexer



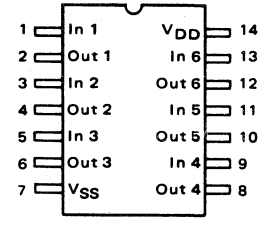
MC14066B
Quad Analog Switch Quad Multiplexer



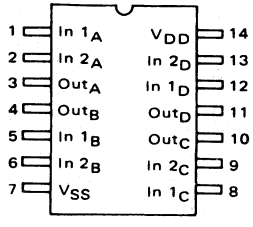
MC14068B
8-Input NAND Gate



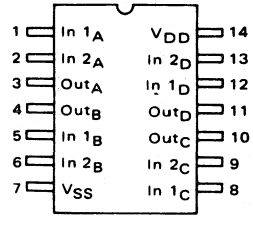
MC14069UB
Hex Inverter



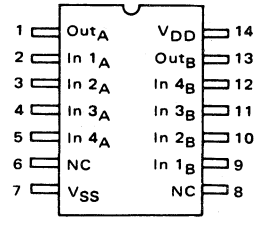
MC14070B
Quad Exclusive OR Gate



MC14071, MC14071B
Quad 2-Input OR Gate



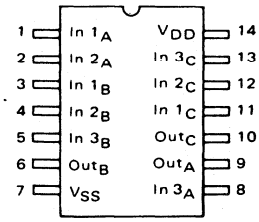
MC14072B
Dual 4-Input OR Gate



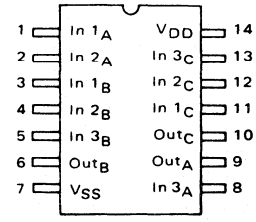
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NC = No Connection

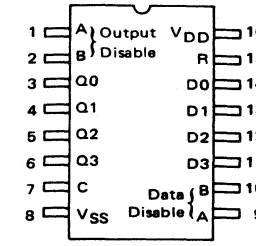
MC14073B
Triple 3-Input AND Gate



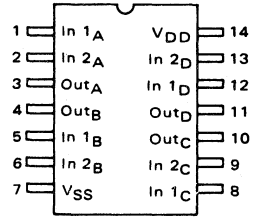
MC14075B
Triple 3-Input OR Gate



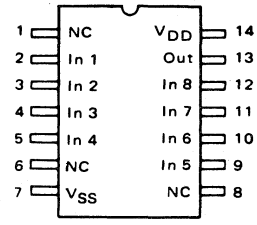
MC14076B
Quad D-Type Register



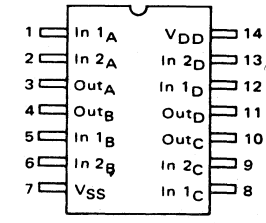
MC14077B
Quad Exclusive NOR Gate



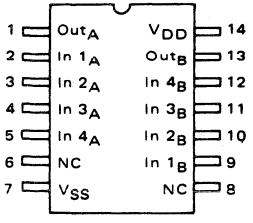
MC14078B
8-Input NOR Gate



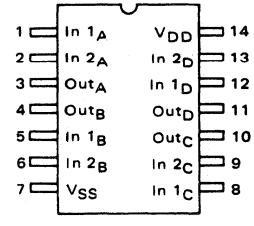
MC14081, MC14081B
Quad 2-Input AND Gate



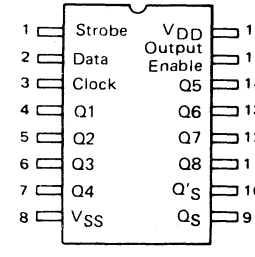
MC14082B
Dual 4-Input AND Gate



MC14093B
Quad 2-Input NAND Schmitt Trigger



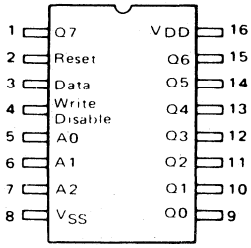
MC14094B
8-Stage shift/Store Register



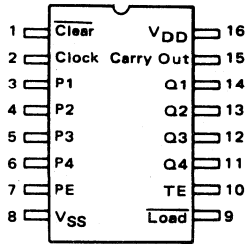
NC = No Connection

PIN ASSIGNMENTS (continued)

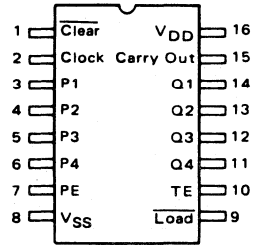
MC14099B
8-Bit Addressable Latch



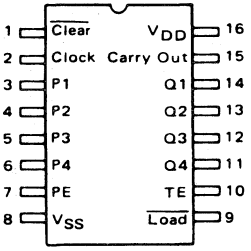
MC14160B
Decade Counter
with Asynchronous Clear



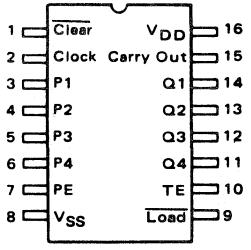
MC14161B
4-Bit Binary Counter
with Asynchronous Clear



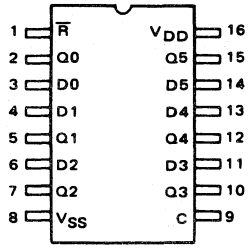
MC14162B
Decade Counter
with Synchronous Clear



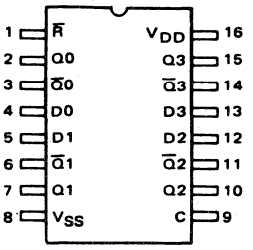
MC14163B
4-Bit Binary Counter
with Synchronous Clear



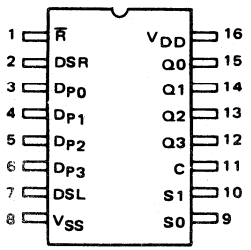
MC14174B
Hex Type D Flip-Flop



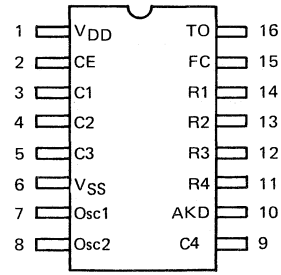
MC14175B
Quad Type D Flip-Flop



MC14194B
4-Bit Bidirectional
Universal Shift Register



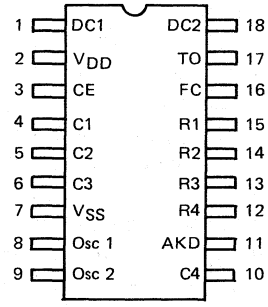
MC14403
Tone Encoder



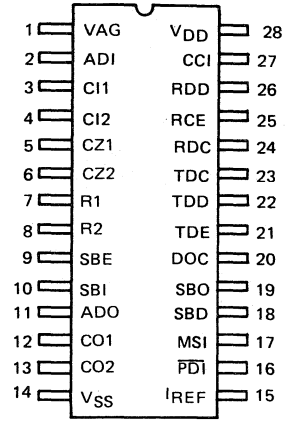
2

NC = No Connection

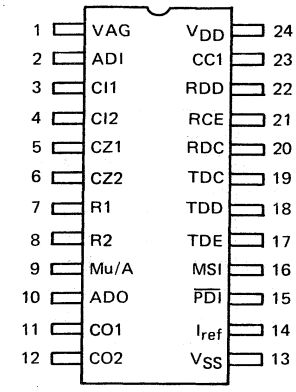
MC14405
Tone Encoder



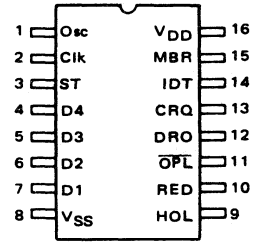
MC14406
PCM Codec



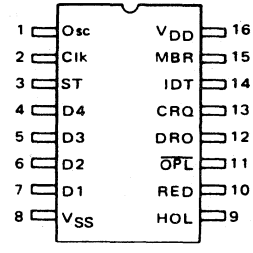
MC14407
PCM Codec



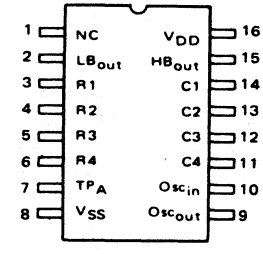
MC14408
Binary to Phone Pulse
Converter Subsystem



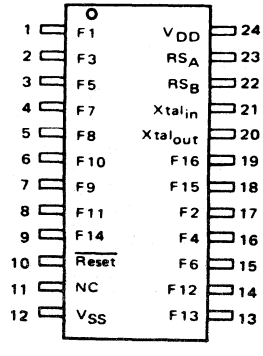
MC14409
Binary to Phone Pulse
Converter Subsystem



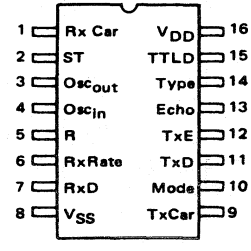
MC14410
2-of-8 Tone Encoder



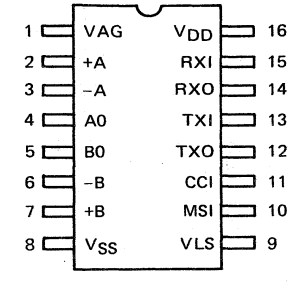
MC14411
Bit Rate Generator



MC14412
Universal
Low Speed Modem



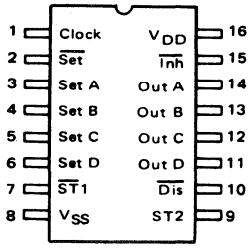
MC14413
PCM Filter



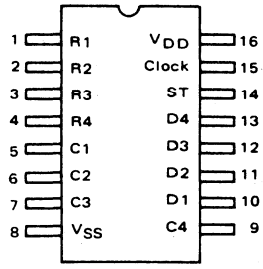
NC = No Connection

PIN ASSIGNMENTS (continued)

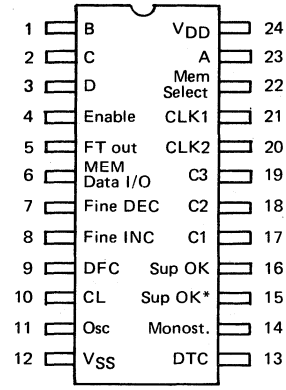
MC14415
Quad Precision Timer/Driver



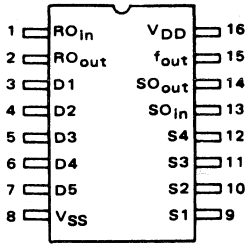
MC14419
2-of-8 Keypad-to-Binary Encoder



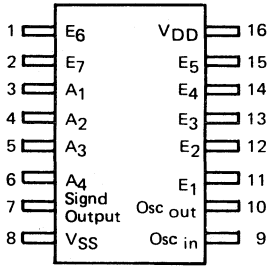
MC14421
Tuning Memory System Memory Interface Circuit



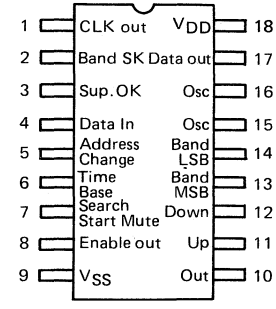
MC14422
Remote Control Transmitter



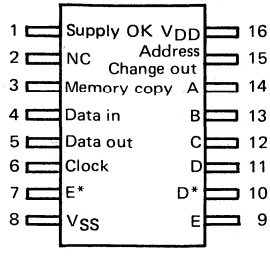
MC14424
Remote Control Transmitter



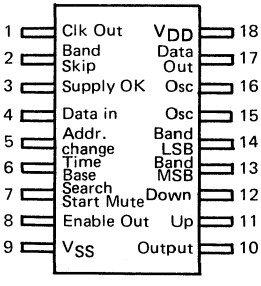
MC14425
Tuning Memory Control



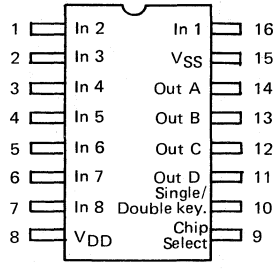
MC14426
Tuning Memory Circuit



MC14429A
Control Circuit for TV Tuning Kit

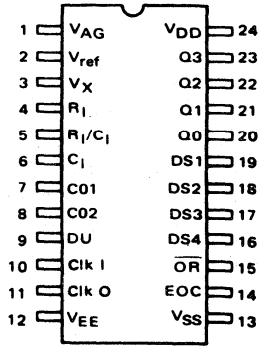


MC14430
Input Addressing Encoder

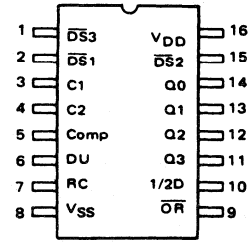


NC = No Connection

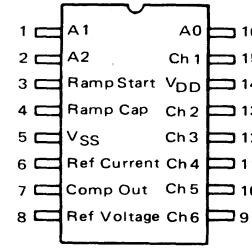
MC14433
3-½ Digit A/D Converter



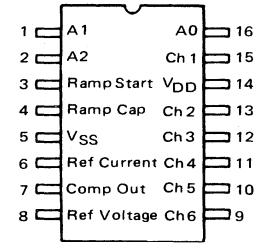
MC14435
3-½ Digit A/D Logic Subsystem



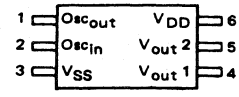
MC14443
A/D Converter Subsystem



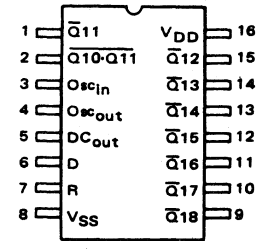
MC14447
A/D Converter Subsystem



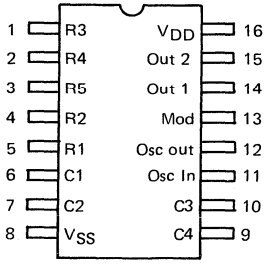
MC14450
Oscillator/216 Divider/ Buffer



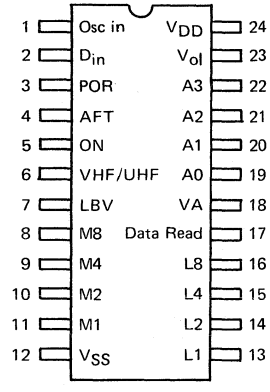
MC14451
Oscillator/211 to 219 Divider/ Buffered Duty Cycle Control



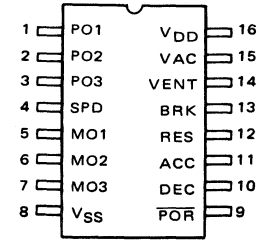
MC14457
Transmitter



MC14458
Receiver



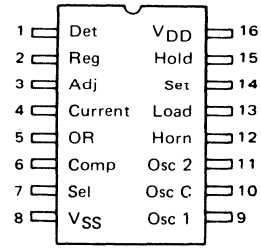
MC14459
Automotive Speed Control Processor



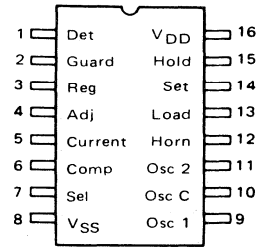
NC = No Connection

PIN ASSIGNMENTS (continued)

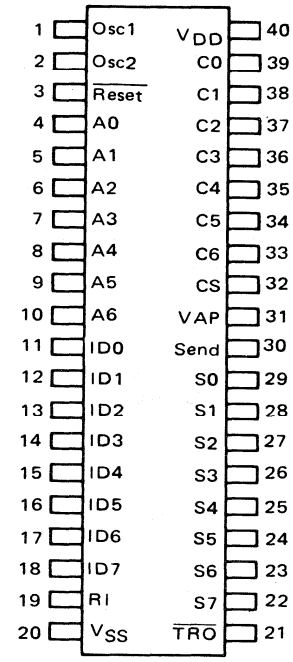
MC14461
Smoke Tetector Circuit



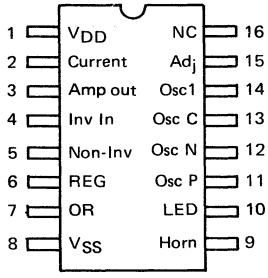
MC14462
Smoke Detector Circuit



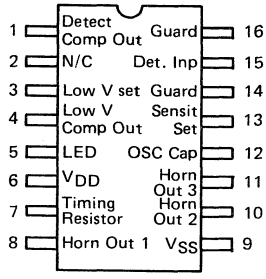
MC14469
Addressable Asynchronous Reveiver/Transmitter



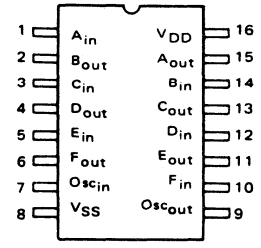
MC14464
MC14465
Smoke Detector Circuits



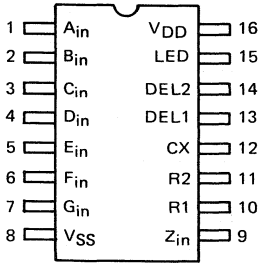
MC14466
Low Cost Smoke Detector



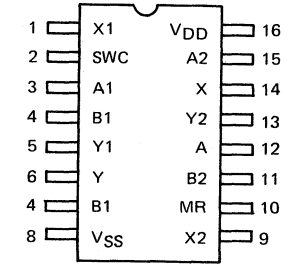
MC14490
Hex Contact Bounce Eliminator



MC14491
Multifunction Debounce Circuit

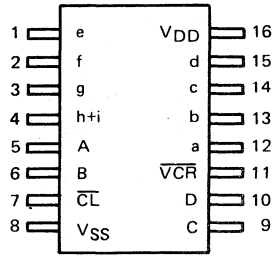


MC14492
Dual 2 x 2 Cross Point Matrix

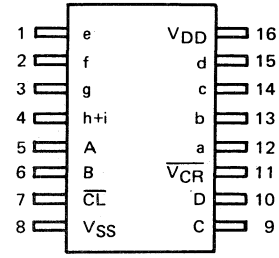


NC = No Connection

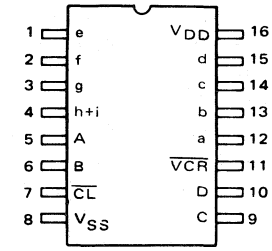
MC14493
Binary-to-7 Segment Latch/Decoder/Driver



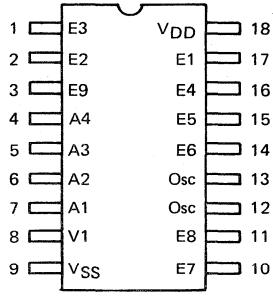
MC14494
Binary-to-7 Segment Latch/Decoder/Driver



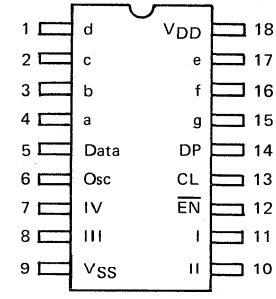
MC14495
BCD-to-7 Segment Hex Latch/Decoder/Driver



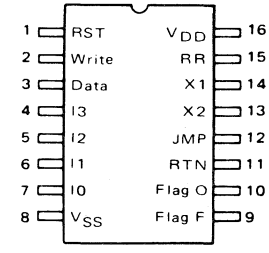
MC14497
AM/FSK Remote Control Transmitter



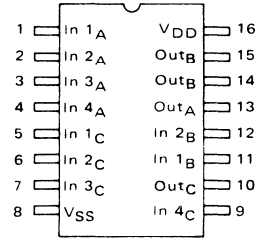
MC14499
Multiplexed Seven Segment Four Digit Driver



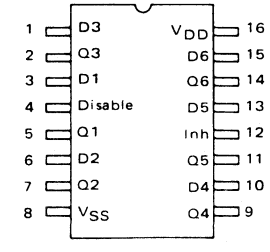
MC14500B
Industrial control Unit



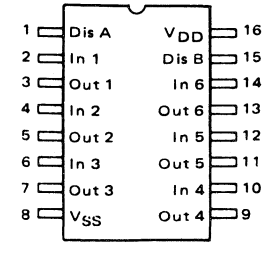
MC14501UB
Triple Gate



MC14502B
Strobed Hex Inverter/Buffer



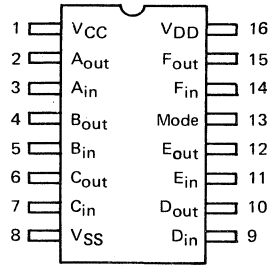
MC14503B
Hex 3-State Buffer



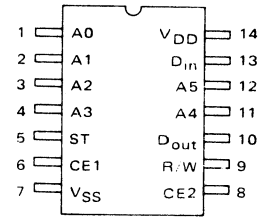
NC = No Connection

PIN ASSIGNMENTS (continued)

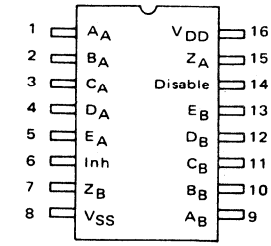
MC14504B
Hex TTL or CMOS to CMOS Shifter



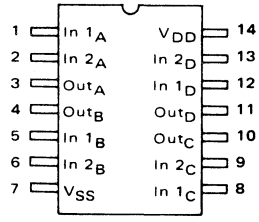
MCM14505
64-Bit Static Random Access Memory



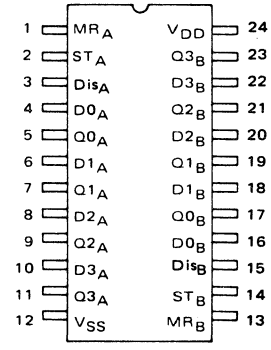
MC14506B
Dual Expandable AND-OR-INVERT Gate



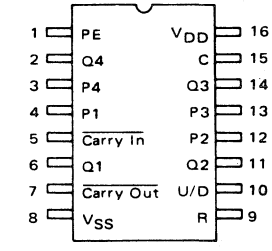
MC14507
Quad Exclusive OR Gate



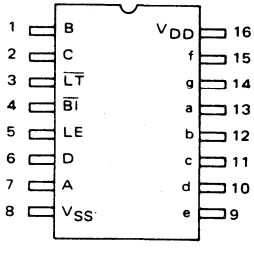
MC14508B
Dual 4-Bit Latch



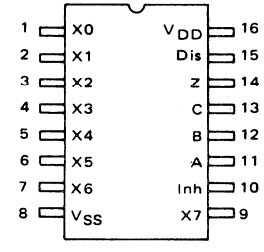
MC14510B
BCD Up/Down Counter



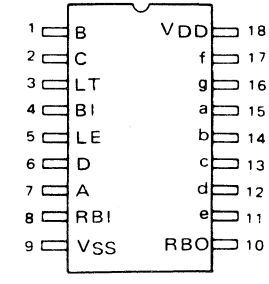
MC14511B
BCD-to-Seven Segment Latch/Decoder/Driver



MC14512B
8-Channel Data Selector

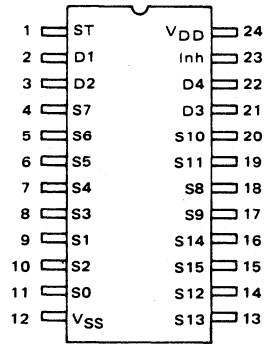


MC14513B
BCD-to-7 Segment Decoder/Driver

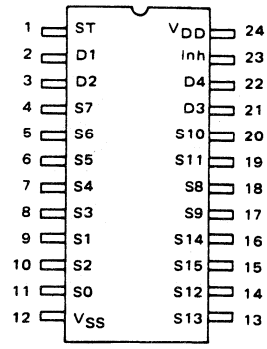


NC = No Connection

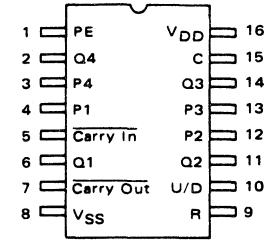
MC14514B
4-Bit Latch/4-to-16 Line Decoder



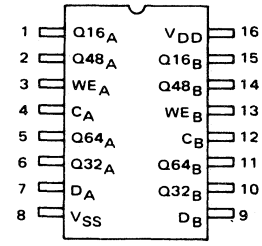
MC14515B
4-Bit Latch/4-to-16 Line Decoder



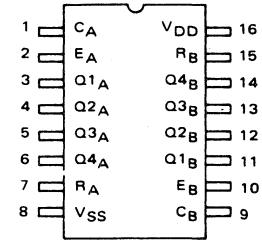
MC14516B
Binary Up/Down Counter



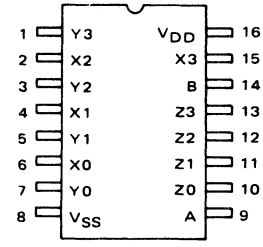
MC14517B
Dual 64-Bit Static Shift Register



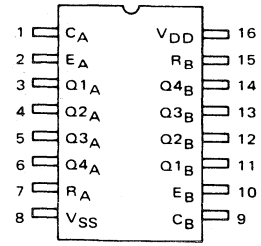
MC14518B
Dual BCD Up Counter



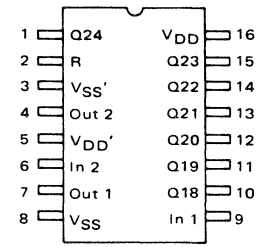
MC14519B
4-Bit AND/OR Selector



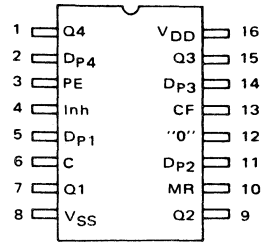
MC14520B
Dual Binary Up Counter



MC14521B
24-Stage Frequency Divider



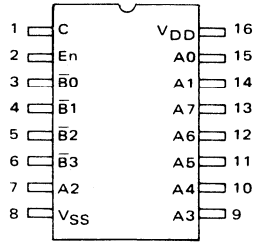
MC14522B
Programmable Divide-By-N-4-Bit BCD Counter



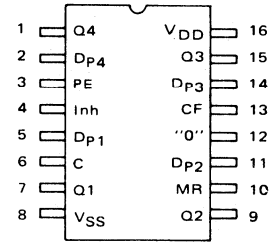
NC = No Connection

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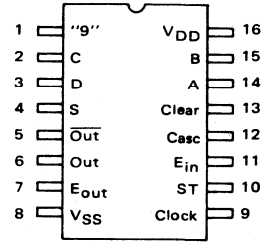
MCM14524
1024-Bit Read Only Memory



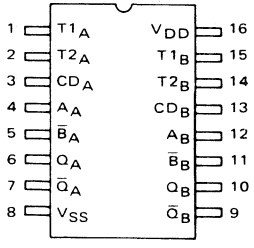
MC14526B
Programmable Divide-By-N-4-Bit Binary Counter



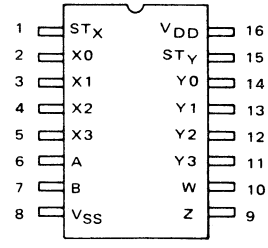
MC14527B
BCD Rate Multiplier



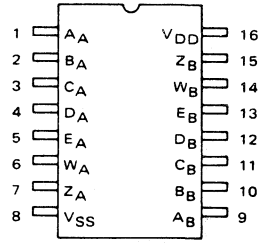
MC14528B
Dual Retriggerable/Resettable Monostable Multivibrator



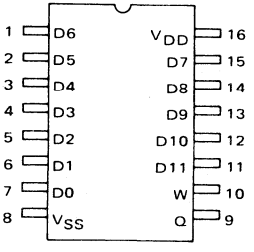
MC14529B
Dual 4-Channel Analog Data Selector



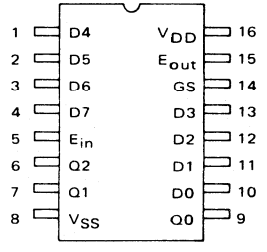
MC14530B
Dual 5-Input Majority Logic Gate



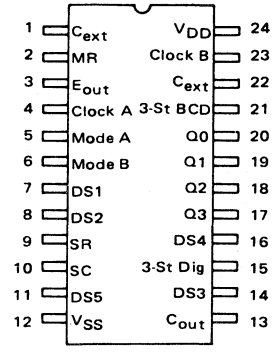
MC14531B
12-Bit Parity Tree



MC14532B
8-Bit Priority Encoder

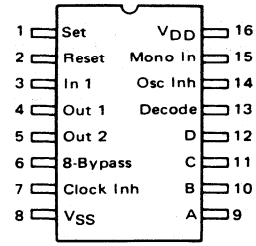


MC14534B
Real Time 5-Decade Counter

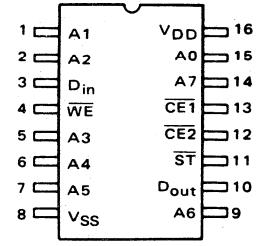


NC = No Connection

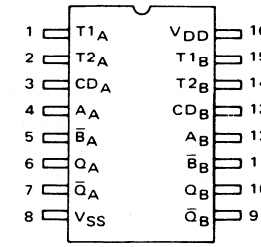
MC14536B
Programmable Timer



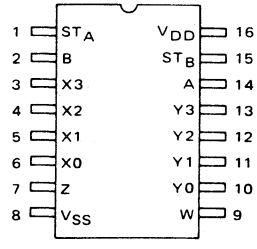
MCM14537
256-Bit Static Random Access Memory



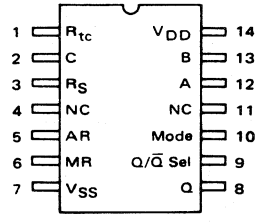
MC14538B
Dual Precision Retriggerable/Resettable Monostable Multivibrator



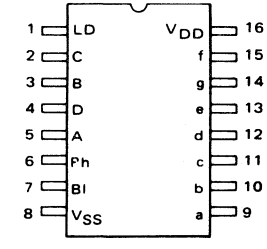
MC14539B
Dual 4-Channel Data Selector/Multiplexer



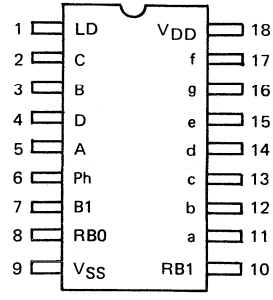
MC14541B
Programmable Oscillator/Timer



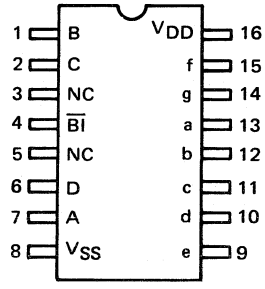
MC14543B
BCD-to-Seven Segment Latch/ Decoder/Driver



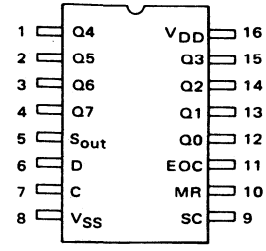
MC14544B
BCD-to-7 Segment Latch/Decoder/Driver Ripple Blanking



MC14547
BCD-to-7 Segment Decoder/Driver



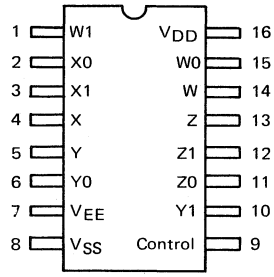
MC14549B
Successive Approximation Register



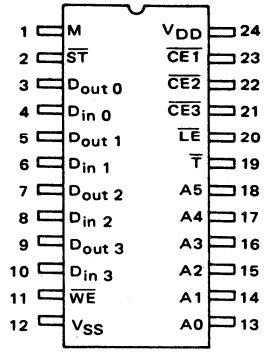
NC = No Connection

PIN ASSIGNMENTS (continued)

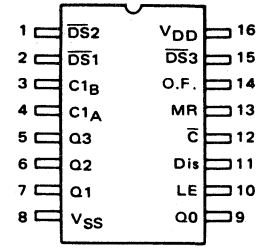
MC14551B
Quad 2-Channel Multiplexer



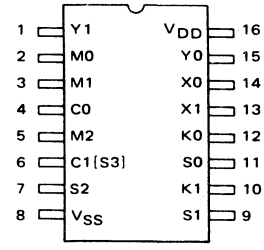
MCM14552
256-Bit Static Random Access Memory



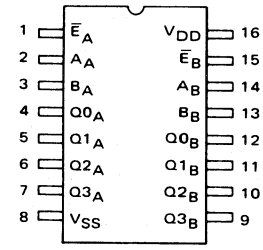
MC14553B
3-Digit BCD Counter



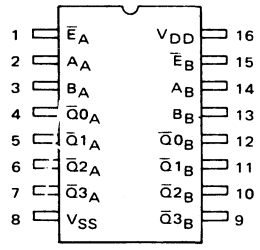
MC14554B
2 x 2-Bit Parallel Binary Multiplier



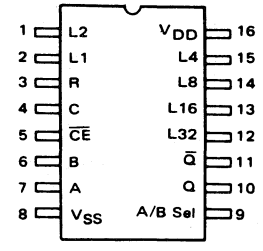
MC14555B
Dual Binary to 1-of-4 Decoder/ Demultiplexer



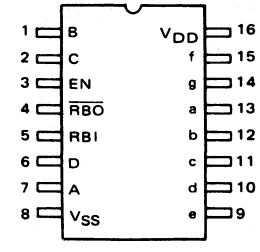
MC14556B
Dual Binary to 1-of-4 Decoder/ Demultiplexer



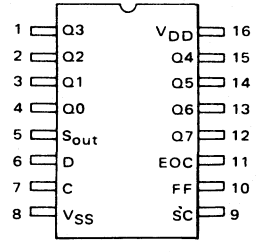
MC14557B
1 to 64-Bit Variable Length Shift Register



MC14558B
BCD-to-7 Segment Decoder

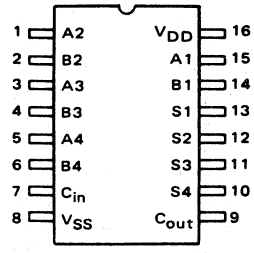


MC14559B
Successive Approximation Register

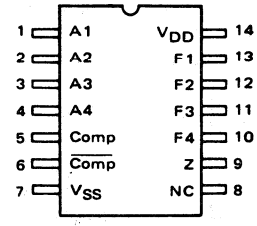


NC = No Connection

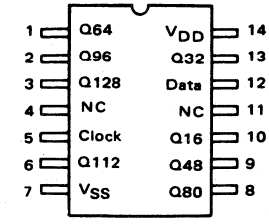
MC14560B
NBCD Adder



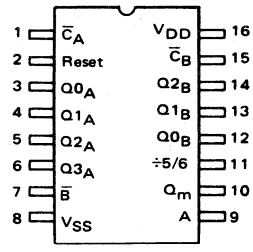
MC14561B
9's Complementer



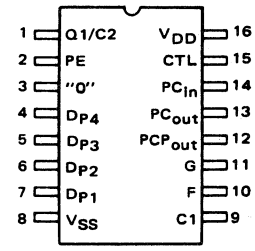
MC14562B
128-Bit Static Shift Register



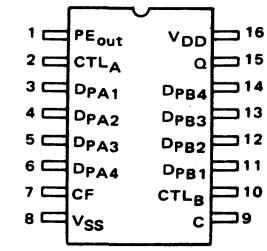
MC14566B
Industrial Time Base Generator



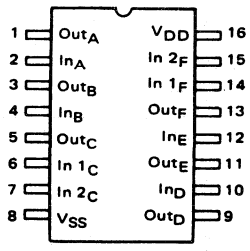
MC14568B
Phase Comparator and Programmable Counters



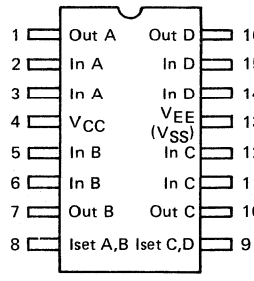
MC14569B
High Speed Programmable Divide-by-N Dual 4-Bit BCD/Binary Counter



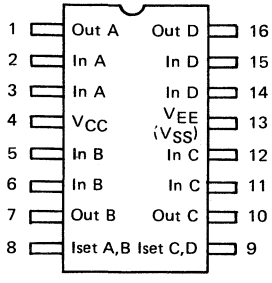
MC14572UB
Hex Gate



MC14573
Quad Programmable Op Amp



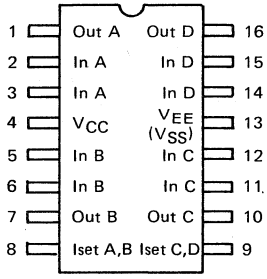
MC14574
Quad Programmable Comparator



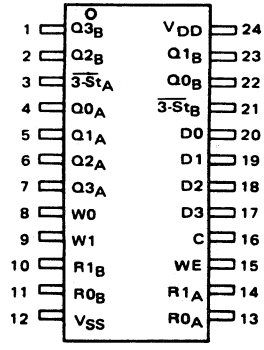
NC = No Connection

PIN ASSIGNMENTS (continued)

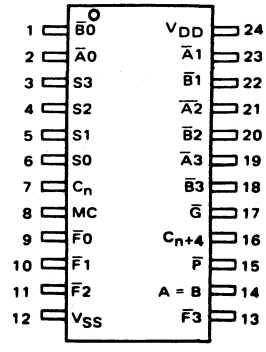
MC14575
Dual/Dual Programmable Op Amp Comparator



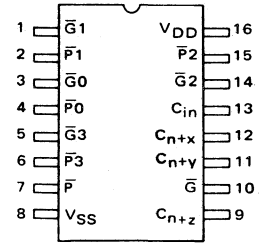
MC14580B
4 x 4 Multiport Register



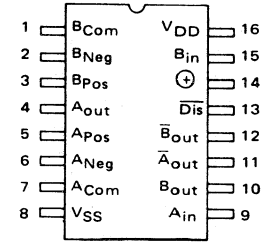
MC14581B
4-Bit Arithmetic Logic Unit



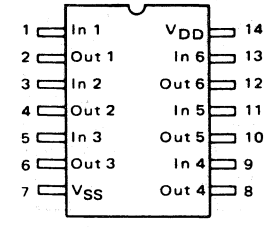
MC14582B
Look-Ahead Carry Block



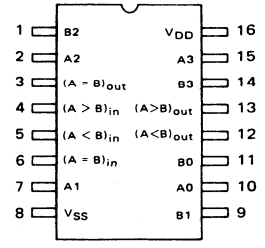
MC14583B
Dual Schmitt Trigger



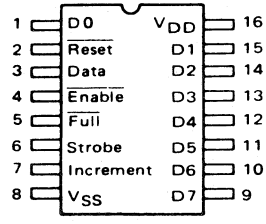
MC14584B
Hex Schmitt Trigger



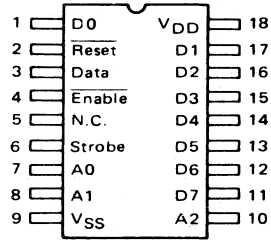
MC14585B
4-Bit Magnitude Comparator



MC14597B
8-Bit Latch/Counter

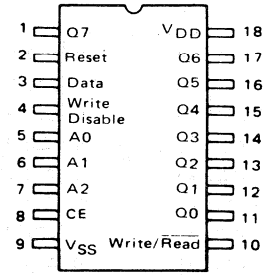


MC14598B
8-Bit Addressable Latch

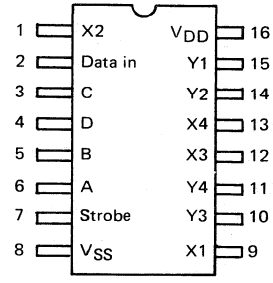


NC = No Connection

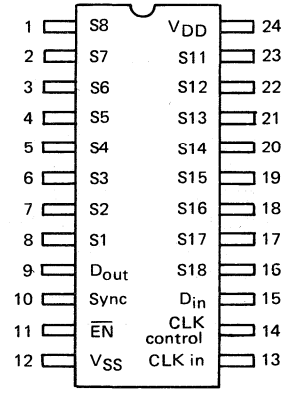
MC14599B
8-Bit Addressable Latch



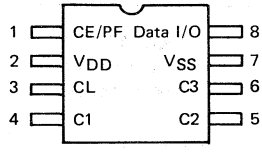
MC142100
4 x 4 Cross Point Switch w/Control Memory



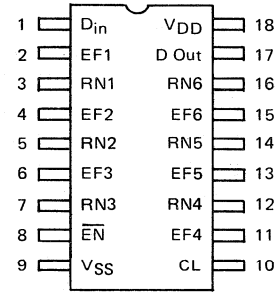
MC144100
32-Bit Register + 4-Digit Display Driver



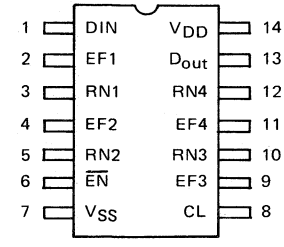
MCM144102
256-Bit (16 x 16) Static CMOS RAM



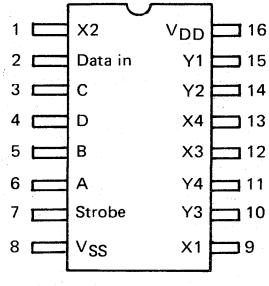
MC144110
Hex D/A Converter



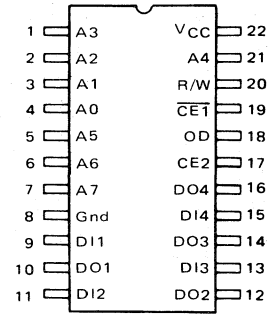
MC144111
Quad D/A Converter



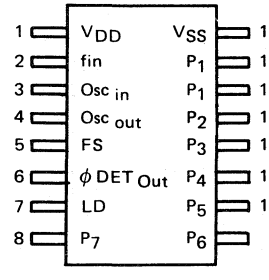
MC145100
4 x 4 Cross Point Switch w/Control Memory



MCM145101
1024-Bit Static Random Access Memory



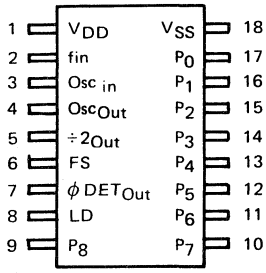
MC145104
PLL Frequency Synthesizer



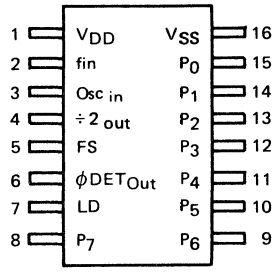
NC = No Connection

PIN ASSIGNMENTS (continued)

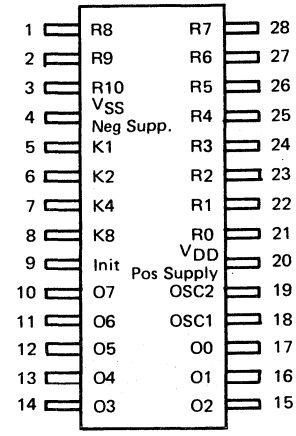
MC145106
PLL Frequency Synthesizer



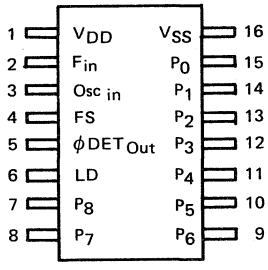
MC145107
PLL Frequency Synthesizer



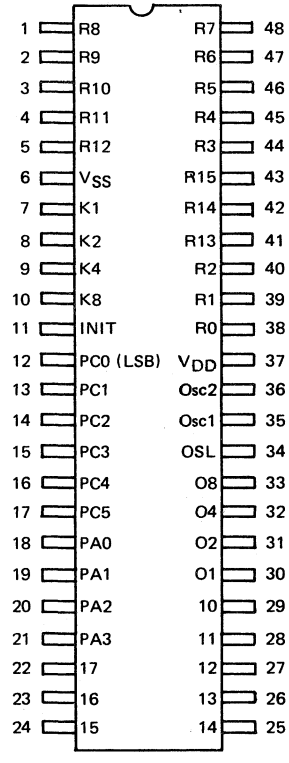
MC141000
One-chip 4-Bit Microcomputer



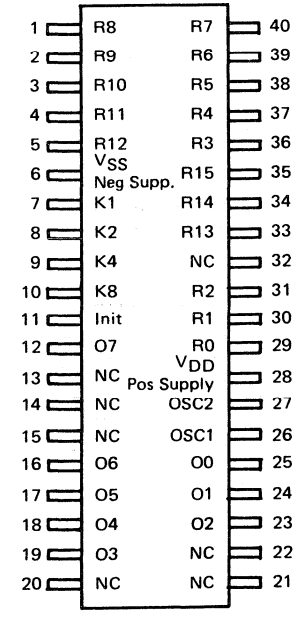
MC145109
PLL Frequency Synthesizer



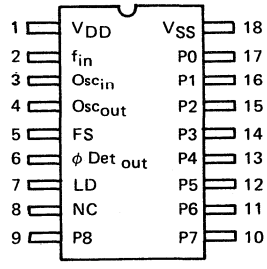
MC141099
4-Bit MPU



MC141200
One-chip 4-Bit Microcomputer

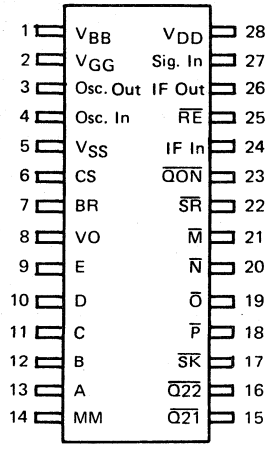


MC145112
PLL Frequency Synthesizer

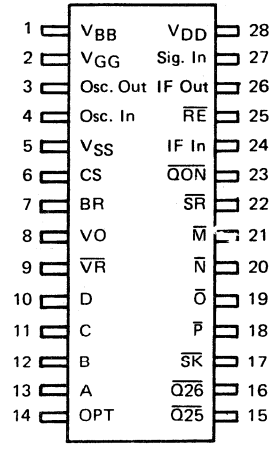


NC = No Connection

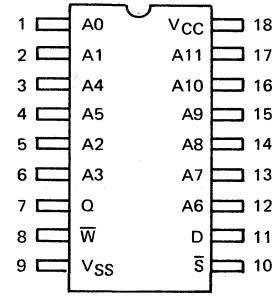
MC6526
Remote Control Receiver



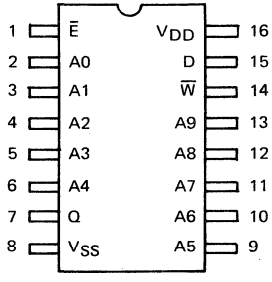
MC6529
Remote Control Receiver



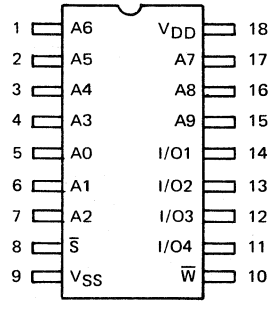
MC146504
4096 x 1-Bit Static RAM



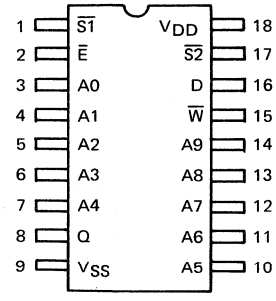
MCM146508
1024 x 1 Static RAM



MCM146514
1024 x 4 Static RAM



MCM146518
1024 x 1 Static RAM

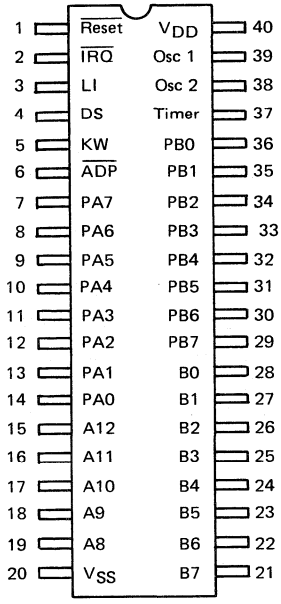


NC = No Connection

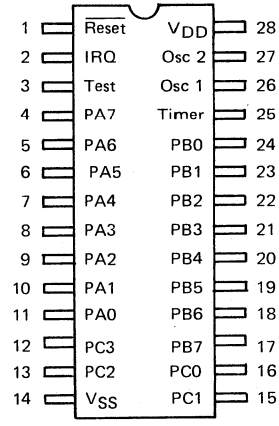
PIN ASSIGNMENTS (continued)

MC146805 Series
Microprocessors/Microcomputers

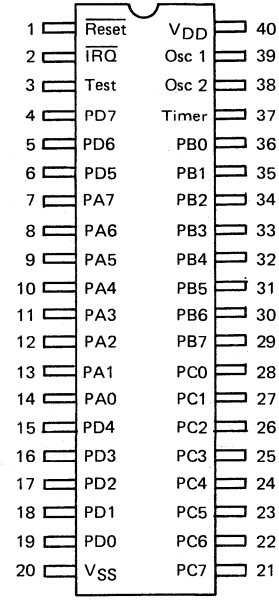
MC146805E2



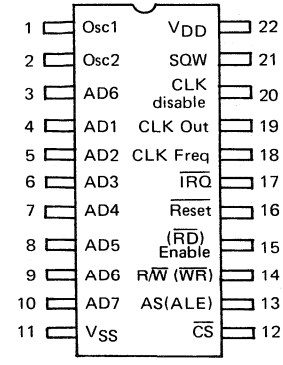
MC146805F2



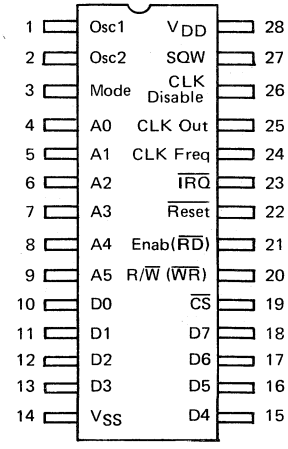
MC146805G2



MC146818
Real Time Clock/RAM



MC146819
Real Time Clock/RAM



NC = No Connection

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